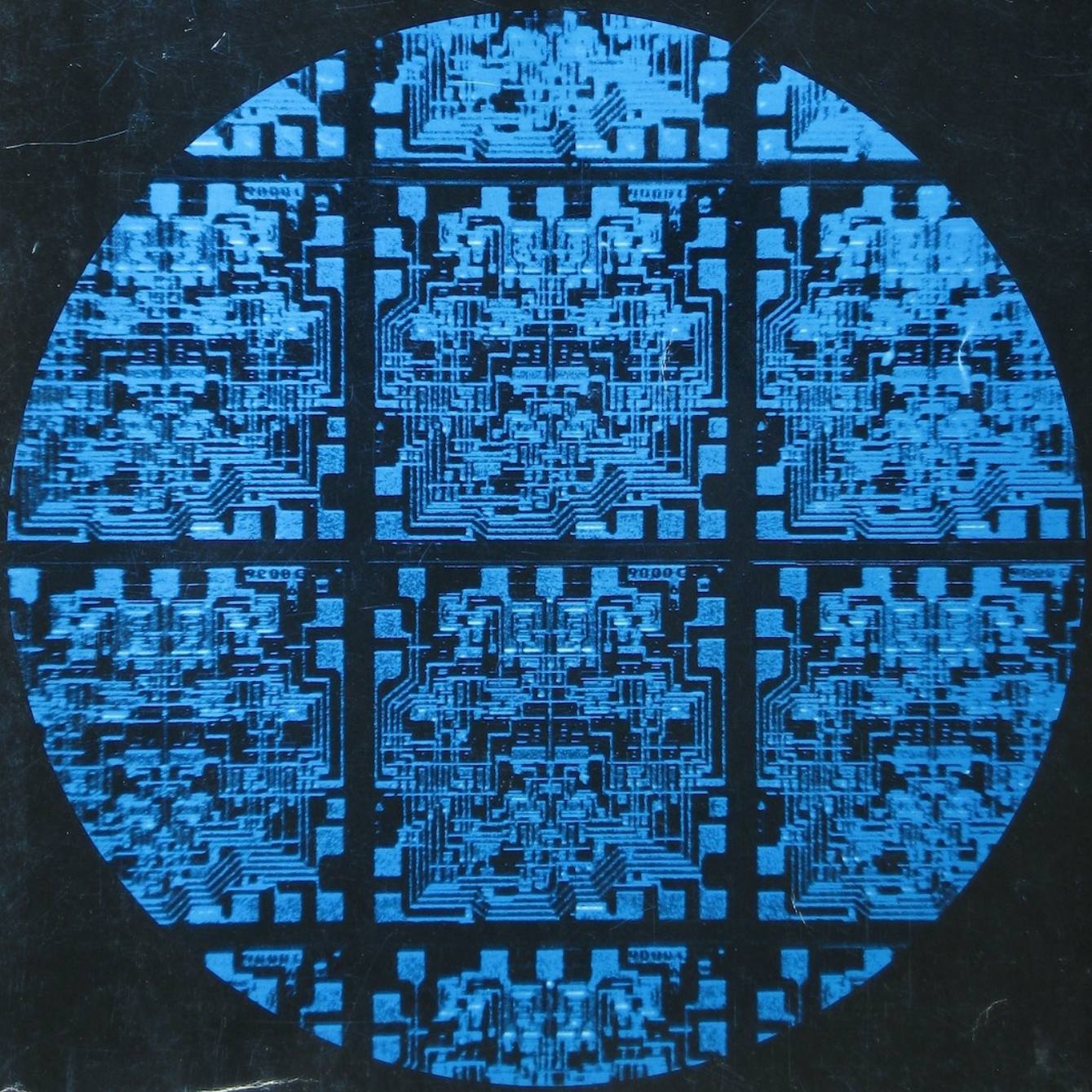
Fairchild Semiconductor Integrated Circuits



Fairchild Semiconductor Integrated Circuits

Written and Edited by E. Floyd Kvamme and L. H. Bieler

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Total capability is an important concept at Fairchild Semiconductor. As the largest and most experienced manufacturer of semiconductor devices in the world, Fairchild knows and understands the needs of the industry for which it is the leading supplier, and prides itself in its ability to design products which meet those needs. Over the years, this capability has led to the development of the most comprehensive line of digital and linear microcircuits the world has ever seen, produced in volume under a number of Fairchild patented processes ■ Fairchild Semiconductor was founded in 1958 by a group of eight scientists who saw the myriad possibilities inherent in silicon mesa technology. Since that time, facilities have been expanded again and again to meet the demand for Fairchild's superior products. (Fairchild ships over one million units every month.) Plant locations now include California, New Mexico, and Maine, with affiliated plants in Hong Kong, Australia, Italy, Great Britain, France, Germany, and Sweden. Still further expansion is under consideration ■ The technology behind this rapid growth and overwhelming acceptance is Fairchild's patented Planar* process, which incorporates the latest state-of-the-art developments to ensure the utmost in performance, stability, and reliability ■ Years of production experience stand behind these products - production experience which has enabled Fairchild to maintain price leadership across the board since it filled the first commercial order for a silicon mesa transistor in 1958 ■ Technology and experience combine to make this complete line of integrated circuits the most advanced and most reliable in the industry today - available at the lowest possible cost. For years, the name "Fairchild" has been synonymous with quality, leadership, and reliability.

We plan to keep it that way.

*Planar is a patented Fairchild Process

The digital integrated circuits are presented according to three technological groupings with similar genetic characteristics: 1) Current Sourcing, 2) Current Sinking, and 3) Current Mode.

As used here, Current Source and Current Sink require some brief explanation. A common analogy is the kitchen sink, where the tap is the "source" and, of course, the place where the water goes is the "sink".

For RTL, current must flow from an output and be forced into the input of a similar RTL to activate the output of the second circuit. The output of the RTL, then, resembles the water tap of our analogy inasmuch as it is a "source".

DTL, however, requires a flow of current *out* of its input(s). Hence, the output stage of a circuit preceding a DTL gate resembles a "sink", in that it must provide a place for the outflowing current to go.

Current Mode circuits (CTL, CML) may either sink or source current, and take several forms. Their name is derived from their ability to change logic levels by switching between two active current levels or modes. They commonly employ emitter-follower, or emitter-coupled circuitry.

Current Sourcing

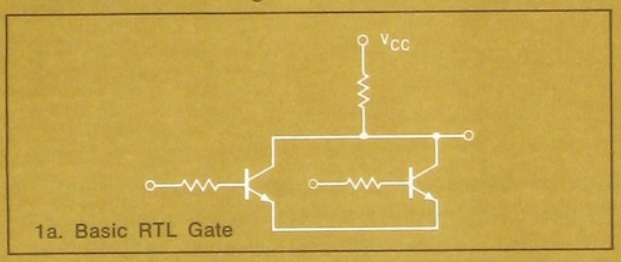
General Characteristics

Logic Current flows into inputs
Drive current flows out of outputs
Gate performs positive NOR function
Simplest logic form - good for complex circuits

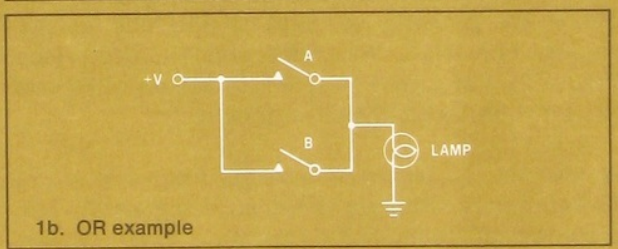
Figure 1a shows a typical RTL gate. Logically, this circuit performs the NOR gating function. Figure 1b has become a classic example of an "OR" circuit, demonstrating that when switch A and/or switch B is closed, the lamp lights - i.e., we have an output. An OR gating function, then, is performed when one, all, or any combination of "positive" events, defined here as the closing of switches, results in another positive event (in this case, the lighting of the lamp). Had we connected the circuit as in Figure 1c, while retaining our same definitions, we would have obtained a NOR result; that is, if we were to close either switch A or switch B, we would not have an output (the lamp would not light). Functionally, circuits 1a and 1c are identical in that they are both NOR circuits. Defining a "high" voltage condition (H) as a positive event, and a "low" voltage condition (L) as a negative event, we see that the RTL gate is a NOR gate: a high on the input of any or all of the bases saturates one or more transistors and forces the output to its low level.

The NOR gate may also be considered as an OR gate followed by an inverter.

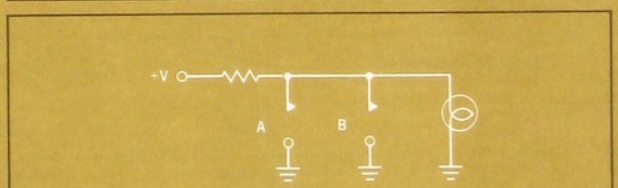
Figure 1. OR/NOR Gating Examples



1a. Basic RTL Gate



1b. OR example



1c. NOR example

Figure 2 shows the output of an RTL gate driving the inputs of several other RTL circuits. Note that no particular RTL family need be specified. Fan-out is the ratio of I_A to I_{IN}: I_A is determined by V_{CC} and R_2. I_{IN} is determined, primarily, by the h_{FE} of the transistor being driven and R_1.

The RTL families, then, may be intermixed by changing the loading rules, as illustrated in Figure 3. I_{IN} of the Low Power RTμL has been given a normalized value of 1. I_{IN} of the RTμL is three times the I_{IN} of the Low Power RTμL. In Figure 3, for example, we see that one RTμL9903 element would drive sixteen Low Power RTμL9910 or five RTμL9914 inputs. Circuit C_1 of Figure 2 is the current source for circuits C_2, C_3 and C_n.

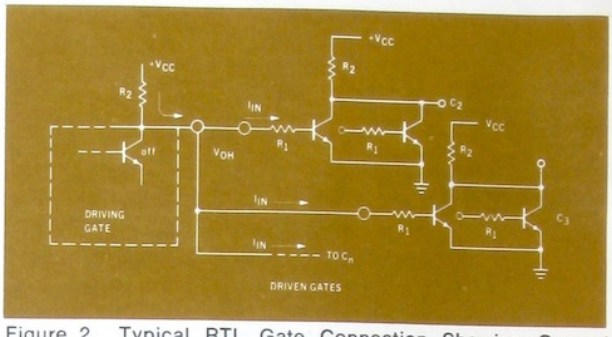
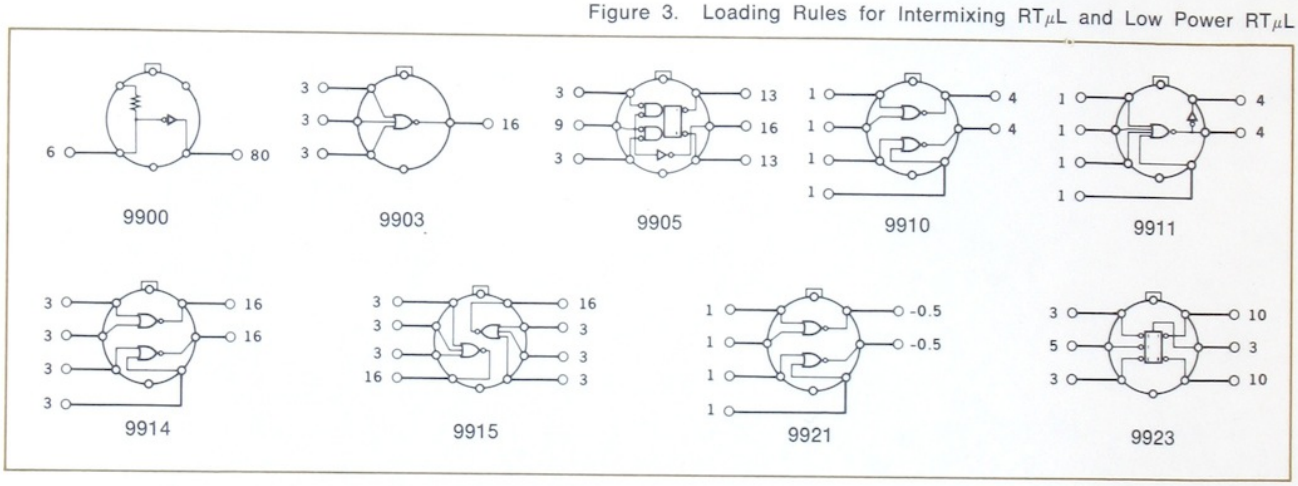


Figure 2. Typical RTL Gate Connection Showing Current Sourcing

Figure 3. Loading Rules for Intermixing RTμL and Low Power RTμL



Another important difference in the RTL families is speed. As the various RTL families use transistors which are essentially identical, speed variations are primarily a result of different resistor values. For RTμL, R_1=450Ω and R_2=640Ω (see Figure 2). For Low Power RTμL, values of R_1 and R_2 are 1.5KΩ and 3.6KΩ respectively.

A transfer of electrical charge from one point to another is required to switch a transistor. The dimensional relationship between time, charge, current, resistance, and capacitance may be expressed as $t=\frac{Q}{I}=\frac{CV}{I}=RC$; time increases as R and C increase. Assuming constant capacitance, and identical transistors, time is primarily a function of resistance, which is greater for Low Power RTμL than for RTμL. While RTμL and Low Power RTμL capacitances are about the same, a change in the resistor values causes the switching speed of Low Power RTμL to be higher than that of RTμL. The following comparisons are for an RTμL9914 and a Low Power RTμL9910:

Characteristic	RTμL	Low Power RTμL	Ratio of Low Power RTμL to RTμL
R_1	**450Ω**	**1.5KΩ**	**3.3:1**
R_2	**640Ω**	**3.6KΩ**	**5.6:1**
t_{pd} (typ)	**15 ns**	**30 ns**	**2.0:1**

Current Sinking

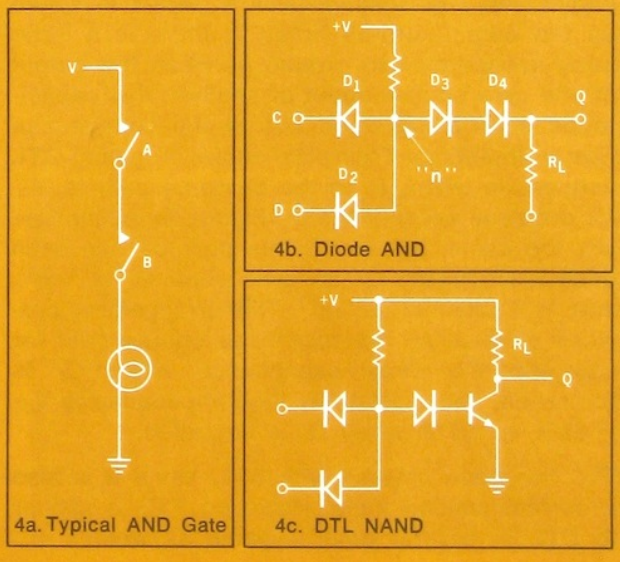
General Characteristics

Logic current flows out of inputs
Outputs "sink" drive current
Gate performs positive NAND function
Highest voltage noise immunity

DTL is NAND logic. An AND circuit is one such as Figure 4a, in which only one set of conditions will activate the output. That is, closing switches A and B will turn on the lamp, but if either or both switches are open, the lamp will not light.

Figure 4b is a diode AND gate. For the output (Q) to be at a high level, inputs C and D must be at a high level (diodes D_1 and D_2 must be off). If either input C or D is connected to ground, the voltage at n will be insufficient to turn on D_3 and D_4, and no current will flow through R_L; point Q will remain at zero volts. The replacement of D_4 and R_L in Figure 4b with a transistor produces a NAND circuit, as in Figure 4c, since the transistor inverts the output. R_L in Figure 4c is used to speed up the switching times; it is not necessary for logic performance.

Figure 4. AND Circuit examples

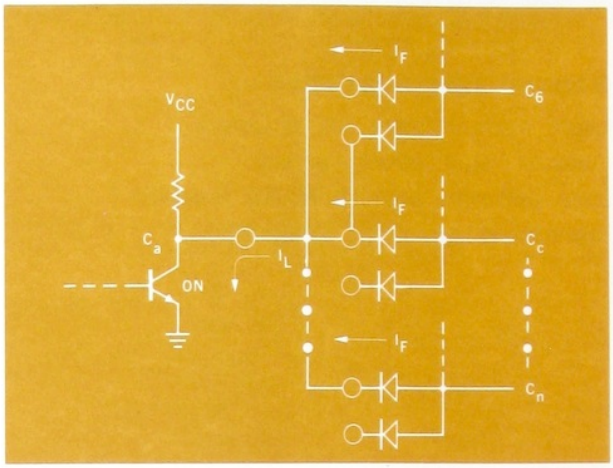


4a. Typical AND Gate

4b. Diode AND

4c. DTL NAND

Figure 5. Typical DTL NAND Connection Showing Current Sinking.



In Figure 5, current flows from circuits C_b, C_c, C_n, representing current sinking (i.e., the current must be drawn from the inputs.) DTL fan-out will be determined by the ratio I_{OL}/I_F.

The discussion of speed characteristics for RTL also applies to DTL. There is, however, another method sometimes used to speed up circuits driving highly capacitive loads. As mentioned earlier, the DTL load resistor is added to speed up the output turn-off times. If there is a large stray capacitance to ground between the output of one gate and the input of another, this capacitance must be charged before the voltage can rise to threshold. Figure 6a shows a typical DTL connection where R_L is the charging path to V_{CC} for the stray capacitance C_S. Figure 6b is functionally the same, but an "active pull-up" has been added. Transistor Q_3 is "on" when Q_2 is "off", and "off" when Q_2 is "on". This arrangement provides a relatively low resistance charge path for charging the stray capacitance when Q_2 is turned off, and a relatively high impedance to V_{CC} (1.85 K + .15 K) when Q_2 is saturated.

TTL has been classed with DTL, since it is also a current sinking logic. However, TTL is similar to DTL in several other aspects as well.

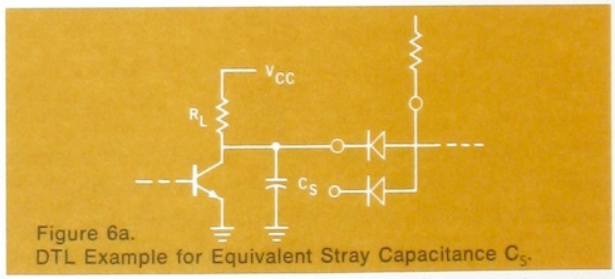
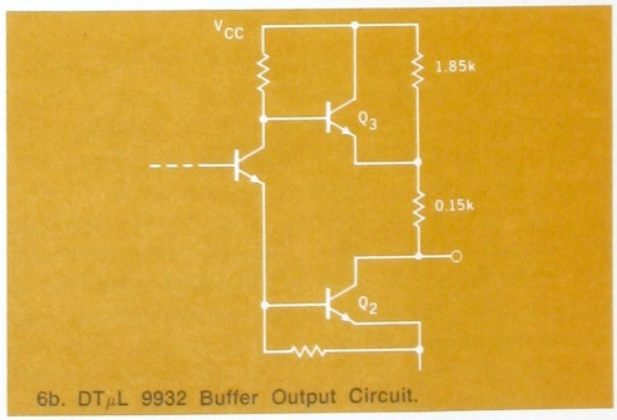
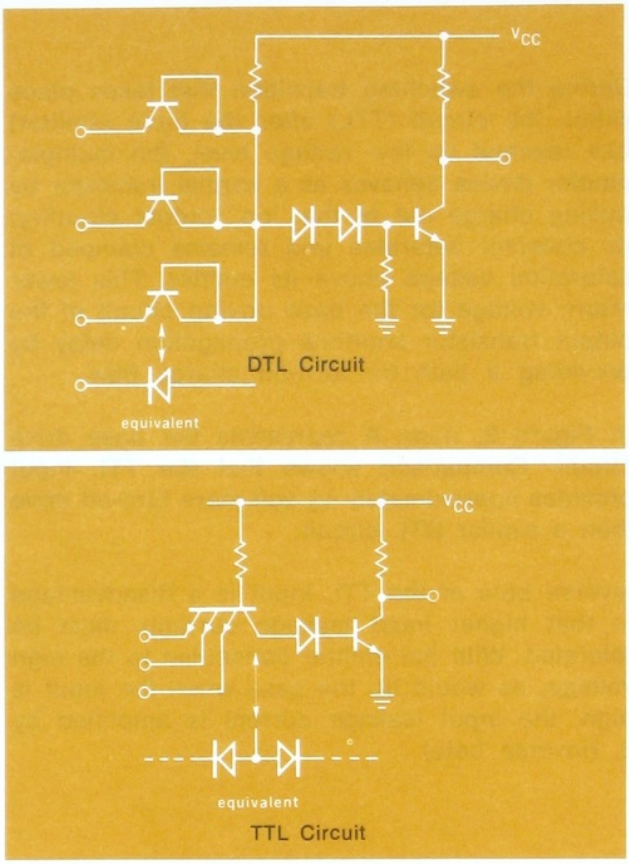


Figure 6a.
DTL Example for Equivalent Stray Capacitance C_S.



6b. DTμL 9932 Buffer Output Circuit.

Figure 7. Comparison for DTL and TTL



Comparison of the simple DTL and TTL circuits in Figure 7 reveals that they differ only in their input circuitry. The DTL circuit has been drawn showing the transistor emitter inputs with their collector-base junctions shorted, which is the circuit configuration used for Fairchild DTμL. (The emitter-base diode has lower capacitance and lower forward voltage drop than the base-collector diode, and is used in preference to it primarily because it has faster switching characteristics.) Operationally, the circuits are identical. A "low" on the input of the TTL gate shunts current away from the base circuit of the inverting transistor, and the output goes to a high level. With a "high" on the inputs, the current flows through the base-collector diode of the multiple-emitter input transistor. If we dissect the DTL and the TTL circuits of Figure 7 and show the current paths, the similarity is readily apparent. (See Figure 8.)

The TTL circuit has one advantage and one disadvantage peculiar to the multiple-emitter transistor. The advantage is speed and the disadvantage is inverse beta leakage.

Figure 8. Input Comparison for DTL and TTL

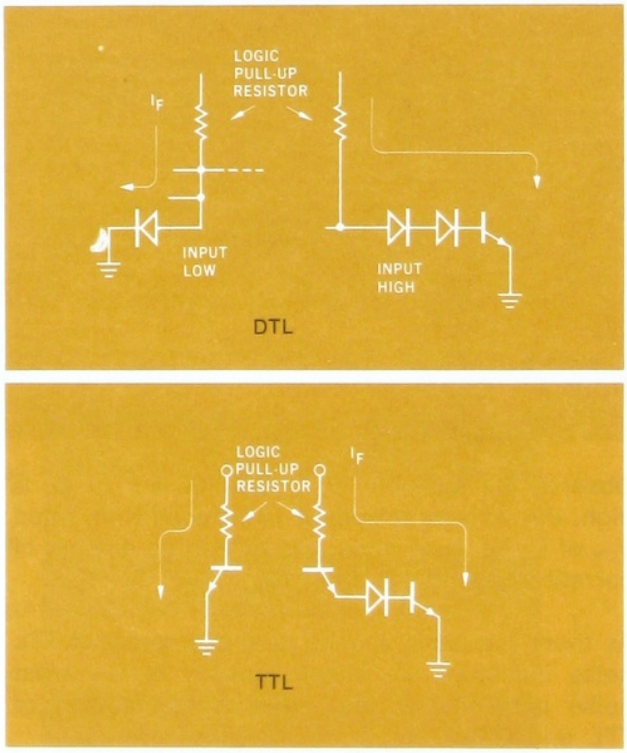
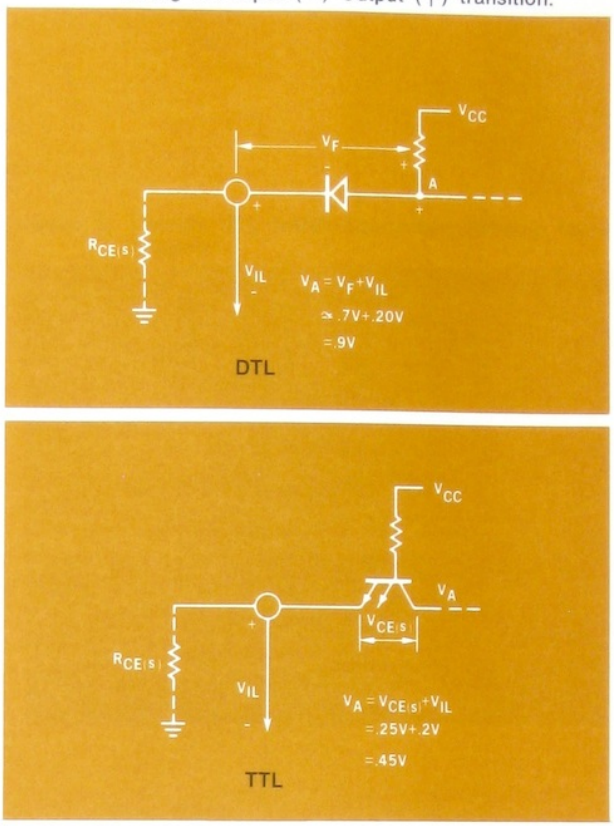


Figure 9. Comparison of voltage drop for DTL and TTL during the Input (—) Output (+) transition.

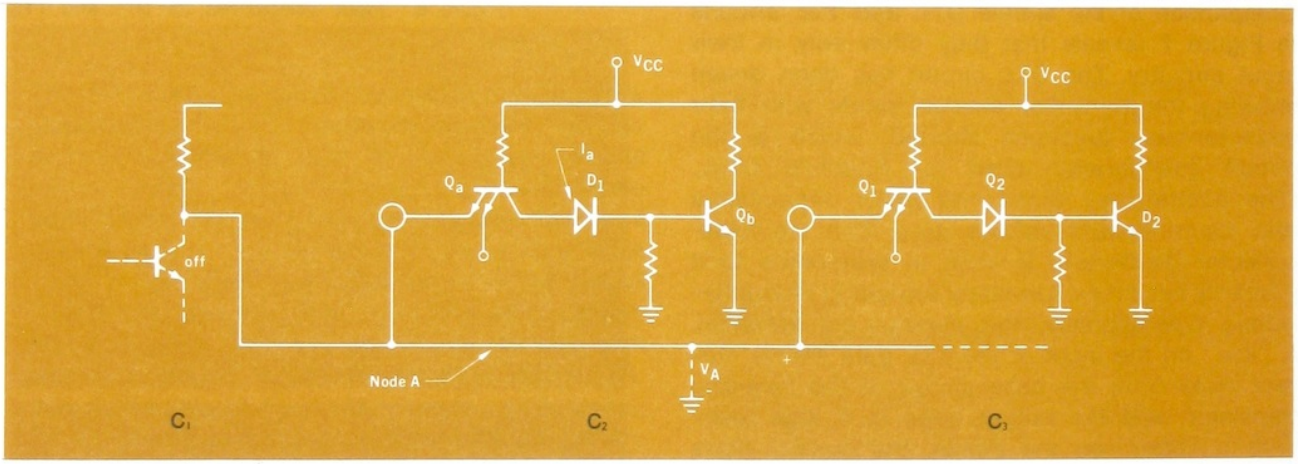


During the switching transition that takes place within the circuit (TTL) after the input (emitter) has reached its low voltage level, the multiple-emitter device behaves as a normal transistor by pulling charge out of the "on" output circuitry; its collector saturates and remains clamped at saturation voltage above its emitter. This lower return voltage for the base driving circuit of the output transistor shortens propagation delay by providing a path for turn-off charge flow.

In Figure 9, node A represents the base drive circuit. Comparison shows that the TTL input provides approximately ½ volt more turn-off drive than a similar DTL circuit.

Inverse beta of the TTL input is a disadvantage in that higher input leakage currents must be tolerated. With the emitter connected to the high voltage, as would be the case when the input is high, the input leakage current is amplified by β_I (inverse beta).

Figure 10. TTL Example for Parallel Gate Operation.



Observe the example of Figure 10. If β_I of Q_a is high, the voltage at node A is reduced from rated V_{OH} of C_1 because node A is pulling an amount of current equal to $\beta_I I_a$ from C_1.

As there has been a good deal of interest in TTL noise immunity, we should quickly review what noise immunity is, and make a comparison of TTL and DTL.

Noise immunity is a measure of safety margin; there are three margins one must consider: low level, high level, and a.c.

Low-level noise immunity is the difference between the threshold voltage of the circuit being driven and the most positive low-level voltage of the driving circuit. In Figure 11, this would be the difference between V_{TH} and V_L (max.)

Similarly, high-level noise immunity is the difference between V_H(min) of the driving circuit and V_{TH} of the driven circuit. Noise immunity, then, is that amount of voltage spiking, positive or negative, that can be tolerated at V_L or V_H without exceeding the next threshold level and causing an error.

In reality, the threshold voltage is not a single value, but a region. There are two factors that must be considered: first, the threshold varies, within limits, of course, from unit to unit. Secondly, there is a minimum value required to hold an input circuit fully "on" for full fan-out, and a maximum value that can be applied without turning the circuit partially "off".

Figure 12 shows the voltage levels for DTL noise immunity calculation.

Using these values, we see that worst-case noise immunity at 25°C is:

High Level

$$N.I._{HL} = V_{OH} - V_{IH}$$
$$= 2.6V - 1.9V$$
$$= 0.7V$$

Low Level

$$N.I._{LL} = V_{IL} - V_{OL}$$
$$= 1.10V - 0.40V$$
$$= 0.7V$$

Typically, V_{OH} would be in excess of 4V, V_{OL} about 0.25V, V_{IL} about 1.3V, and V_{IH} less than 1.7V, for which a typical rating of 1 volt is the low level noise immunity usually given by manufacturers of DTL circuits.

Figure 11. Voltage Levels for Transistor Logic Circuits.

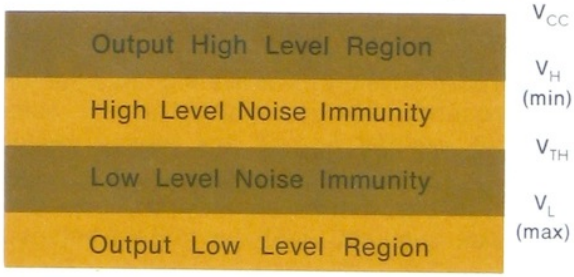


Figure 12. D.C. Voltage Levels for DTL Noise Immunity at 25°C

Spurious noise signals are present in every system. Some are externally generated and are electromagnetically coupled to the system through the atmosphere or the power line. Others are generated internally by relays or neighboring logic. Their frequency and magnitude cover a very wide spectrum. Some can be shielded out or designed around; others can be disregarded; and still others, one must learn to live with. The subject of a.c. noise immunity studies a system's immunity to these spurious noise sources.

A.C. noise immunity is usually most critical during the time that a circuit is switching through the threshold level. The following factors normally apply:

1. The switching transition time interval.
2. The stray capacitances that limit the circuit switching times may shunt noise to ground.
3. Most noise signals exhibiting high voltage and narrow pulse width have insufficient power to drive many logic circuits.

For purpose of analysis, noise signals of relatively low frequency may be regarded as d.c. noise. If a circuit exhibits ringing just after a switching transition, which can be considered self-generated noise, the a.c. noise immunity is less than the d.c. noise immunity until the ringing settles out.

The TTL circuit of Figure 8 has the same d.c. noise immunity as the DTL circuit because the same number of diode drops exist between the input logic pull-up resistor and ground. One must compare the individual circuits to ascertain their relative merits in a.c. noise immunity. Generally, a circuit containing high output drive capability and using an active pull-up as shown in Figure 6b will generate more supply and ground line noise than a circuit without the pull-up, since high current pulses are delivered from active pull-up outputs. In high speed systems, care must be exercised in by-passing all supplies so as to minimize the effects of this noise.

Current Mode

General Characteristics

Logic current is small and flows in or out of inputs, depending on circuit (high impedance input).

Outputs source and/or sink current (low impedance output).

Gates perform AND/OR functions (AND/OR may be inverted by common base stage to NAND/NOR).

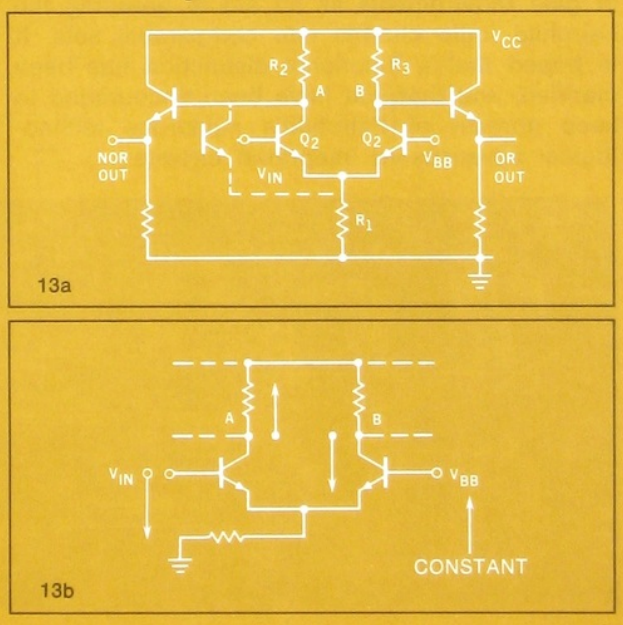
Fastest logic form - non-saturating.

Both Current "Sinking" and "Sourcing" were rather straightforward; Current Mode circuits are more difficult to categorize. There are, however, some identifying characteristics.

Figure 13a shows a Current Mode circuit. The peculiarity worth noting is emitter-coupled, non-saturating circuitry. The input portion of the circuit, Figure 13b, has been set apart for closer inspection; in this case, the input is differential. The arrows with a dot on the tail indicate the relative voltage variations of points A and B with respect to V_{IN}. More inputs may be provided by adding more transistors parallel to Q_2. Since point A drives an emitter-follower, the output is in phase with point A. Likewise, the OR output is in phase with point B.

The emitter-follower output enhances propagation time because it does not saturate, and therefore there is no delay due to storage time.

Figure 13. Current Mode Circuit Example



Fairchild CTμL is a form of Current Mode logic, but it has been specially designed for application in simple circuit board or open transmission systems. The CTL basic gate in Figure 14 has those characteristics thus far attributed to Current Mode circuits. It is non-saturating logic and uses emitter-followers.

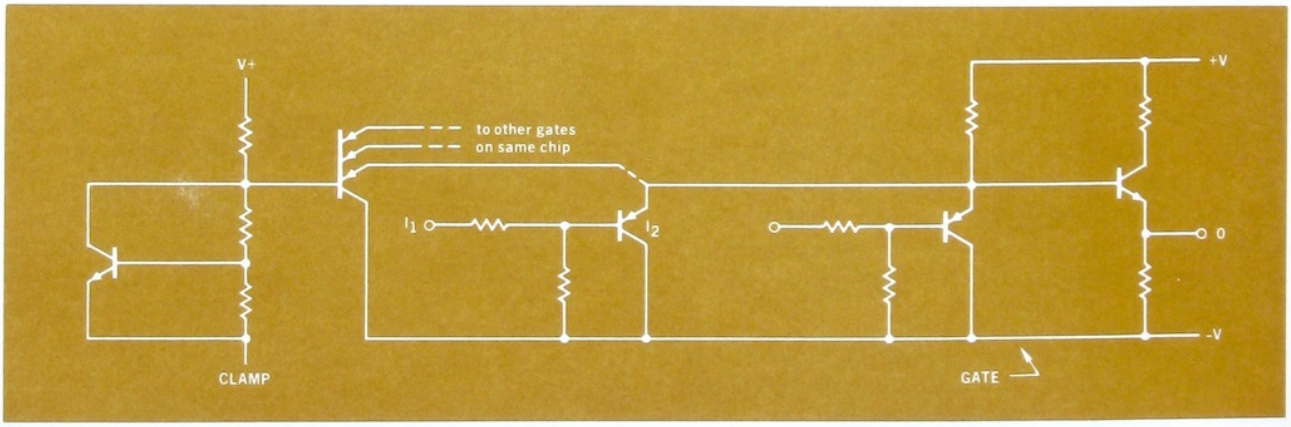
The inputs are PNP emitter-followers, biased so as to be "on" with no connection to their base. The inputs require low voltage, a current sink to drive the output to its low level, and a current source to make the output high.

The output of the CTL gate meets the requirements of the CTL inputs. When its inputs are high, the base of the NPN is high, the output is high, and the requirement of current sourcing is met. Conversely, with the inputs low, current sinking is provided.

One problem common to some forms of CML and CTL is "level shift". Since the voltage gain is less than, but nearly equal to one, the voltage extremes of the output are less than those of the input by a small amount. This means that after several decision levels, one must restore logic levels. This is done for CTL with the 9952 gates and the flip-flops, which use saturating inverter circuits.

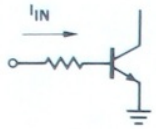
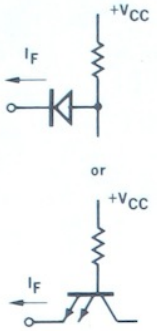
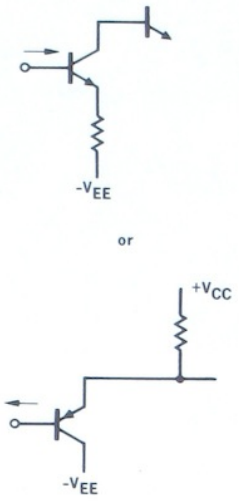
No mention of flip-flops has been made. The current classification has been presented on the basis of gate requirements as an aid to grouping the Fairchild logic circuits into comparable sets. It is hoped that a functional distinction has been clarified, and that you have been encouraged to keep abreast of Fairchild's numerous technological advances in integrated circuits.

Figure 14. CTL AND Gate

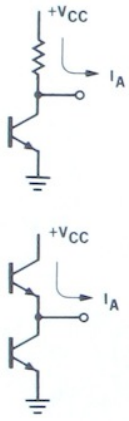
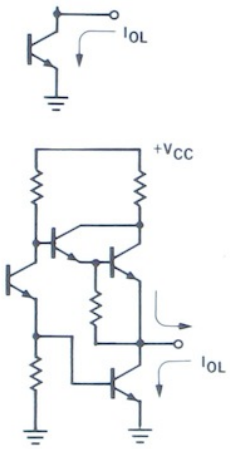


Input, Output Summary

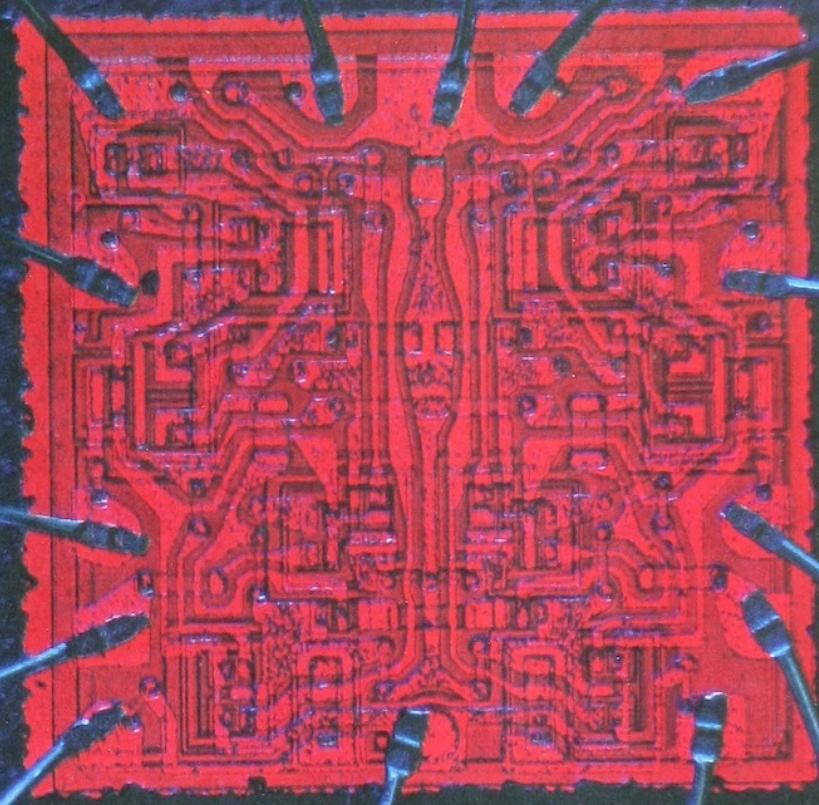
INPUTS:

CURRENT SOURCING	CURRENT SINKING	CURRENT MODE
		

OUTPUTS: Normal Pull-Up or Pull-Down

CURRENT SOURCING	CURRENT SINKING	CURRENT MODE
		

Current Sourcing Circuits



TOTAL CAPABILITY

RESISTOR-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

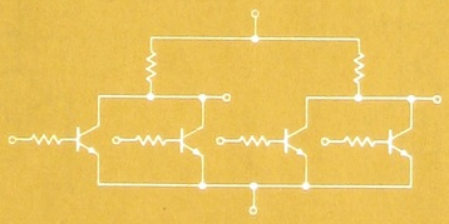
Fairchild Resistor-Transistor Micrologic® integrated circuits are a set of compatible integrated circuits manufactured by the patented Planar* epitaxial process. All the necessary transistors and resistors are diffused into a single silicon wafer, with individual RTμL gates interconnected by the patented metal-over-oxide process.

The RTμL family in itself can comprise the logic section of a computer. It features very low propagation delays, making it ideal for use in high-speed systems. Typical propagation delay for the basic RTμL circuit is 12 nanoseconds.

Fairchild RTμL elements are specifically designed to permit highly reliable data processing at the lowest cost per logic function.

Absolute Maximum Ratings
(25°C Free Air Temperature)

Maximum voltage applied to pin 8	+12.0 volts
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW



Basic Schematic

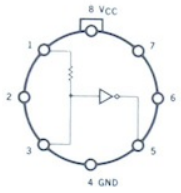
*Planar is a patented Fairchild Process

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9900	Buffer	300 mV	16 nsec	30 mW	25

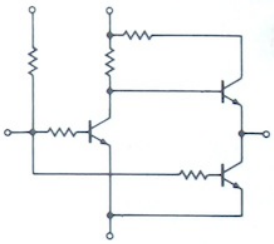
DESCRIPTION

Low impedance inverting driver circuit for use as a line driver, an astable or monostable multivibrator, or pulse differentiator. Valuable for driving heavily loaded circuits or minimizing rise-time deterioration due to capacitive loading.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5D)
3.6 volts ±10%	+15°C to + 55°C (28) 0°C to + 70°C (29)	Epoxy (8B)



Logic Diagram



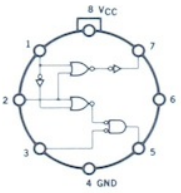
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9901	Counter Adapter	300 mV	24 nsec	55 mW	5

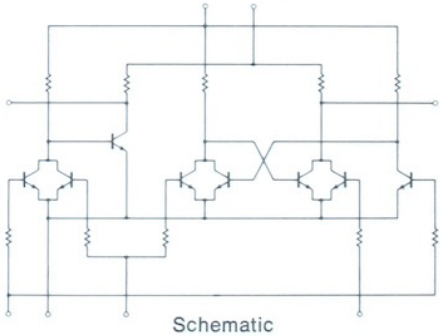
DESCRIPTION

Non-inverting gating unit composed of five basic RTμL circuits. Gives complementary outputs from a single-valued input. Power is supplied separately to the output nodes so that the outputs may be paralleled with other elements.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5B)



Logic Diagram



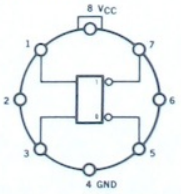
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9902	Flip-Flop	300 mV	14 nsec	22 mW	4

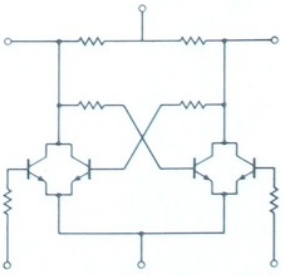
DESCRIPTION

Consists of two basic RTμL gate circuits internally cross-connected to form a bi-stable flip-flop storage unit. Since only a positive input can cause an internal change of state, the unit should be regarded as a NOR circuit. Input and output are provided externally for each of the gate circuits.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5D)



Logic Diagram



Schematic

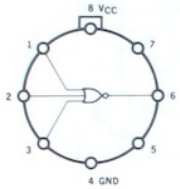
All numbers in parentheses refer to Product Code, explained fully on p. 83.

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9903	Three-Input Gate	300 mV	12 nsec	12 mW	5

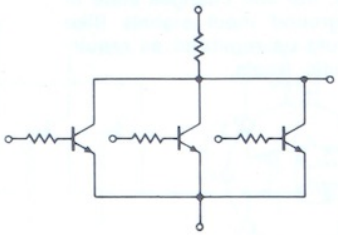
DESCRIPTION

Three-input gate for NAND/NOR functions. Permits the generation of any logic-function through the exclusive use of gate elements. Individual gate elements may be paralleled to increase the number of inputs to a single output node, or combined with other elements to augment their logic functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5C)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



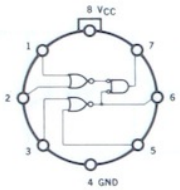
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9904	Half-Adder	300 mV	16 nsec	34 mW	5

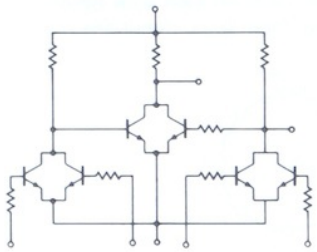
DESCRIPTION

Multi-purpose combination of three basic RTμL circuits as two-level AND/OR gate suitable for half-adder, exclusive OR, or other similar logic functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



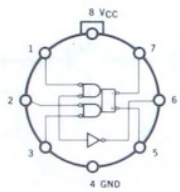
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9905	Half-Shift Register (with Inverter)	300 mV	18 nsec	53 mW	4

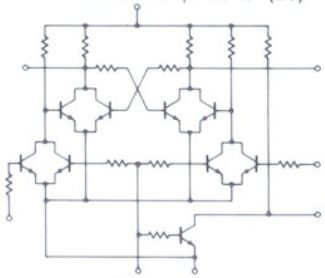
DESCRIPTION

Gated input storage element composed of five basic RTμL gate circuits. Internal cross-connection of the two output gate circuits provides memory. Should be regarded as requiring NAND input logic levels.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

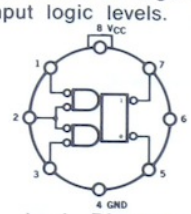
RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9906	Half-Shift Register (without Inverter)	300 mV	22 nsec	36 mW	4

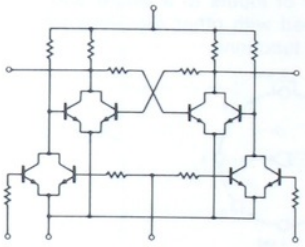
DESCRIPTION

Gated input storage element composed of four basic RTμL gate circuits. Internal cross-connection of the two output gate circuits provides memory. Because of two cascaded internal logic levels, the unit changes state in response to near-ground input signals (like the 9905), and should be regarded as requiring NAND input logic levels.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram

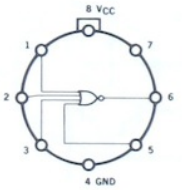

Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9907	Four-Input Gate	300 mV	12 nsec	12 mW	5

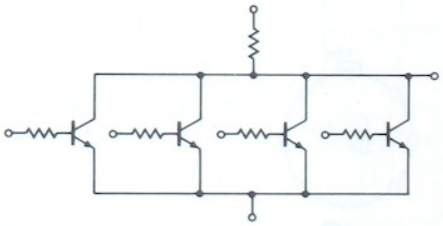
DESCRIPTION

Four-input gate for NAND/NOR functions. Permits the generation of any logic-function. Individual four-input gate elements may be paralleled to increase the number of inputs to a single output node, or combined with other elements to augment their logic functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram

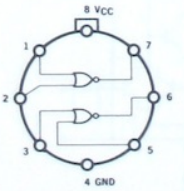

Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9914	Dual Two-Input Gate	300 mV	12 nsec	24 mW	5

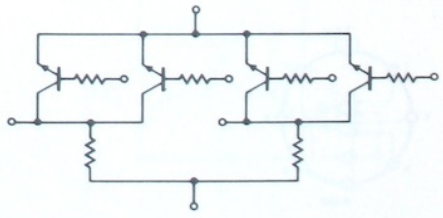
DESCRIPTION

Dual two-input gate capable of generating any logic function. Element circuits may be cross-connected to form a flip-flop, or connected in tandem to form non-inverting gates.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	
	+15°C to + 55°C (28)	Epoxy (8A)



Logic Diagram

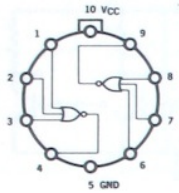

Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9915	Dual Three-Input Gate	300 mV	12 nsec	24 mW	5

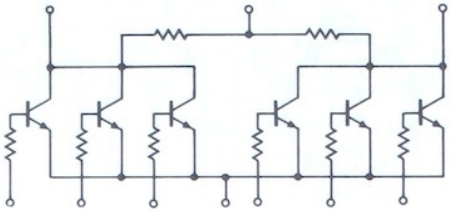
DESCRIPTION

Dual three-input gate capable of performing flip-flop and non-inverting gate functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

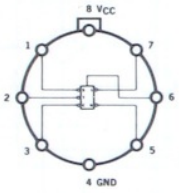
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9923	J-K Flip-Flop	300 mV	40 nsec	54 mW	3

DESCRIPTION

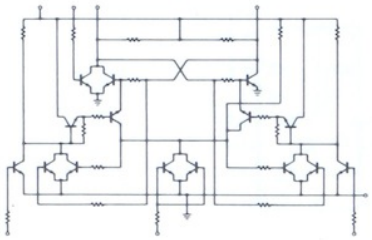
Complete general purpose storage element designed for use in industrial shift register and binary counting applications.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.6 volts ±10%	+15°C to + 55°C (29)	TO-5 (5B)
	+15°C to + 55°C (28)	Epoxy (8A)

Operation from −55°C to +125° can be obtained by use of a sliding voltage supply system (i.e., 4.2 volts at −55°C, 3.6 volts at 25°C, 2.6 volts at +125°C; ±10%)



Logic Diagram



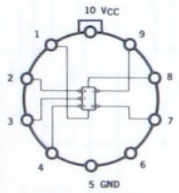
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9926	J-K Flip-Flop	300 mV	40 nsec	56 mW	5

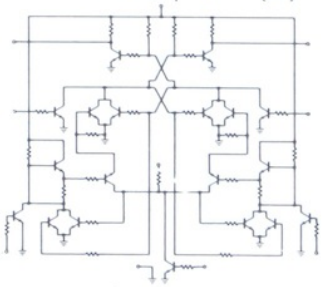
DESCRIPTION

Complete, general purpose storage element suitable for use in shift registers, counters, or any type of control function. Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5F)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

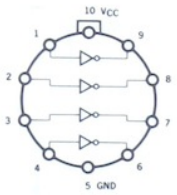
RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9927	Quad Inverter	300 mV	12 nsec	48 mW	5

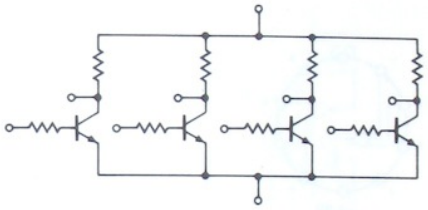
DESCRIPTION

Quad single-input inverter for multi-inversion functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
	0°C to +100°C (22)	TO-5 (5F)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



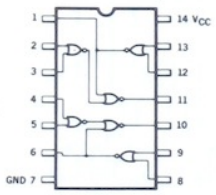
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9970	Dual Half-Adder	300 mV	16 nsec	34 mW/half-adder	5

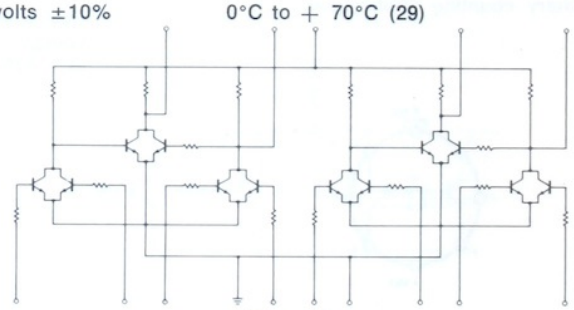
DESCRIPTION

Multi-purpose element suitable for half-adder, exclusive OR, and other similar logic constructions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3I)
	0°C to +100°C (22)	Dual In-Line (6A)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



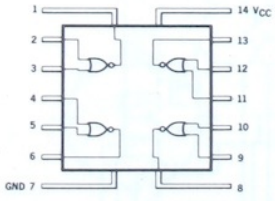
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9991	Quad Two-Input Gate	300 mV	12 nsec	12 mW/gate	5

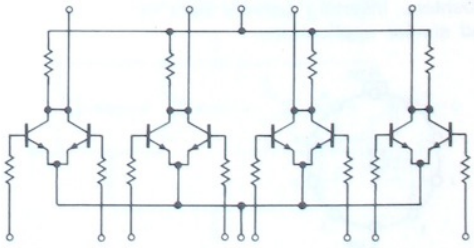
DESCRIPTION

Each of the four two-input gates performs the NAND/NOR functions with positive/negative logic.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3I)
	0°C to +100°C (22)	Dual In-Line (6A)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

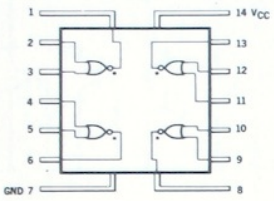
RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9992	Quad Two-Input Expander	300 mV	12 nsec	—	—0.5

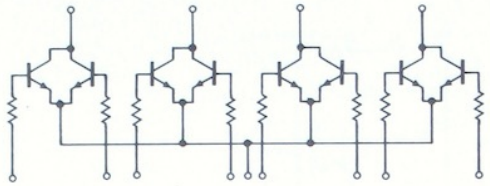
DESCRIPTION

Consists of four two-input gates without collector node resistors. Output terminal may be connected in parallel with any gate to increase fan-in capability. When used in conjunction with another gate, V_{CC} must also be connected to pin 14 of the expander.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat Pack (3I) Dual In-Line (6A)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



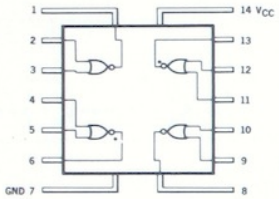
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9993	Dual Two-Input Gate and Dual Two-Input Expander	300 mV	12 nsec	12 mW/gate	5

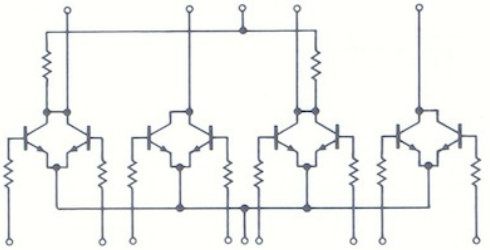
DESCRIPTION

Each gate performs the NAND/NOR functions with negative/positive logic. Each of the two-input expanders provides the additional versatility of paralleling inputs to any gate of the same circuit, making connection to V_{CC} pin of the expanders unnecessary.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21) 0°C to +100°C (22)	Flat-Pack (3I) Dual In-Line (6A)
3.6 volts ±10%	0°C to + 70°C (31)	



Logic Diagram



Schematic

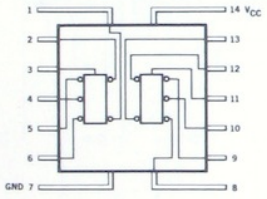
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9994	Dual J-K Flip-Flop	300 mV	40 nsec	54 mW/FF	3

DESCRIPTION

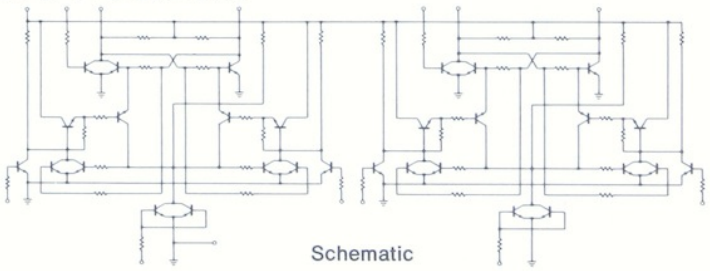
Complete general purpose storage element designed for use in industrial shift register and binary counting applications.

SUPPLY VOLTAGE	TEMPERATURE RANGE*	PACKAGE
3.6 volts ±10%	0°C to + 70°C (29)	Flat-Pack (3I) Dual In-Line (6A)

*Operation may be expanded to −55°C to +125°C by using a sliding scale power supply (i.e., 4.2 volts at −55°C, 3.5 volts at +25°C, 2.6 volts at +125°C; ±10%).



Logic Diagram



Schematic

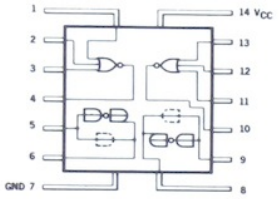
RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	DRIVE FACTOR
9995	Dual Buffer and Dual Three-Input Gate Expander	300 mV	12 nsec (gate) 16 nsec (buffer)	30 mW/buffer	5 (gate) 25 (buffer)

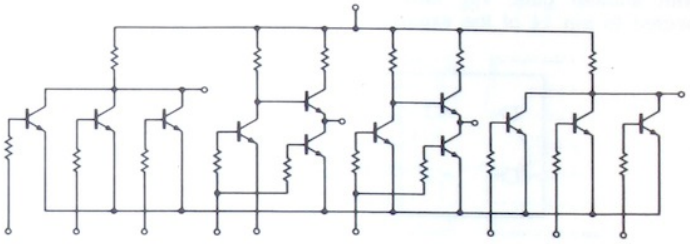
DESCRIPTION

Each of the three-input gates performs the NAND/NOR function with positive/negative logic. Each of the buffers is a low-impedance, inverting driver circuit which can supply substantially more output current than a standard RTμL gate.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C 0°C to +100°C	Flat-Pack Dual In-Line
3.6 volts ±10%	0°C to + 70°C	



Logic Diagram



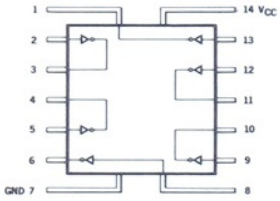
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9996	Hex Inverter	300 mV	12 nsec	12 mW/node	5

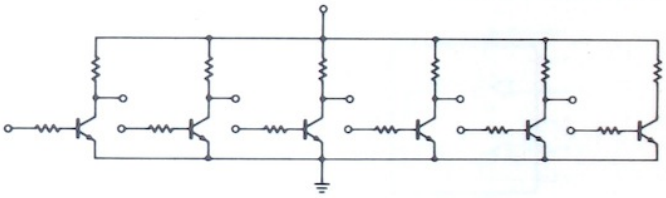
DESCRIPTION

Six-input RTμL inverter circuit designed for use in applications where complements of several signals are desired simultaneously.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C 0°C to +100°C	Flat Pack Dual In-Line
3.6 volts ±10%	0°C to + 70°C	



Logic Diagram



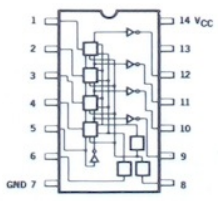
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9997	Four-Bit Shift Register	300 mV	45 nsec	220 mW	5

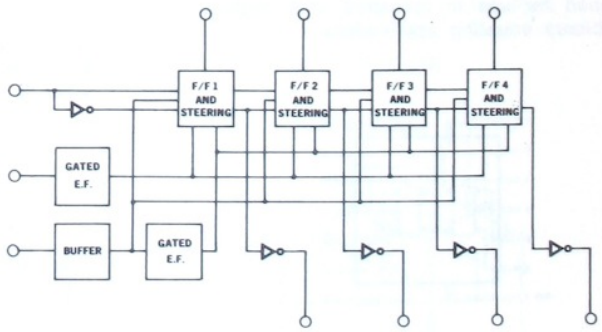
DESCRIPTION

Features serial and parallel inputs and outputs, and common reset with four single-ended outputs. Shifts on the falling edge of the pulse on the trigger input.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.5 volts to 5.5 volts ±10%	0°C to + 70°C	Dual In-Line



Logic Diagram



Schematic

TOTAL CAPABILITY

LOW POWER RESISTOR-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

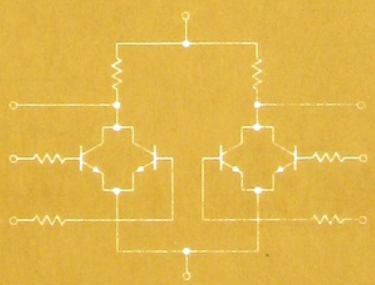
Fairchild Low Power Resistor-Transistor Micrologic® integrated circuits (formerly Milliwatt Micrologic®) are a compatible set of integrated logic building blocks. As with the standard RTμL family, all the necessary transistors and resistors are diffused into a single silicon wafer by the patented Planar* process, with individual RTμL gates inter-connected by the patented metal-over-oxide technique.

Low Power RTμL features very low propagation delays at low DC power dissipation. Typical propagation delay for the basic circuit is 40 nanoseconds; power dissipation is 2 mW.

These low power elements may be used through the full military temperature range of −55°C to +125°C.

Absolute Maximum Ratings (25°C Free Air Temperature)

Maximum voltage applied to pin 8 (continuous)	8 volts
Maximum voltage applied to pin 8 (pulsed $\leq$ 1 second)	12 volts
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +150°C
Power Dissipation	250 mW



Basic Schematic

*Planar is a patented Fairchild Process

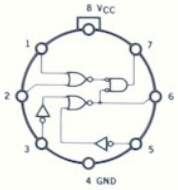
LOW POWER RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9908	Adder	300 mV	70 nsec	10 mW	4

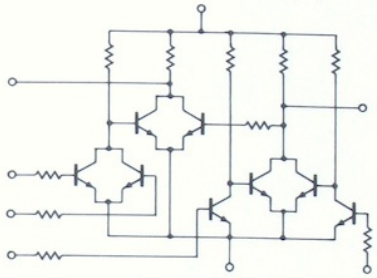
DESCRIPTION

Performs Mod 2 addition, or exclusive OR function, and is used to select one of two data streams under control of a single gate signal.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
		TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



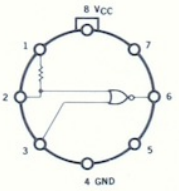
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9909	Buffer	300 mV	70 nsec	10 mW	30

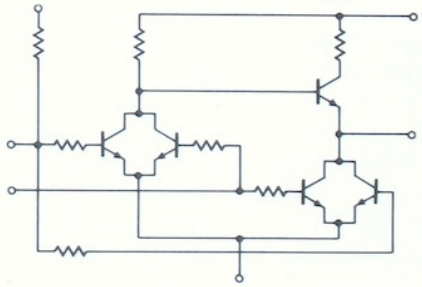
DESCRIPTION

Two-input, low impedance inverting driver circuit. Can supply more output current than the basic RTμL circuit. For use as a line driver, astable or monostable multivibrator, or pulse differentiator.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
		TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



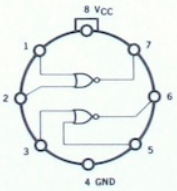
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9910	Dual Gate	300 mV	35 nsec	4 mW	4

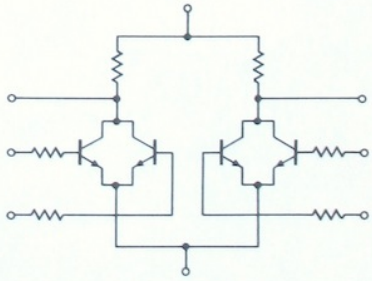
DESCRIPTION

Dual two-input gate for use as a pair of NOR gates, as an R-S flip-flop, as a pair of inverters, or as a double inverter. It may also be used with the 9921 Gate Expander to increase its fan-in capacity.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F)
		TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

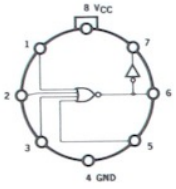
LOW POWER RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9911	Gate	300 mV	65 nsec	4 mW	4

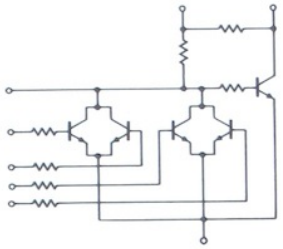
DESCRIPTION

Four-input gate for OR, NOR, AND or NAND gate functions. Fan-in capacity can be increased by use with the 9921 Gate Expander.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



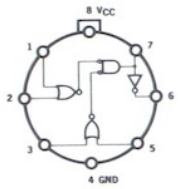
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9912	Half-Adder	300 mV	70 nsec	8 mW	4

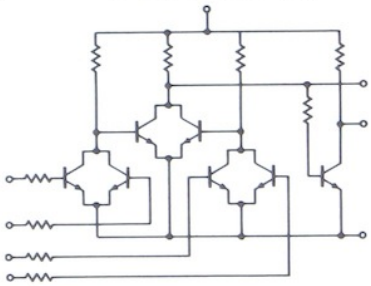
DESCRIPTION

Two-level AND-OR gate with added output inverter for use as complete half-adder, exclusive OR gate, or any similar logic construction.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



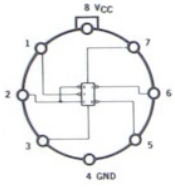
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9913	Type D Flip-Flop	300 mV	70 nsec	12 mW	3

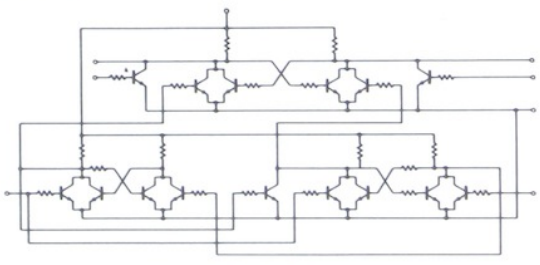
DESCRIPTION

Complete, general purpose gated storage element suitable for shift registers, counters, and control circuitry.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



Schematic

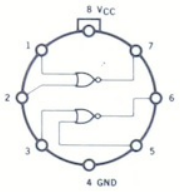
LOW POWER RESISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9921	Gate Expander	300 mV	35 nsec	–	–

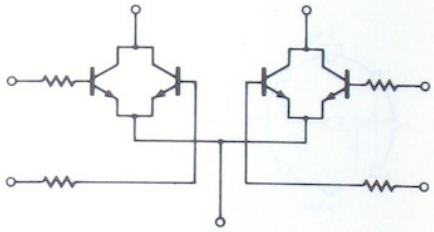
DESCRIPTION

Dual two-input gate without resistors, used to increase fan-in capability of gate circuits.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C (21)	Flat-Pack (3F) TO-5 (5B)
3.6 volts ±10%	0°C to + 70°C (29)	



Logic Diagram



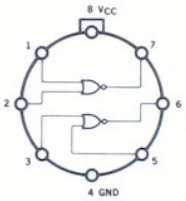
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9938	Dual Buffer	300 mV	70 nsec	20 mW	30/buffer

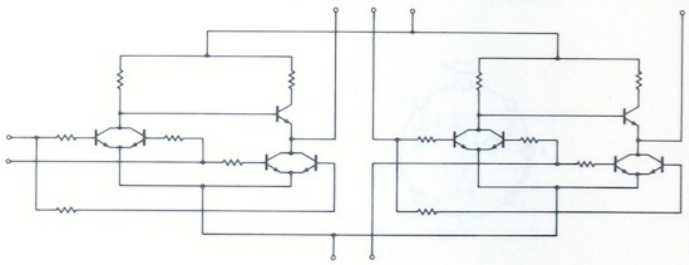
DESCRIPTION

Dual two-input low-impedance inverting driver circuit. Can supply more output current than the basic RTμL circuit, for use as a line driver, astable or monostable multivibrator, or pulse differentiator.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C	Flat Pack TO-5
3.6 volts ±10%	0°C to + 70°C	



Logic Diagram



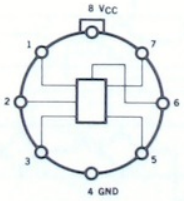
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9940	J-K Flip-Flop	300 mV	80 nsec	12 mW	3

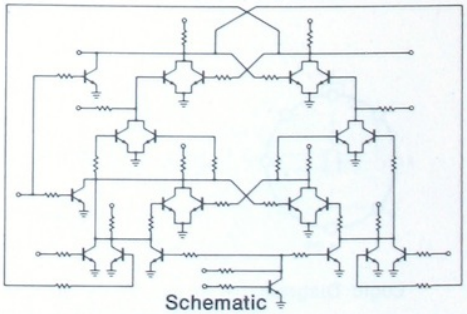
DESCRIPTION

Complete, general purpose storage element suitable for use in shift registers, counters, or binary control functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C	Flat Pack TO-5
3.6 volts ±10%	0°C to + 70°C	



Logic Diagram



Schematic

TOTAL CAPABILITY

COUNTING MICROLOGIC®

INTEGRATED CIRCUITS

Fairchild Counting Micrologic® integrated circuits are a compatible family of integrated circuits designed for various types of counting and allied applications.

The CμL family compresses all of the circuit components of a printed circuit card into the space formerly occupied by a single transistor. Functionally, however, it is equivalent to four flip-flops and at least one logic gate. Counting microcircuits offer the advantages of reliability, small size, and low power consumption at prices that are difficult to meet with discrete components and impossible with other integrated circuit approaches.

The 9958 and 9989 are both complete counters in themselves; the other members of the family provide storage and decoding capabilities.

Absolute Maximum Ratings (25°C Free Air Temperature)

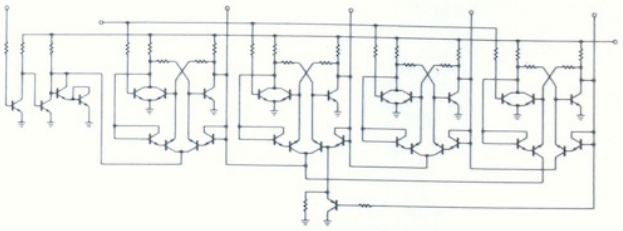
Maximum voltage at pin 7 (0°C to +75°C)	+6.0 volts
Count Input Pin Voltage	+4.0 volts, −2.0 volts
Reset Input Pin Voltage	+4.0 volts, −2.0 volts
Current into Each Output Terminal	±5.0 mA
Storage Temperature	−55°C to +150°C

PART NUMBER	ELEMENT TYPE	DESCRIPTION
9958	Decade Counter	Complete decade counter consisting of four cascaded binary-triggered flip-flops modified by a feedback loop to count in the familiar 8-4-2-1 code. Provision is made for clearing and presetting any one of the possible decimal states.

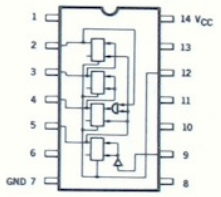
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature)

	Minimum	Maximum
Count Input - Low		0.45 V
Count Input - High	1.2 V	
Count Input Pulse Width - High	150 nsec	
Count Input Slope - Positive Going		1.0 V/μsec
Maximum Count Input Frequency		2.0 MHz
Reset Input - Low		0.45 V
Reset Input - High	1.2 V	
Output - Low		0.35 V
Output - High	1.4 V	

Power Consumption	140 mW at 4.0 V
Supply Voltage	3.3 volts to 5.5 volts
Temperature Range	0°C to +75°C (59)
Package	TO-5 (5B) Dual In-Line (6A)



Schematic



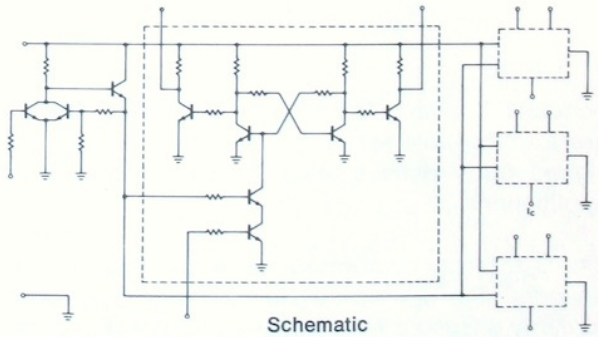
Logic Diagram

PART NUMBER	ELEMENT TYPE	DESCRIPTION
9959	Buffer Storage	Consists of four gated-latch circuits and a common gate driver. Information present at the four data inputs enters the latches throughout the interval of a load command applied to the gate input terminal. With gate high, information is stored until a subsequent load command permits a change.

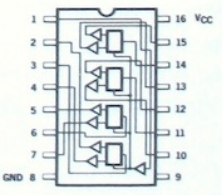
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature)

	Minimum	Maximum
Input High	1.0 V	
Input Low		0.5 V
Output Low		0.4 V
Sampling Pulse Width	100 nsec	

Information Rate	5.0 MHz
Through Delay	60 nsec
Power Consumption	140 mW at 4.0 V
Supply Voltage	3.3 volts to 5.5 volts
Temperature Range	−55°C to +125°C, V_{CC} = 4.0 volts to 4.4 volts
Package	Dual In-Line (6B)



Schematic



Logic Diagram

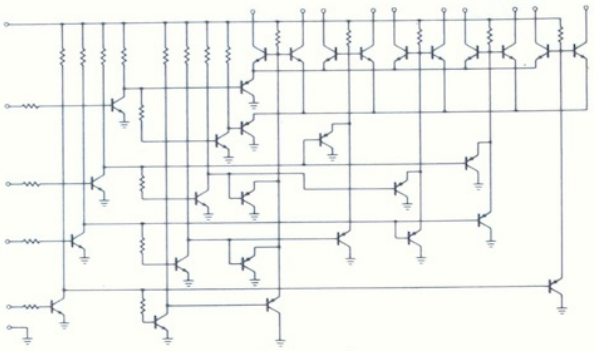
COUNTING MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	DESCRIPTION
9960	Decimal Decoder/Driver	Accepts 1-2-4-8 binary coded decimal inputs at integrated circuit signal levels and produces ten mutually exclusive outputs to control a nixie tube. Only true values are accepted as inputs to simplify connection with counters or other sources.

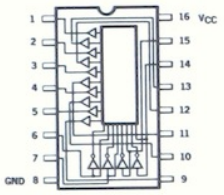
ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature)

	Minimum	Maximum
Input High	1.0 V	
Input Low		0.4 V
ON Output Voltage		4.0 V
OFF Output Voltage	55.0 V	
Power Consumption	35 mW at 4.0 V	
Supply Voltage	3.3 volts to 5.5 volts	
Temperature Range	−55°C, $V_{CC} = 4.0$ V*	
Package	Dual In-Line (6B)	

*High temperature on request



Schematic

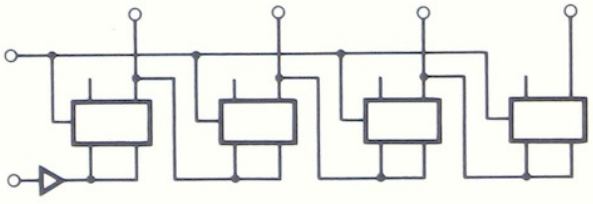


Logic Diagram

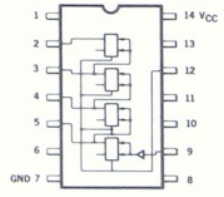
PART NUMBER	ELEMENT TYPE	DESCRIPTION
9989	Mod 16 Counter	Complete Mod 16 counter consisting of four cascaded binary-triggered flip-flops. Counts in the familiar 8-4-2-1 code. Provision is made for clearing and presetting any one of the possible states.

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature)

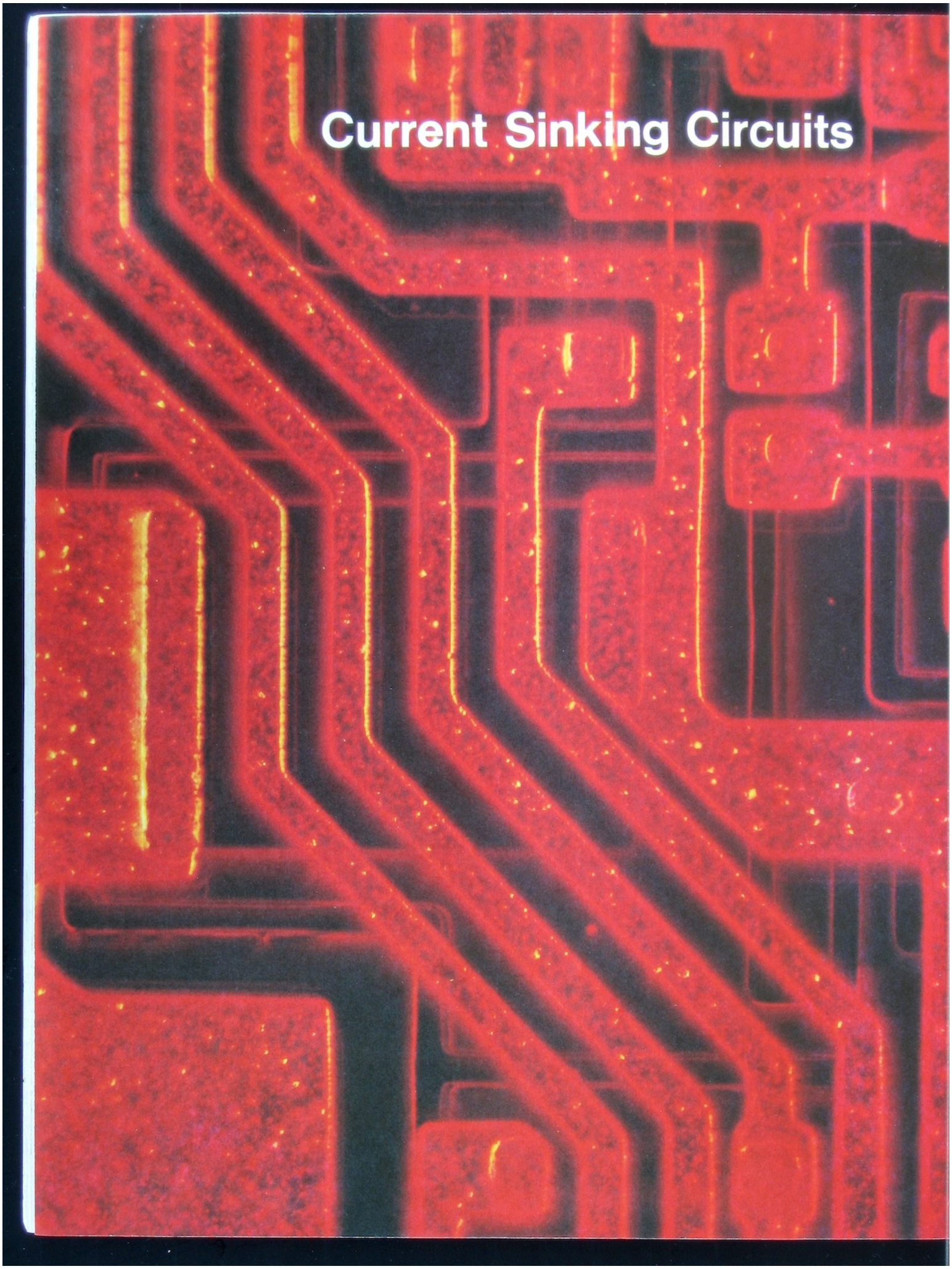
	Minimum	Maximum
Count Input - Low		0.45 V
Count Input - High	1.2 V	
Count Input Pulse Width - High	45 nsec	
Count Input Slope - Positive Going		1.0 V/μsec
Maximum Count Input Frequency		15 MHz
Reset Input - Low		0.45 V
Reset Input - High	1.2 V	
Output - Low		0.35 V
Output - High	1.4 V	
Power Consumption	140 mW at 4.0 V	
Supply Voltage	3.6 volts to 5.5 volts	
Temperature Range	0°C to +75°C (59)	
Package	TO-5 (5B) Dual In-Line (6A)	



Schematic



Logic Diagram


Current Sinking Circuits

TOTAL CAPABILITY

TRANSISTOR-TRANSISTOR MICROLOGIC®

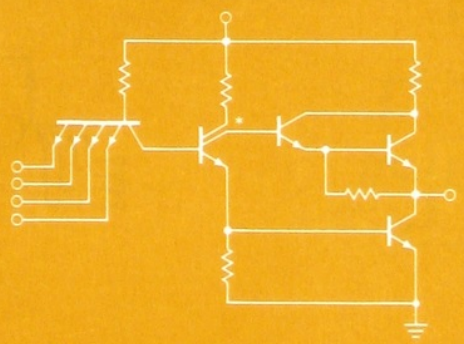
INTEGRATED CIRCUITS

Fairchild Transistor-Transistor Micrologic® integrated circuits are high-level positive NAND gates capable of driving high capacitance and high fan-out loads over the −55° to +125°C temperature range. They are designed for compatibility with DTμL elements.

Transistor-Transistor Micrologic® IC's feature low typical propagation delays of 6 nanoseconds with 15 pf load capacitance and high and low fan-out. Typical propagation delay at 600 pf load capacitance and a fan-out of 15 is less than 50 nanoseconds from −55°C to +125°C. The difference between logic levels at any combination of temperature and fan-out is typically greater than 2.8 volts with a power supply of 5.0 volts ±10%. Pin outline is compatible with the Fairchild DTμL 9930 series in both flat pack and Dual In-Line.

Absolute Maximum Ratings
(25°C Free Air Temperature)

Input Voltage	+5.5 volts DC
Output Voltage	+5.5 volts DC
Input Current	±10 mA
Output Current	±60 mA
Storage Temperature	−65°C to +125°C



Basic Schematic

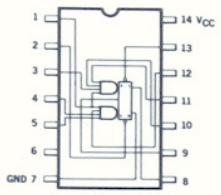
TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9000	J-K Flip-Flop	"1" Level: 3.0 V "0" Level: 0.4 V	25 nsec	45 mW	10

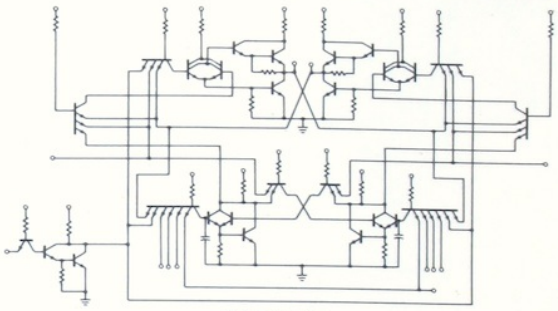
DESCRIPTION

Positive edge, clock-gated flip-flop suitable for all general control logic, register, and counting applications. Incorporates 3 J and 3 K inputs, and a JK input.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



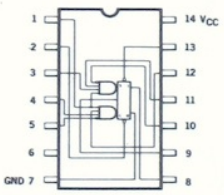
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9001	J-K Flip-Flop	"1" Level: 3.0 V "0" Level: 0.4 V	25 nsec	45 mW	10

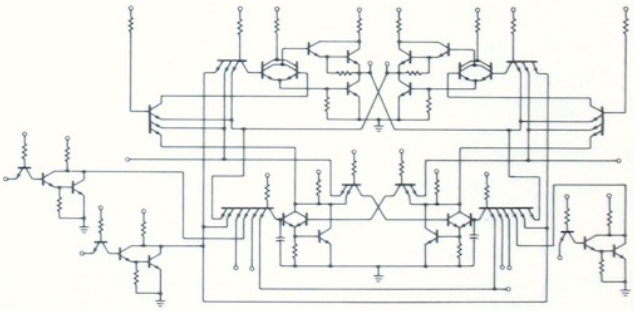
DESCRIPTION

Clock-gated flip-flop, positive edge, designed for general control logic, register, and counting applications. Features 2 J and 2 K, 1 $\overline{J}$ and 1 $\overline{K}$ inputs, and a JK input.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



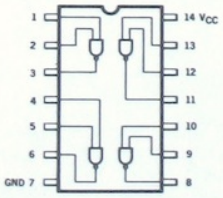
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9002	Quad Gate	"1" Level: 3.0 V "0" Level: 0.4 V	10 nsec	12 mW	12

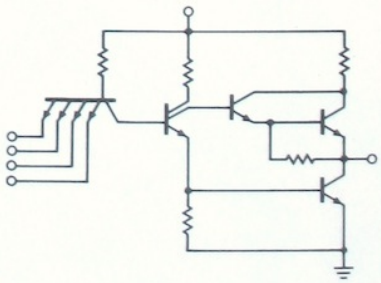
DESCRIPTION

Quad two-input gate for inversion, exclusive OR, and other general logic functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



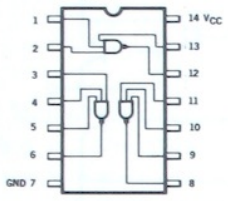
Schematic

All numbers in parentheses refer to Product Code, explained fully on p. 83.

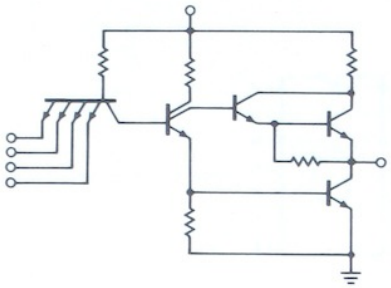
TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9003	Triple Gate	"1" Level: 3.0 V "0" Level: 0.4 V	10 nsec	12 mW	12

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Triple three-input gate for inversion, exclusive OR, and other general logic functions.	5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



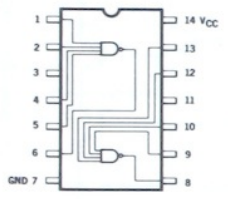
Logic Diagram



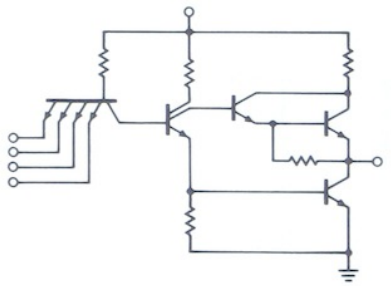
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9004	Dual Gate	"1" Level: 3.0 V "0" Level: 0.4 V	10 nsec	12 mW	12

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Dual four-input gate for general high fan-in functions.	5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



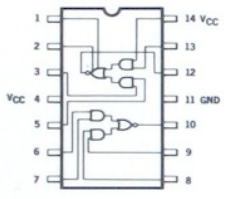
Logic Diagram



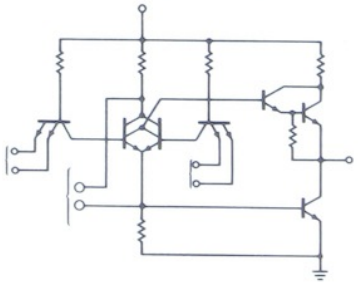
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9005	Dual Gate	1 volt	12 nsec	12 mW	12

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Expandable dual AND/OR/NOT gate for use as exclusive OR.	5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram

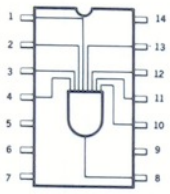


Schematic

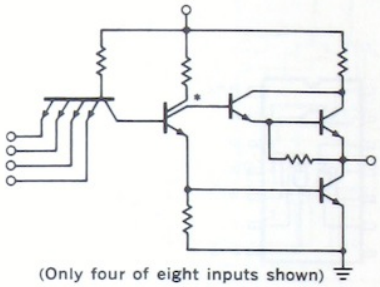
TRANSISTOR-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9007	Gate	"1" Level: 1.5 V "0" Level: 0.4 V	10 nsec	12 mW	12

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Eight-input gate for high fan-in functions.	5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram

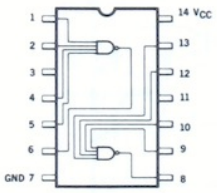


(Only four of eight inputs shown)

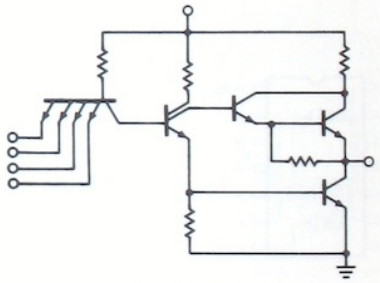
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9009	Dual Buffer	"1" Level: 1.5 V "0" Level: 0.4 V	15 nsec	22 mW	30

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Dual four-input buffer for high-speed, high-capacitance loading.	5.0 volts ±10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



Schematic

TOTAL CAPABILITY

DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

Fairchild Diode-Transistor Micrologic® integrated circuits are a compatible family designed specifically for integrated circuit technology. The elements are all of Planar* epitaxial construction.

Diode-Transistor Micrologic® integrated circuits feature low power dissipation, operation over a wide range of supply voltages, high fan-out capability, and high worst-case noise immunity.

DTμL circuits are specified over the full military range of −55°C to +125°C, and the limited temperature range of 0°C to +75°C.

Absolute Maximum Ratings (25°C Free Air Temperature)

Supply Voltage (continuous)	+8 volts
Supply Voltage (pulsed, <1 second)	+12 volts
Input Forward Current	−10 mA
Input Reverse Current	1 mA
Output current, into outputs (all gates)	30 mA
Output Current, into outputs (buffer and power gate)	100 mA
Storage Temperature	−65°C to +125°C

DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9930	Dual Gate	1 volt	25 nsec	8 mW	8

DESCRIPTION

Dual four-input gate for high fan-in gating (with input extension available in each gate).

SUPPLY VOLTAGE

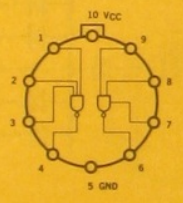
5.0 volts ± 10%

TEMPERATURE RANGE

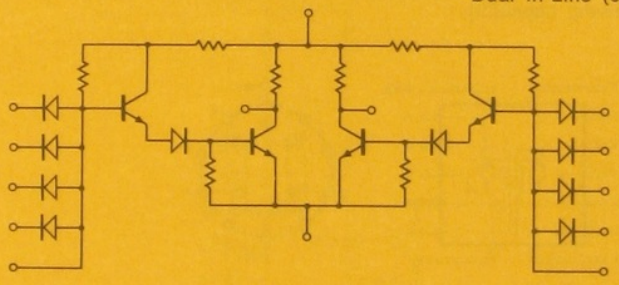
−55°C to +125°C (51)
0°C to + 75°C (59)

PACKAGE

Flat Pack (3I)
TO-5 (5F)
Dual In-Line (6A)



Logic Diagram



Schematic

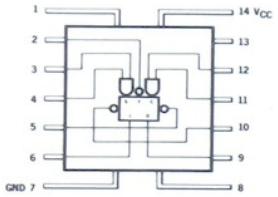
*Planar is a patented Fairchild Process

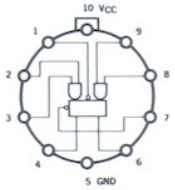
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9931	Clocked Flip-Flop	1 volt	50 nsec	20 mW	7

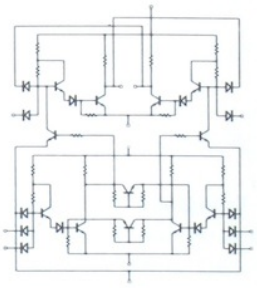
DESCRIPTION

R-S or J-K clock-gated flip-flop for storage functions. Consists of two flip-flop connected as a "master-slave" combination, thereby eliminating the need for capacitors or other circuit delay elements. The "master" stores the input information when the clock voltage is high and transfers it to the "slave" when the clock voltage is low. Has direct set and clear inputs.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)







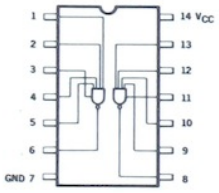
Schematic

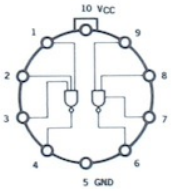
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9932	Dual Buffer	1 volt	35 nsec	35 mW	25

DESCRIPTION

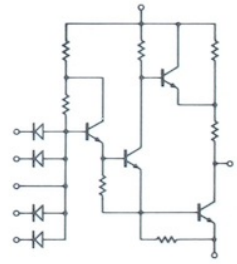
Dual four-input buffer with emitter-follower output pull-up to provide a high fan-out device with superior capacitance-driving capability. Input extension available in each buffer.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)





Logic Diagram



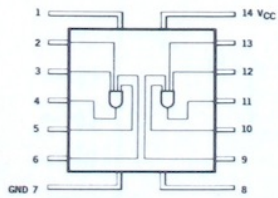
Schematic

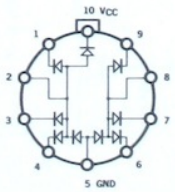
PART NUMBER	ELEMENT TYPE
9933	Dual-Input Extender

DESCRIPTION

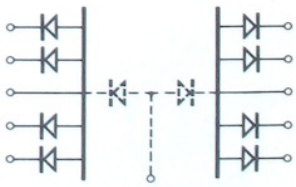
Dual four-input diode array used to increase fan-in capability to more than 20 without adversely affecting noise immunity or load-driving capability.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)





Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9936	Hex Inverter	1 volt	25 nsec	48 mW	8

DESCRIPTION

Consists of six DTμL inverters. Outputs may be tied together for the "wired OR" function.

SUPPLY VOLTAGE

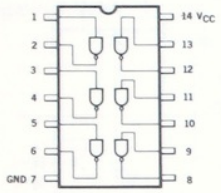
5.0 volts ± 10%

TEMPERATURE RANGE

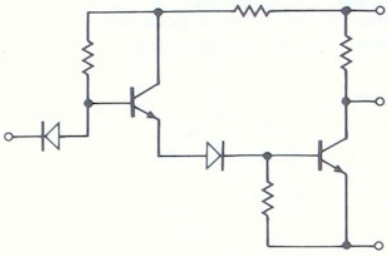
−55°C to +125°C (51)
0°C to + 75°C (59)

PACKAGE

Flat Pack (3I)
Dual In-Line (6A)



Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9937	Hex Inverter	1 volt	20 nsec	72 mW	5

DESCRIPTION

Consists of six DTμL inverters. Identical to the DTμL 9936 except for 2K pull-up resistors to improve switching times.

SUPPLY VOLTAGE

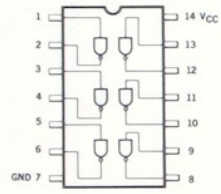
5.0 volts ± 10%

TEMPERATURE RANGE

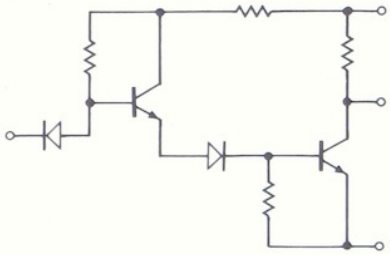
−55°C to +125°C (51)
0°C to + 75°C (59)

PACKAGE

Flat Pack (3I)
Dual In-Line (6A)



Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9944	Dual Power Gate	1 volt	40 nsec	20 mW	27

DESCRIPTION

Dual four-input power gate for use as a high fan-out gate interface driver or low-power lamp driver. Outputs may be tied together for the "wired OR" function, or may drive inputs with logic thresholds of 4 to 6 volts.
Input extension available on each gate.

SUPPLY VOLTAGE

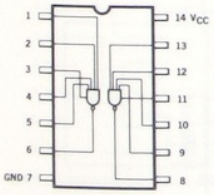
5.0 volts ± 10%

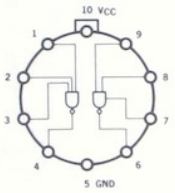
TEMPERATURE RANGE

−55°C to +125°C (51)
0°C to + 75°C (59)

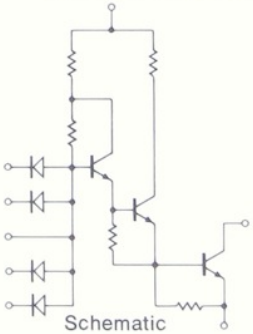
PACKAGE

Flat Pack (3I)
TO-5 (5F)
Dual In-Line (6A)





Logic Diagram



Schematic

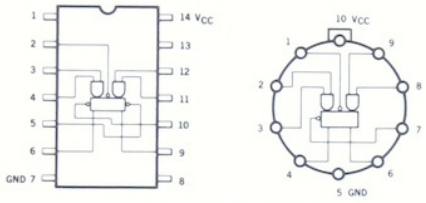
DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9945	Clocked Flip-Flop	1 volt	50 nsec	42 mW	9

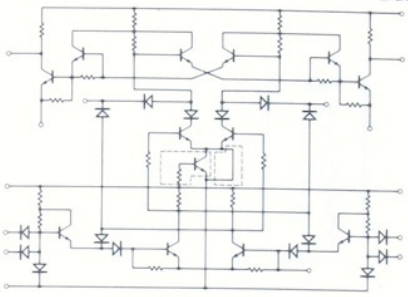
DESCRIPTION

R-S or J-K clock-gated flip-flop suitable for ripple-through counters. Operates on the "master-slave" principle. Information enters "master" when Trigger input voltage is high, and transfers to the "slave" when it goes low. Direct set and clear inputs are provided.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



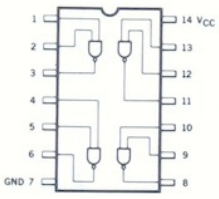
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9946	Quad Gate	1 volt	25 nsec	32 mW	9

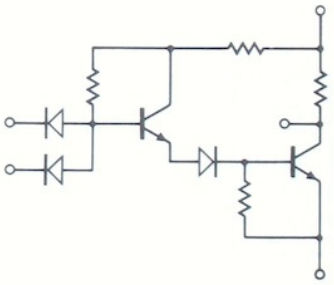
DESCRIPTION

Quad two-input gate for inverter, exclusive OR, and fan-in functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



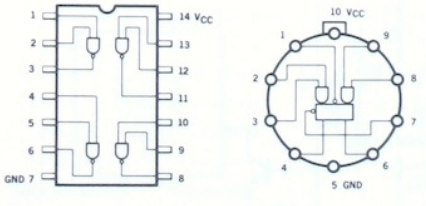
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9948	Clocked Flip-Flop	1 volt	40 nsec	48 mW	8

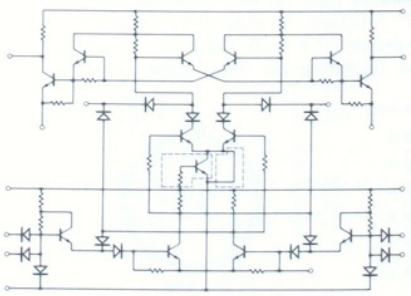
DESCRIPTION

R-S or J-K clock-gated "master-slave" flip-flop for use in shift registers, counters, and memory circuits, suitable for clock frequencies up to 8 MHz. Direct set and clear inputs are provided.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



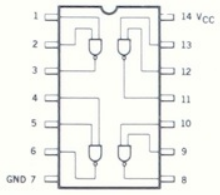
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9949	Quad Gate	1 volt	20 nsec	48 mW	5

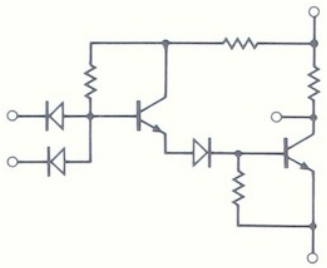
DESCRIPTION

Quad two-input gate for inverter, exclusive OR, and fan-in functions. Identical to the DTμL 9946 except for the use of a 2 KΩ pull-up resistor rather than the standard 6 KΩ resistor in other DTμL elements. Reduction in pull-up resistance improves turn-off time, yielding lower propagation delay.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



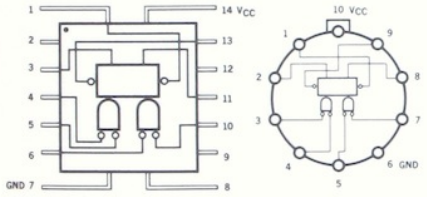
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9950	Pulse-Triggered Binary	1 volt	20 nsec	50 mW	10

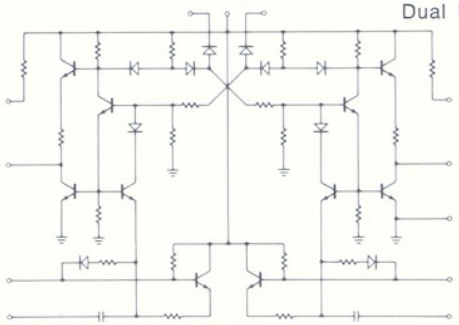
DESCRIPTION

High-speed gated flip-flop which may be used in any application requiring an R-S flip-flop or counter stage. Suited for present ripple-carry counters and similar pulse-triggered applications.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



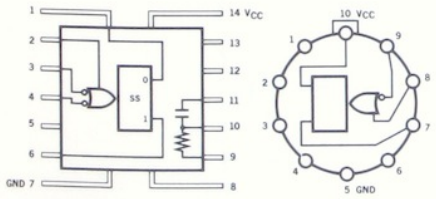
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9951	Monostable Multivibrator	1 volt	25 nsec	35 mW	10

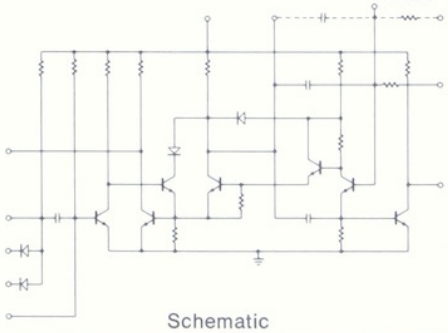
DESCRIPTION

Two-input monostable multivibrator useful as a variable delay pulse generator, and as a stable multivibrator. Provides complementary output pulses typically 100 nsec wide, or adjustable by the addition of external discrete passive components.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



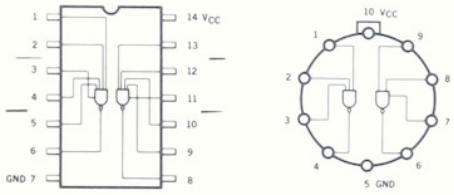
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9961	Dual Gate	1 volt	20 nsec	24 mW	5

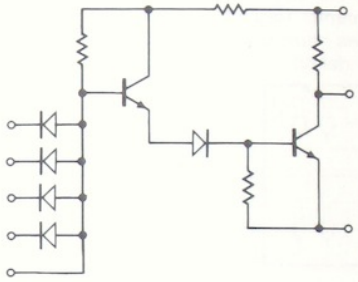
DESCRIPTION

Dual four-input gate (with extender) for high fan-in gating. Same as DTμL 9930 except for 2 KΩ pull-up resistor rather than 6 KΩ. Features improved turn-off time and lower propagation delay.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



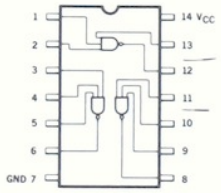
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9962	Triple Gate	1 volt	25 nsec	24 mW	8

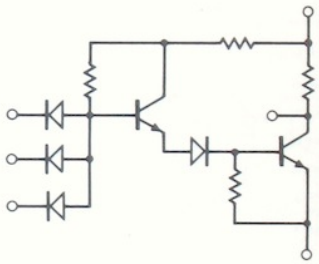
DESCRIPTION

Triple three-input NAND/NOR gate for inverting, exclusive OR, and fan-in functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



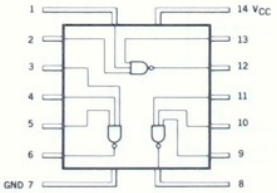
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9963	Triple Gate	1 volt	20 nsec	36 mW	5

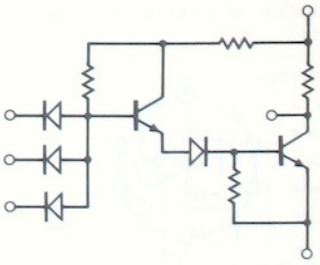
DESCRIPTION

Triple three-input NAND/NOR gate for inverting, exclusive OR, and fan-in functions. Similar to DTμL 9962, but uses 2 KΩ rather than 6 KΩ pull-up resistor, yielding improved turn-off time and lower propagation delay.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ± 10%	−55°C to +125°C (51) 0°C to + 75°C (59)	Flat Pack (3I) TO-5 (5F) Dual In-Line (6A)



Logic Diagram



Schematic

TOTAL CAPABILITY

LOW POWER DIODE-TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

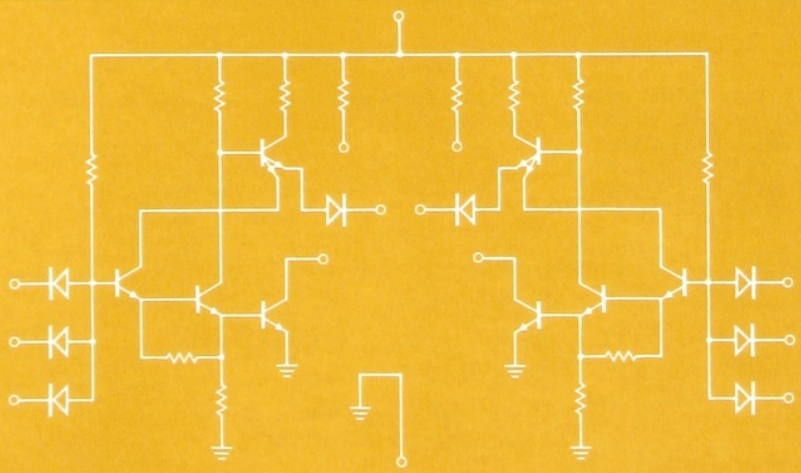
Fairchild Low Power Diode-Transistor Micrologic® integrated circuits comprise a set of compatible integrated circuits specifically designed for low-power, medium speed applications.

Important features of the Low Power Diode-Transistor Micrologic® family include typical power drains of less than 1 mW per gate, guaranteed minimum of 450 mV noise immunity, typical logic gate propagation delays of 60 nanoseconds and binary clock rate of 2.5 MHz.

LPDTμL elements provide reliable operation over the entire military temperature range of −55°C to +125°C.

Absolute Maximum Ratings (25°C Free Air Temperature)

Supply Voltage	**8.0 volts**
Current into Outputs	**15 mA**
Input Forward Current	**−1 mA**
Storage Temperature	**−65°C to +125°C**



Basic Schematic

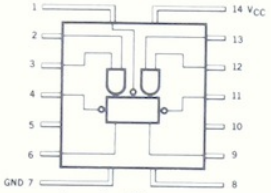
LOW POWER DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9040	Clocked Flip-Flop	1 volt	180 nsec (output going positive) 90 nsec (output going negative)	4 mW	10

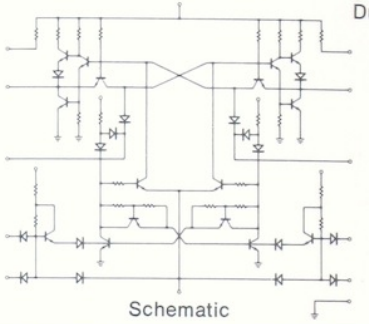
DESCRIPTION

Directly coupled, dual-rank flip-flop suitable for use in counters, shift registers, and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



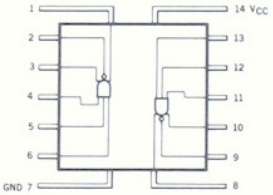
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9041	Dual NAND Gate	1 volt	65 nsec	2 mW	10

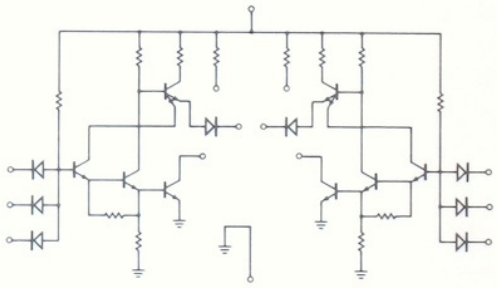
DESCRIPTION

Dual three-input positive logic NAND gates suitable for general logic gate and inverter applications. Collectors can be tied to a common node for the wired "OR" logic function, as output transistor collector and emitter follower pull-up are not internally connected.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



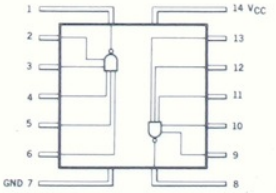
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9042	Dual NAND Gate	1 volt	65 nsec	2 mW	10

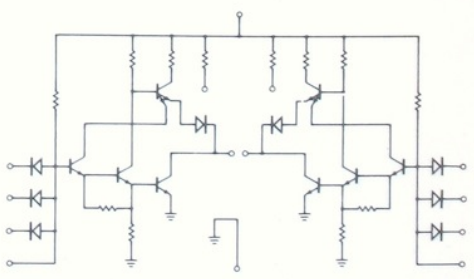
DESCRIPTION

Dual three-input positive logic NAND gate with extender inputs. May be used in conjunction with the DTμL9933 to expand fan-in capability. Allows implementation of logic applications requiring a gate fan-in exceeding three.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3I) Dual In-Line (6A)



Logic Diagram



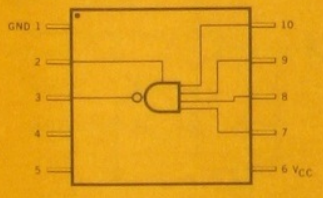
Schematic

ADDITIONAL CURRENT SINKING CIRCUITS

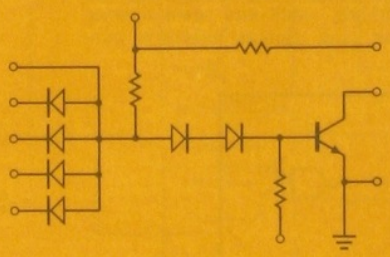
ADDITIONAL CURRENT SINKING CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE101 (5502)	NAND/NOR Gate	1 volt	30 nsec	6 mW	5

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Single four-input NAND/NOR gate capable of operating at high speed with low power consumption. Operates from a single power supply.	4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



Schematic

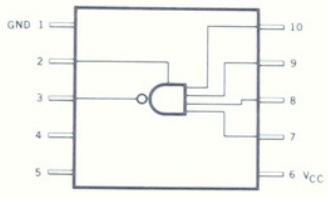
ADDITIONAL CURRENT SINKING CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE102 (5502)	NAND/NOR Gate	1 volt	30 nsec	6 mW	5

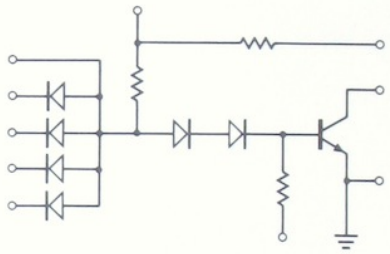
DESCRIPTION

Single three-input NAND/NOR gate for high-speed operation with low power consumption from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



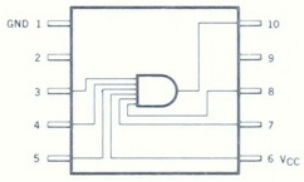
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE105 (5507)	Diode Array	—	—	—	—

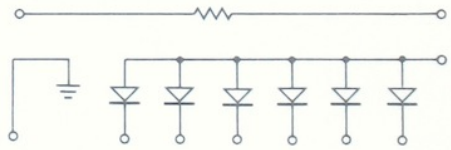
DESCRIPTION

Six-diode array for use in low-power, high-speed digital systems. Operates from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
—	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



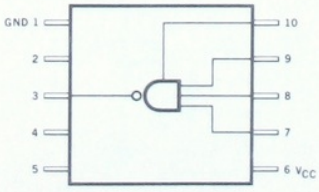
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE110 (5509)	Power Gate	1 volt	40 nsec	40 mW	20

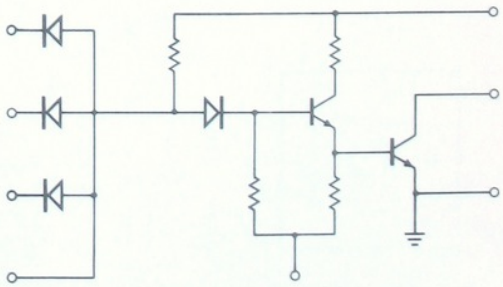
DESCRIPTION

Three-input power gate designed to operate from a single power supply. Well-adapted to high current and capacitive loads. Applications include driving clock and reset busses, terminated lines, and similar interface connections.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



Schematic

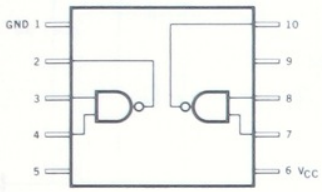
ADDITIONAL CURRENT SINKING CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE115 (5504)	NAND/NOR Gate	1 volt	30 nsec	15 mW	5

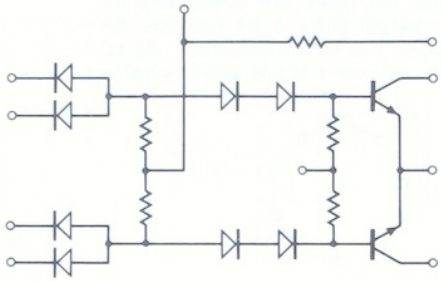
DESCRIPTION

Dual two-input NAND/NOR gate operating from a single power supply at high speed with low power consumption.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



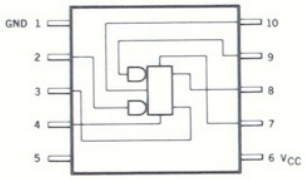
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE124 (5500)	AC Binary	1 volt	80 nsec	16 mW	8

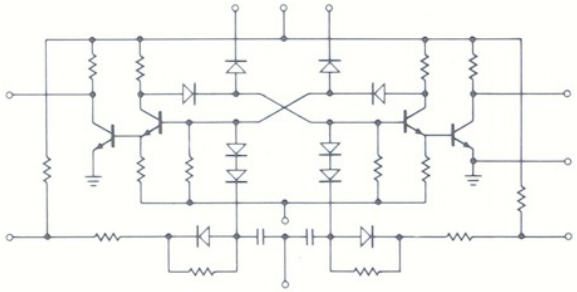
DESCRIPTION

Integrated binary element designed for use in high-speed, low-power digital systems. Operates from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



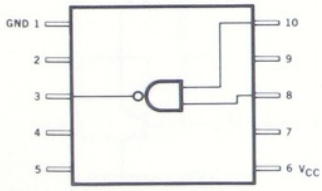
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE150 (5510)	Line Driver	1 volt	50 nsec	45 mW	20

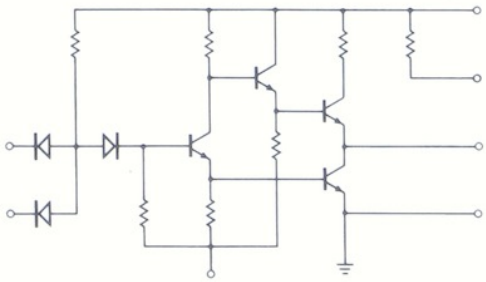
DESCRIPTION

High-speed two-input line driver well-adapted to high current and capacitive loads. Typical applications are driving clock and reset busses, terminated lines and similar interface connections. Designed to operate from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



Schematic

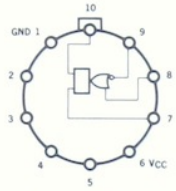
ADDITIONAL CURRENT SINKING CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SE160 (5511)	Multivibrator	—	50 nsec	32 mW	4

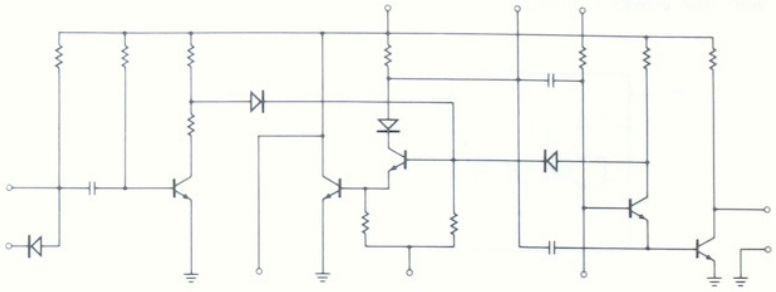
DESCRIPTION

Monostable multivibrator designed for use in high-speed low-power digital systems. Provides complementary output pulses. Output pulse rise and fall times are completely independent of output pulse width and may be used to trigger capacitively-coupled digital circuits. Operates from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



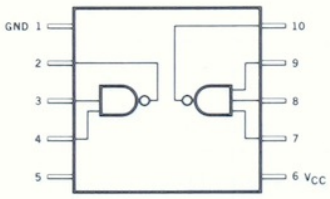
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
CS700 (5503)	NAND/NOR Gate	1 volt	30 nsec	15 mW	4

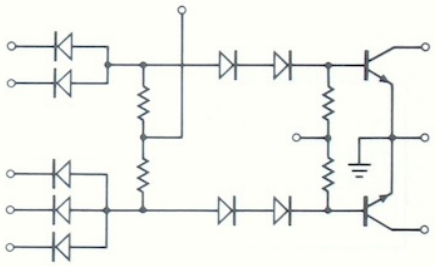
DESCRIPTION

Three-and-two input NAND/NOR gate for high-speed, low-power operation from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



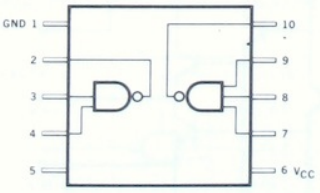
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
CS701 (5505)	NAND/NOR Gate	1 volt	30 nsec	20 mW	4

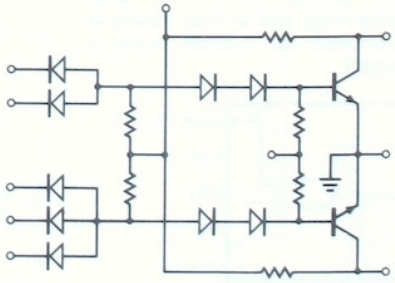
DESCRIPTION

Three-and-two-input NAND/NOR gate capable of operating at high speed with low power consumption from a single power supply.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



Schematic

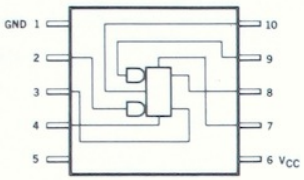
ADDITIONAL CURRENT SINKING CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
CS704 (5501)	AC Binary	1 volt	80 nsec	16 mW	8

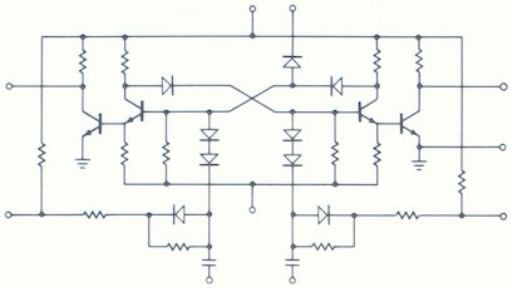
DESCRIPTION

Designed to operate from a single power supply in high-speed, low-power systems.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.0 volts ±10%	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



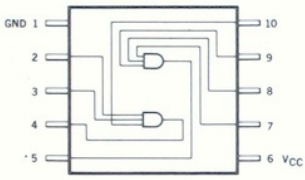
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
CS705 (5506)	Diode Array	—	—	—	—

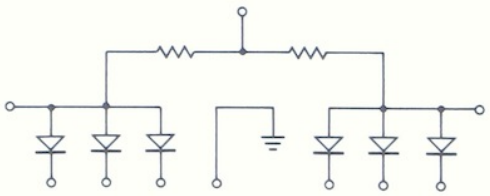
DESCRIPTION

Dual three-diode array designed to operate from a single power supply in high-speed, low-power digital systems.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
—	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram



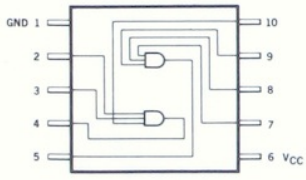
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
CS709 (5508)	Diode Array	—	—	—	—

DESCRIPTION

Dual three-diode array for use in high-speed, low-power digital systems. Operates from a single power supply.

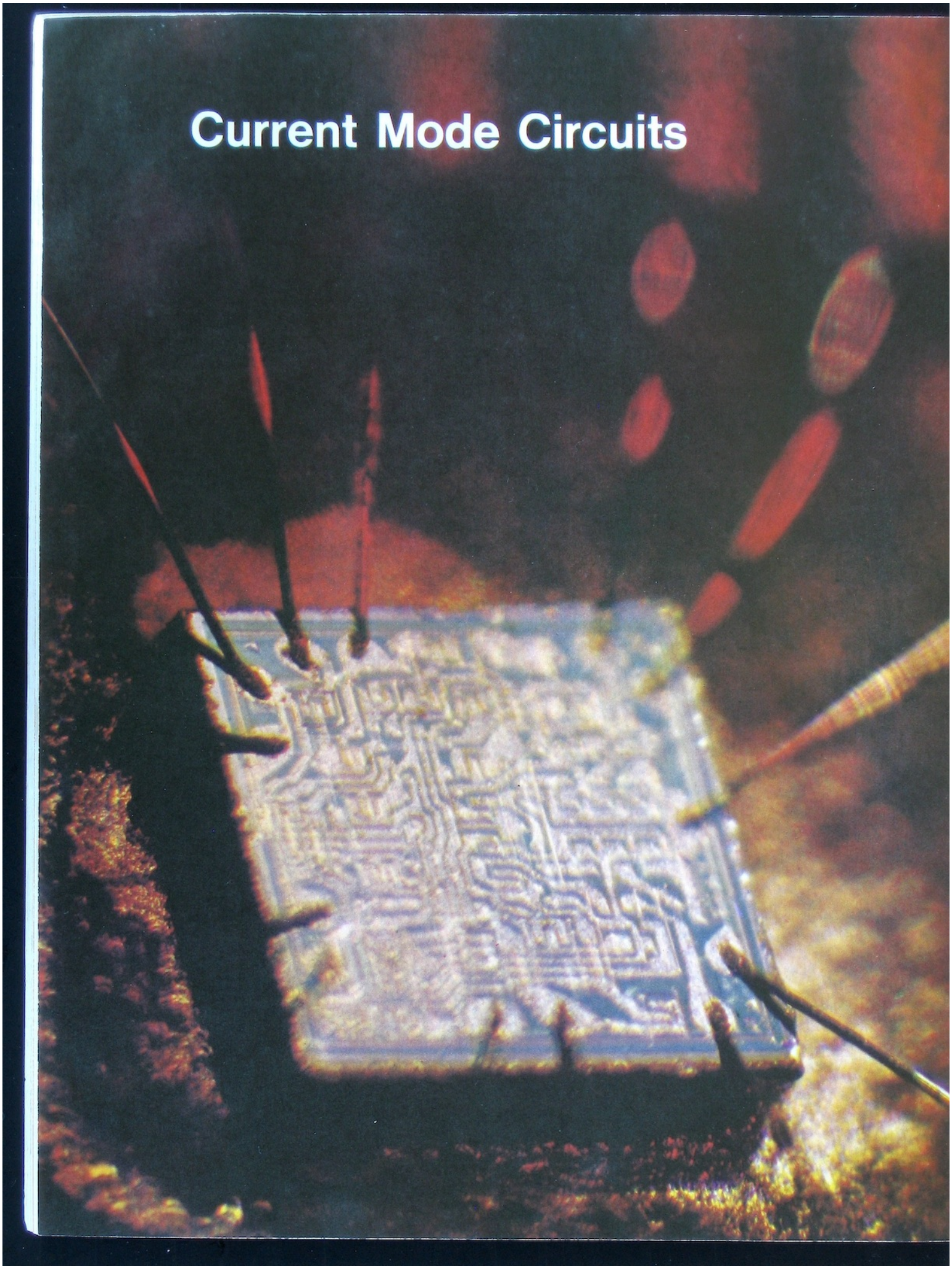
SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
—	−55°C to +125°C (51)	Flat Pack (3F) TO-5 (5E)



Logic Diagram

Schematic

Current Mode Circuits



TOTAL CAPABILITY

COMPLEMENTARY TRANSISTOR MICROLOGIC®

INTEGRATED CIRCUITS

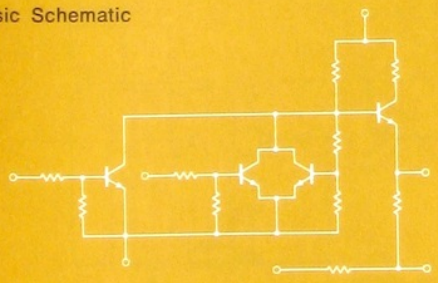
Fairchild Complementary Transistor Micrologic® integrated circuits were designed for very high-speed, low-cost commercial systems applications. The logic form is AND-OR-NOT. All circuits have provisions for output OR ties.

CTμL elements are designed to operate over a commercial ambient temperature range of +15°C to +55°C with forced air ventilation at 200 feet per minute. Power supplies are +4.5 V ±10% and −2 V ±10%. Power dissipation is designed to increase with fan-in and fan-out.

Absolute Maximum Ratings (25 C Free Air Temperature)

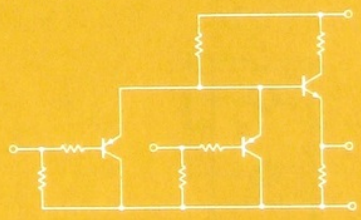
Positive Supply Voltage	−8 volts
Negative Supply Voltage	−4 volts
Maximum voltage applied to any pin (input or output)	+4 volts −2 volts
Storage Temperature	−65 C to +150 C
Power Dissipation	625 mW

Basic Schematic



Note: Only one 2-input inverter gate shown

Basic Schematic



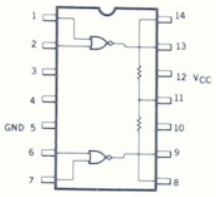
Note: Only one 2-input gate shown

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

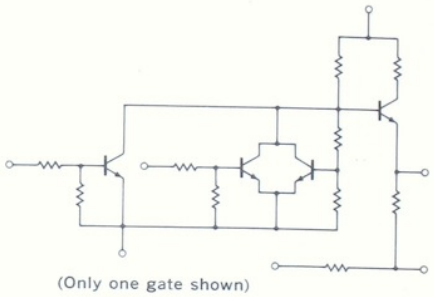
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9952	Dual Inverter Gate	500 mV	9 nsec	75 mW	12

DESCRIPTION
Dual two-input NOR gate for voltage level setting and logic inverting functions.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram

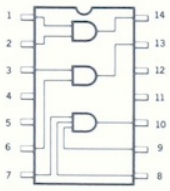


Schematic

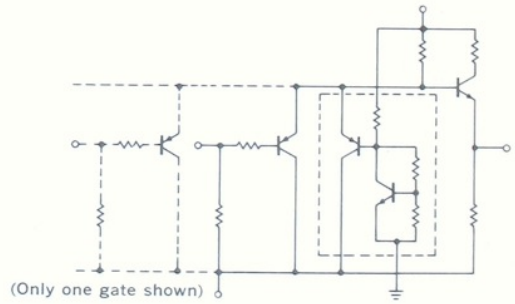
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9953	Triple AND Gate	500 mV	3 nsec	100 mW	15

DESCRIPTION
Dual two-input and single three-input AND gate.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram

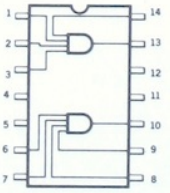


Schematic

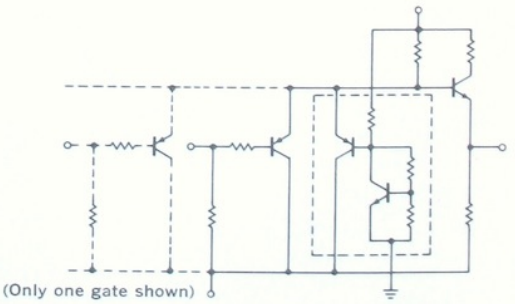
PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9954	Dual AND Gate	500 mV	3 nsec	65 mW	15

DESCRIPTION
Dual four-input AND gate.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



Schematic

All numbers in parentheses refer to Product Code, explained fully on p. 83.

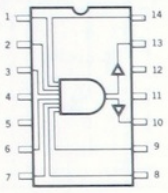
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9955	Single AND Gate	500 mV	3 nsec	33 mW	15

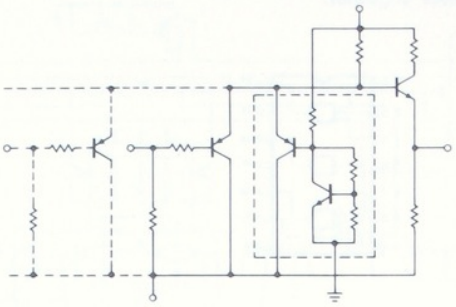
DESCRIPTION

Single eight-input AND gate with two separate outputs that may be used to isolate the output logic signal.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



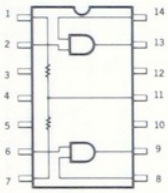
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9956	Dual Buffer	500 mV	12 nsec	150 mW	25

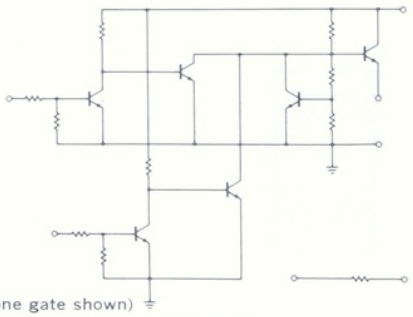
DESCRIPTION

Dual two-input non-inverting, level setting circuit used to drive high fan-out loads and as a line-driver.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (59)	Dual In-Line (6A)



Logic Diagram



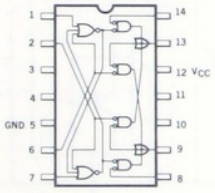
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9957	Dual-Rank Flip-Flop	500 mV	27 nsec	200 mW	9

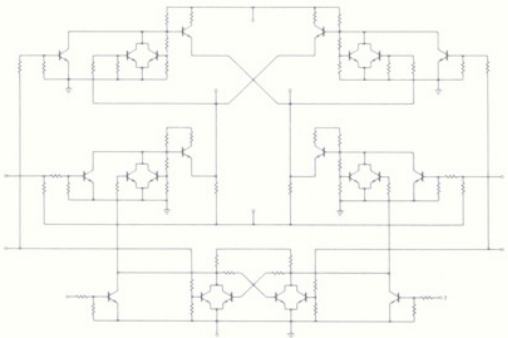
DESCRIPTION

Multi-purpose, direct-coupled dual-rank flip-flop suitable for counters, registers, and other storage applications.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



Schematic

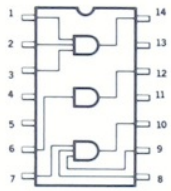
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9964	Triple AND Gate	500 mV	3 nsec	100 mW	15

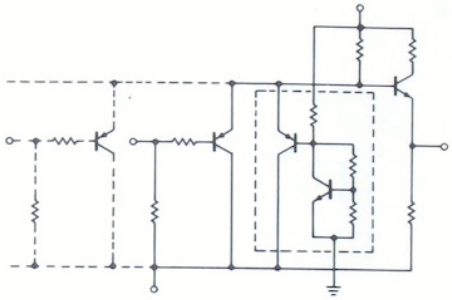
DESCRIPTION

3-3-1 input AND gate with OR provided by tying outputs together.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



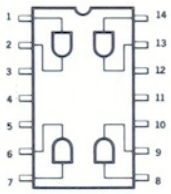
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9965	Quad AND Gate	500 mV	3 nsec	135 mW	15

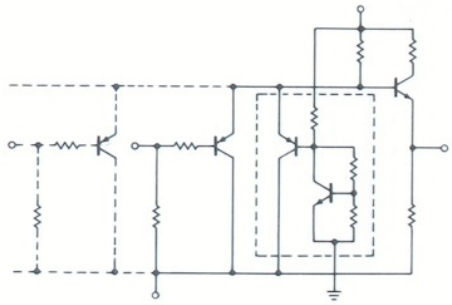
DESCRIPTION

1-1-1-1 input AND gate; OR by tying outputs together.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



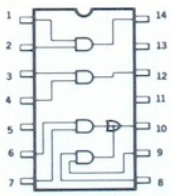
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9966	AND Gate	500 mV	3 nsec	65 mW	15

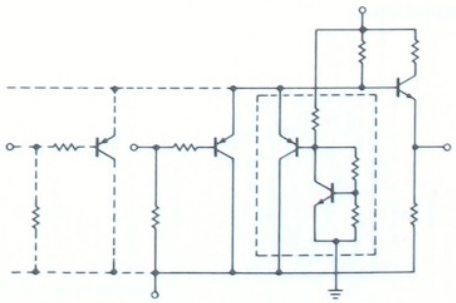
DESCRIPTION

Quad two-input AND gate, with two outputs OR tied.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



Schematic

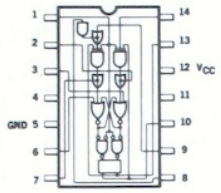
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9967	J-K Flip-Flop	500 mV	25 nsec	270 mW	15

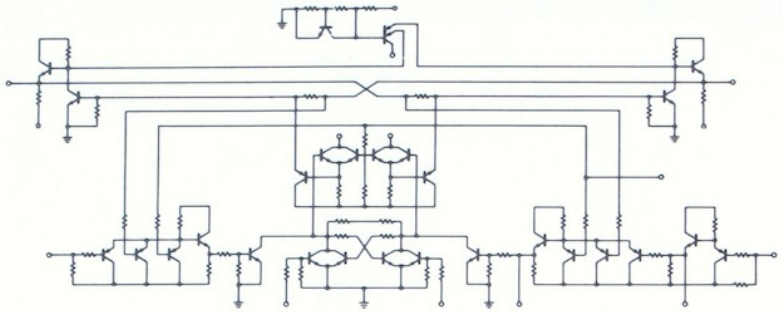
DESCRIPTION

Complete general purpose storage element suitable for use in shift registers, counters, or any type of control function. Fully compatible with other CTμL elements.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



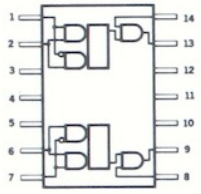
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9968	Dual Latch	500 mV	25 nsec	90 mW	15

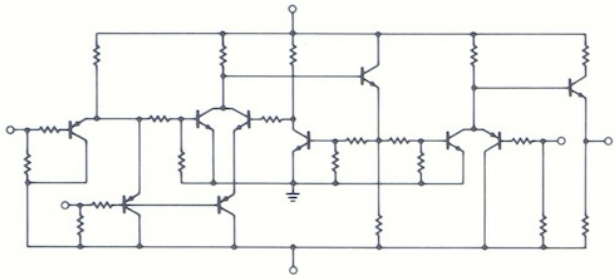
DESCRIPTION

Dual latch element designed specifically for use in high-speed scratch pad memory systems.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



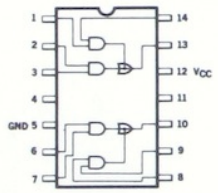
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9971	AND Gate	500 mV	3 nsec	65 mW	15

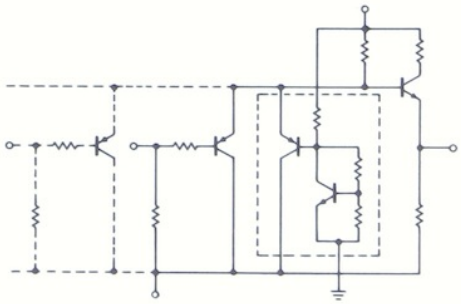
DESCRIPTION

Quad two-input AND gate with each pair of outputs OR tied.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)

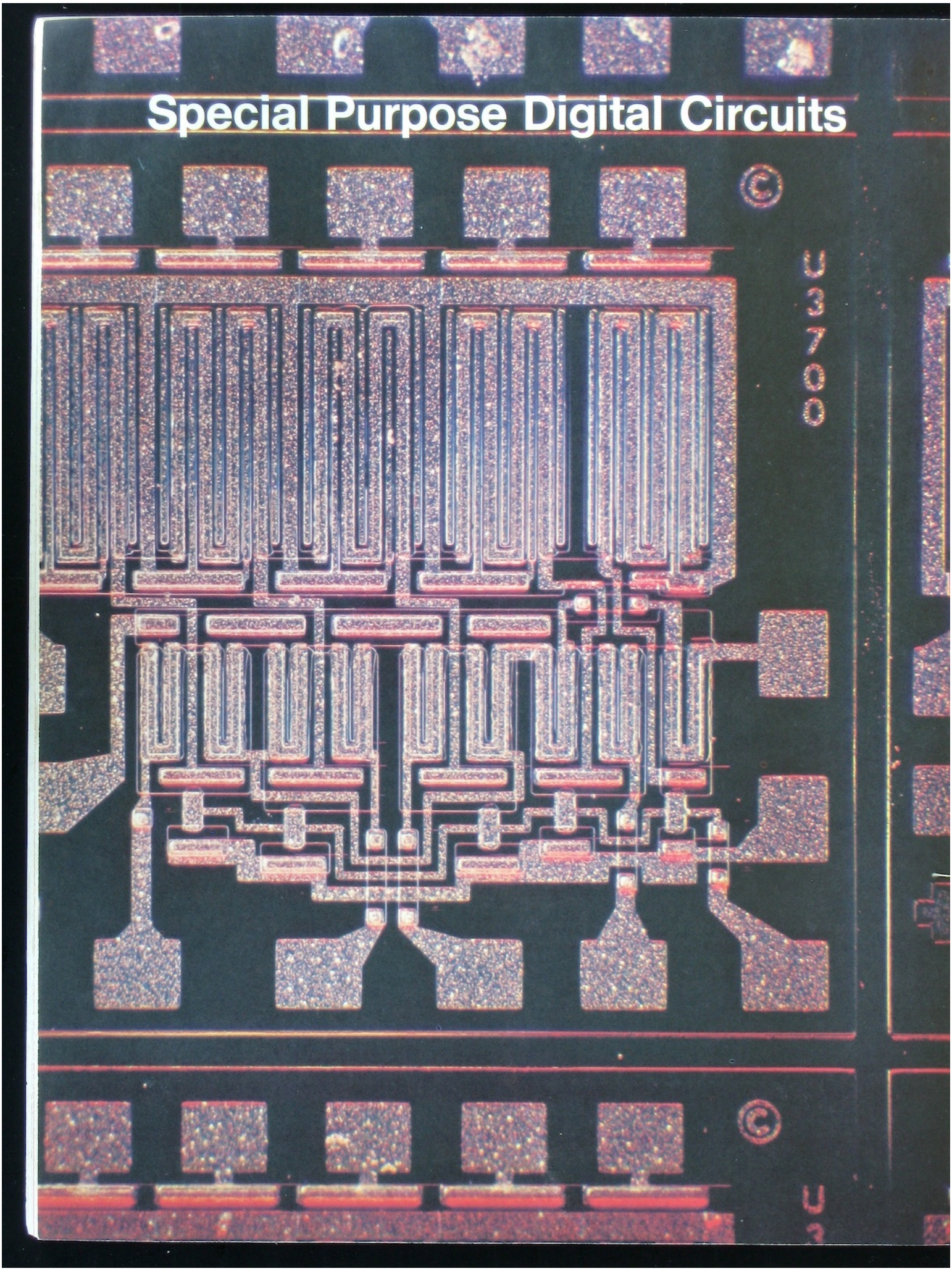


Logic Diagram



Schematic

Special Purpose Digital Circuits



Aware of the tremendous growth in the application of monolithic circuits, Fairchild has expanded its capability in digital integrated circuits beyond the customary boundaries of today's standard logic families to encompass whole new areas of applications and technology.

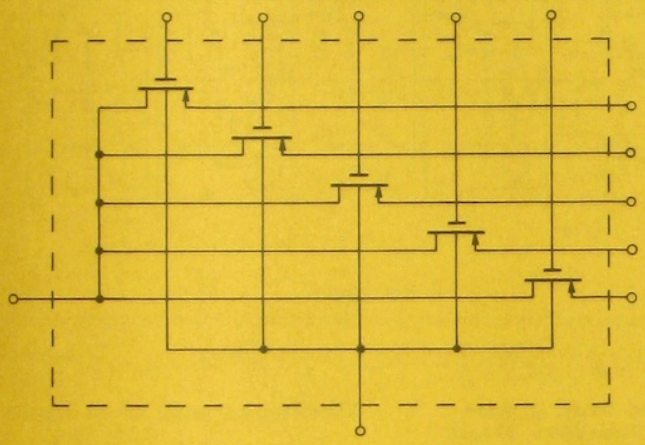
Fairchild MOS FET circuits represent an expansion into areas in which MOS technology is uniquely suited for low power and high impedance circuitry. And, since isolation of individual elements is not required, MOS FET technology is a natural starting point for large-scale integration on a reasonably small chip.

Fairchild Memory circuits represent a major bipolar entry into the field of large-scale integration. Uses of memory elements will include local storage, scratchpad memories, and bulk storage, and will allow the computer manufacturer to realize fully-integrated systems at the lowest possible cost consistent with reliability requirements.

MOS FET CIRCUITS

μM3400 MOS FET Integrated Five-Channel Switch

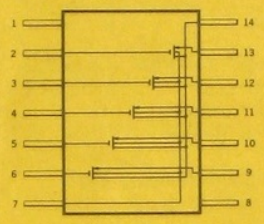
Five-channel, single output switch useful as a basic switching element for airborne or ground instrumentation, telemetry, or other signal routing applications.



Schematic

TYPICAL CHARACTERISTICS

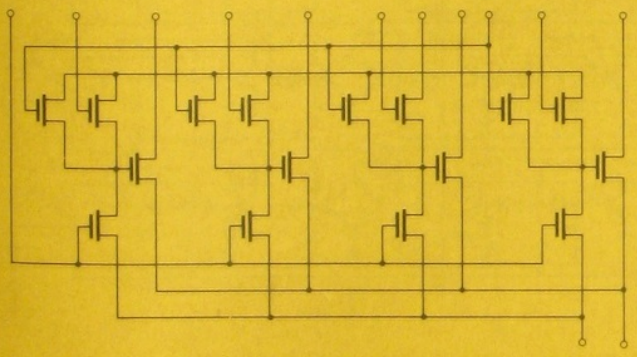
Input analog signal	±10 volts
Channel ON resistance	2 KΩ
OFF/ON impedance ratio	10/1
Input leakage current	0.2 nA
Input capacitance	4 pf
Forward gate leakage current	10 pA
Output leakage current	0.5 nA
Output capacitance	16 pf
Output current	10 mA
Operating junction temperature	−65°C to +175°C
Operating case temperature	−55°C to +125°C



Logic Diagram

μM3700 MOS FET Integrated Four-Channel Switch

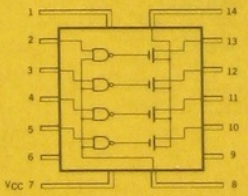
Multi-channel switch useful in multiplexing, telemetry, and A & D conversion systems where low channel ON resistance, high output current, and low channel leakage is required. Features all-channel blanking capability, and diode protection for each control gate.



Schematic

TYPICAL CHARACTERISTICS

Input analog signal	±10 volts
Channel ON resistance	300Ω
Input leakage current	1 nA
Input capacitance	7 pf
Output leakage current	5 nA
Output capacitance	40 pf
Output current	20 mA
Channel turn-on time	500 nsec
Channel turn-off time	2 μsec
Power dissipation	200 mW



Logic Diagram

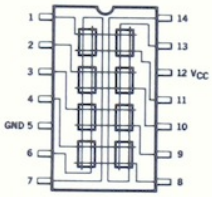
MEMORY CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9030	8-Bit Memory Cell	1 volt	—	300 mW	2

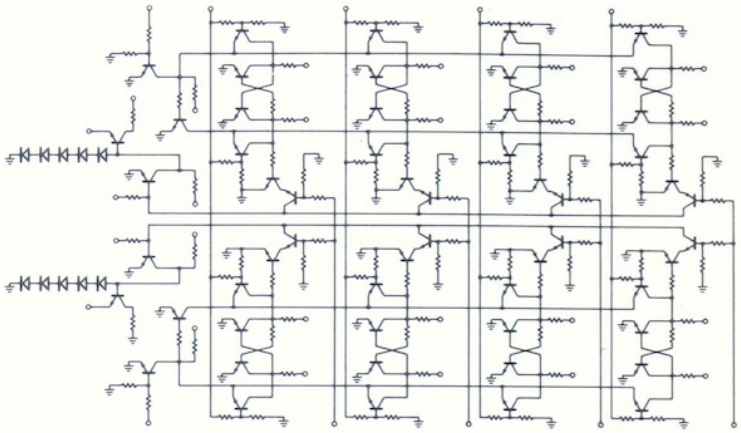
DESCRIPTION

Integrated eight-bit memory cell consisting of four two-bit words. The cell features non-destructive readout, and is addressable by word. Permissible to write one word while reading another. Same information may be written in two words simultaneously.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4.5 volts ±10%	+15°C to +55°C (79)	Dual In-Line (6A)



Logic Diagram



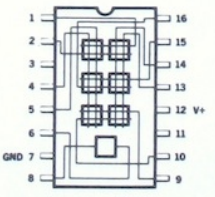
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9032	6-Bit DTμL Memory Cell	1 volt	Read Delay: 20 nsec Write Pulse Width: 20 nsec	300 mW	30 mA at V_{sat} = 0.5 V max.

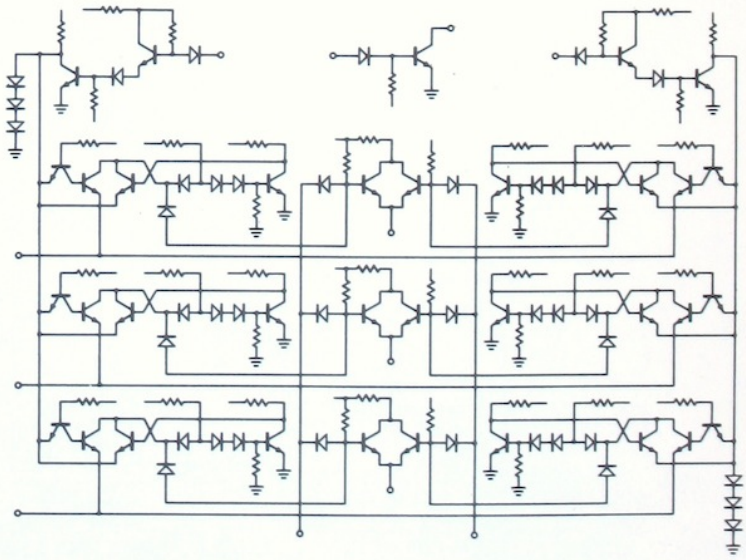
DESCRIPTION

Two word, three bits each, non-destructive DTμL memory cell.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
+6 V, −3 V	+5°C to +65°C	Dual In-Line



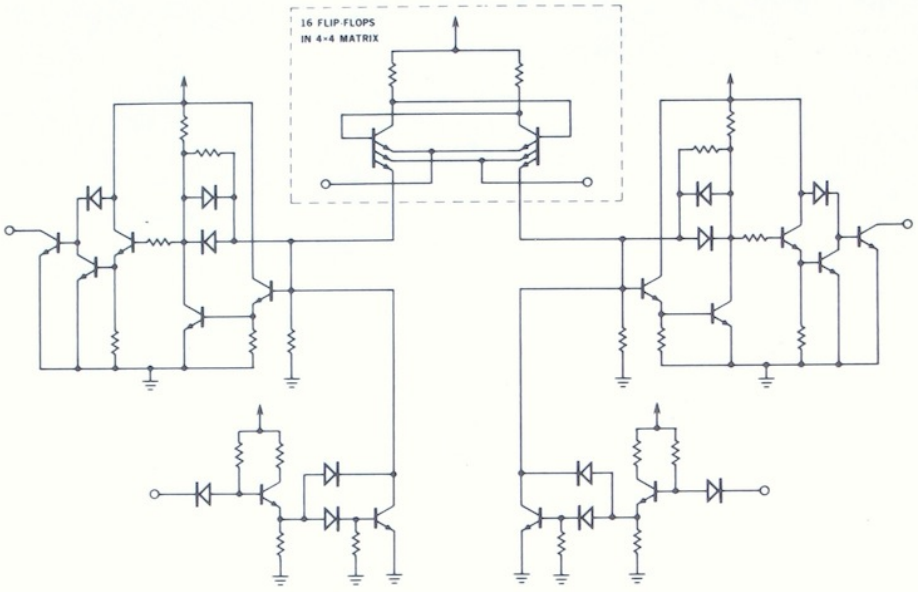
Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
9033	16-Bit Memory Cell	300 mV	20 nsec	200 mV at 5 V	3 mA output current

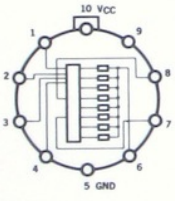
DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Coincident voltage four-by-four matrix, address non-destructible read-out scratchpad memory cell.	4 to 5 volts	0°C to +75°C	Dual In-Line



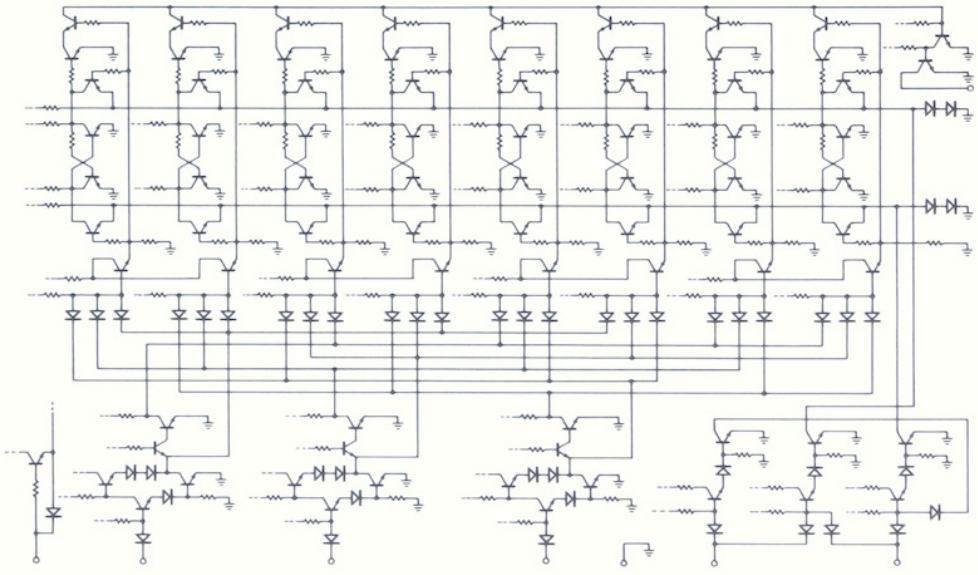
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1128	8-Bit Memory Cell	1 volt	Read: 40 nsec Write: 40 nsec	250 mW	60 mA at .5 V

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
DTμL eight-bit memory cell, including address decoder.	4 volts	0°C to +75°C	TO-5

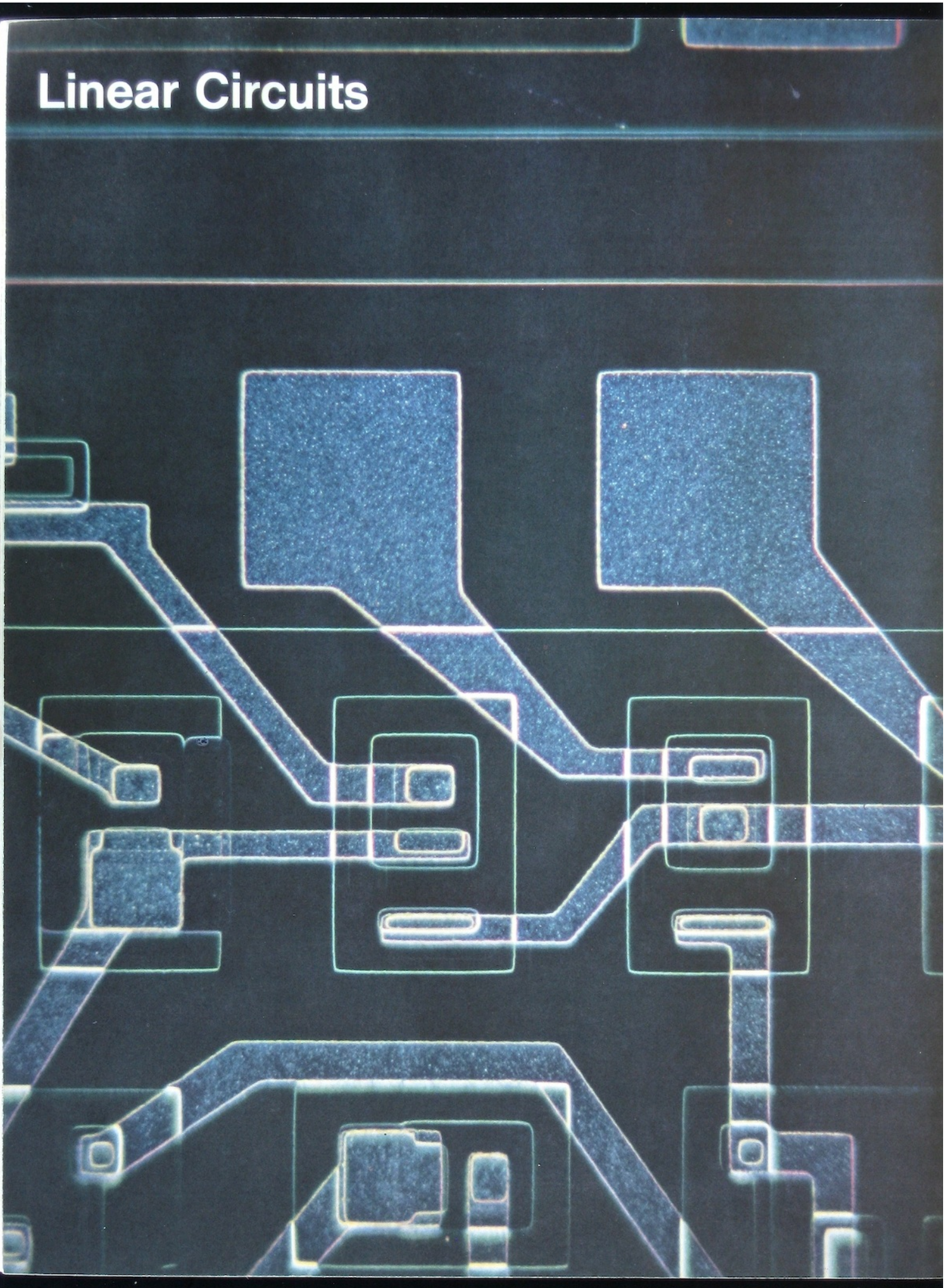


Logic Diagram



Schematic

Linear Circuits



TOTAL CAPABILITY

LINEAR

INTEGRATED CIRCUITS

Fairchild Linear Integrated Circuits comprise a set of compatible "building blocks" for use individually or in combinations for a wide range of applications. They offer specific advantages in cost, size, speed, and reliability over discrete components for applications in analog equipment. Their use reduces the complexities of design and assembly, affording equipment which is superior in performance and lower in cost.

Fairchild's philosophy in designing linear integrated circuits is to use standard linear circuits wherever possible, but with discrete components added to provide flexibility or to accomplish functions which are not economically integrated.

Outstanding characteristics of integrated circuits are used to eliminate parts that might be used but cannot be integrated economically. For example, DC rather than AC coupled amplifiers are used, as they can easily be integrated, and eliminate the need for large capacitors.

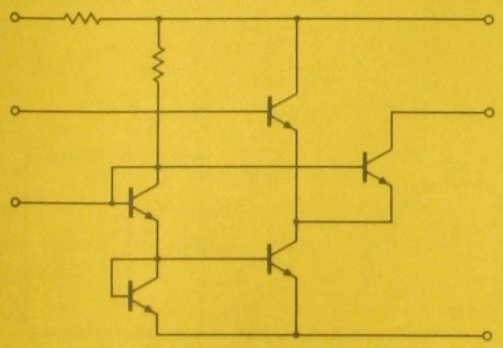
For the design engineer, this optimum usage of discrete parts and standard integrated circuits affords a flexibility which leads to superior circuit design. For the user, it boils down to the immediate availability of a completely specified product at low cost.

All Fairchild Linear Integrated Circuits feature single-chip construction using the patented Planar* epitaxial process which has proved so reliable in digital Microcircuits.

7703 MONOLITHIC I-F LIMITING AMPLIFIER

The 7703 is a linear integrated circuit with useful unneutralized power gain for frequencies in excess of 100 MHz. It features the capability of nonsaturating limiter operation with a suitable output load at all frequencies, making it ideally suited for FM I-F limiter applications.

Other useful applications are as a wideband amplifier, a voltage-controlled oscillator, a locked oscillator for color TV reference signals, and an FM mixer.



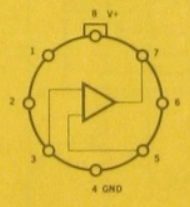
Schematic

TYPICAL CHARACTERISTICS*

Working supply voltage	+12 V
Stability limited gain	41 db
Forward transadmittance	25 mmhos
Reverse transadmittance	.002 mmhos
Input conductance	.50 mmhos
Output conductance	.02 mmhos

*f=10.7 MHz

TEMPERATURE RANGE	PACKAGE
−55°C to +125°C (31)	TO-5 (5B)
0°C to 70°C (39)	Epoxy (8A)



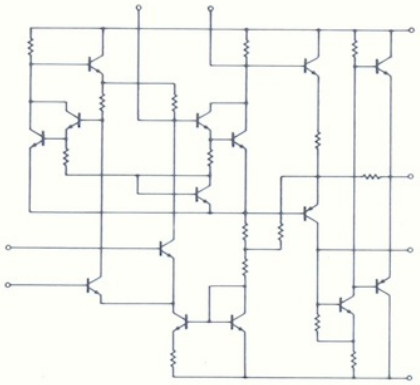
Logic Diagram

*Planar is a patented Fairchild Process

7709 HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

The 7709 is functionally identical to the 7712, but it features considerably improved d-c characteristics. In addition to performing many of the same functions as the 7712, the 7709's larger dynamic range makes it useful as a voltage follower, as a current generator, or as a generator of special linear and nonlinear transfer functions. Its lower input current permits its use in higher impedance circuitry than the 7712. The 7709 is completely specified over a wide range of supply voltages to fit varying requirements.

The 7709 uses the unique properties of integrated circuits to overcome many of their so-called limitations, giving discrete-component performance in a relatively simple microcircuit.

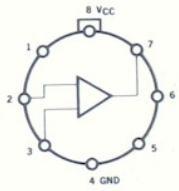


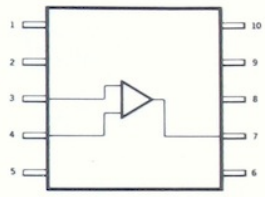
Schematic

TYPICAL CHARACTERISTICS

Working supply voltage	+15V, −15V
Input offset voltage	1 mV
Temperature drift	3 μV/°C
Input offset current	50 nA
Input bias current	200 nA
Input resistance	400 KΩ
Input voltage range	±10 V
Voltage gain	45,000
Output voltage swing	±13 V at 5 mA
Power supply rejection	25 μV/V
Power consumption	80 mW

TEMPERATURE RANGE		PACKAGE	
−55°C to +125°C	(31)	TO-5	(5B)
0°C to 70°C	(39)	Flat Pack	(3G)



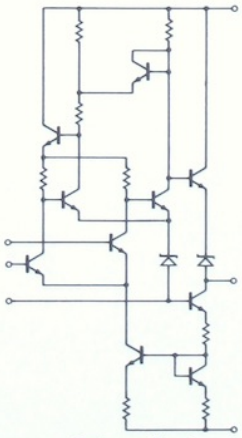


Logic Diagram

7710 HIGH-SPEED DIFFERENTIAL COMPARATOR

The 7710 is a differential voltage comparator featuring exceptionally fast recovery from saturation and an output which is compatible with all popular integrated logic forms. It is useful as a low hysteresis, variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a high noise immunity digital line receiver, a zero-crossing detector, and in many other applications.

The 7710 makes use of the low wiring capacitances of monolithic circuits to achieve high-speed operation at moderate power levels. The exceptional matching characteristics of integrated components are reflected in the low offset and thermal stability.

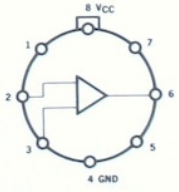


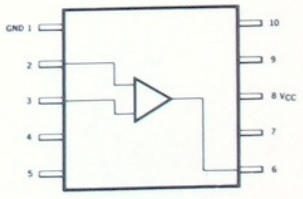
Schematic

TYPICAL CHARACTERISTICS

Working supply voltage	+12V, −6V
Input offset voltage	2 mV
Thermal drift	5 μV/°C
Input offset current	1 μA
Input voltage range	± 5V
Voltage gain	1500
Response time (5 mV overdrive)	40 nsec
Output swing	−0.5 to +3.2V
Power consumption	110 mW

TEMPERATURE RANGE		PACKAGE	
−55°C to +125°C	(31)	TO-5	(5B)
0°C to 70°C	(39)	Flat Pack	(3H)





Logic Diagram

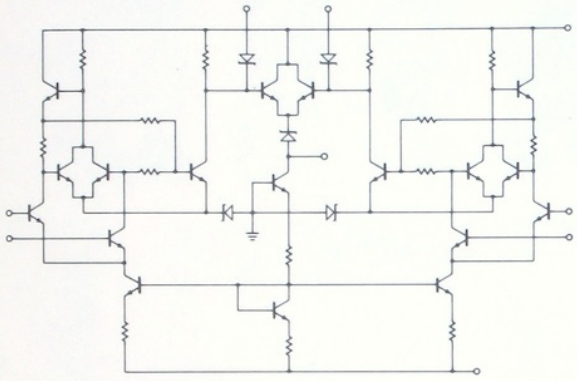
7711 DUAL COMPARATOR

The 7711 is a dual differential voltage comparator, similar in operation to the 7710. An important application is as a core memory sense amplifier. When used as a sense amplifier, the threshold voltage is determined by external resistors and is almost independent of integrated circuit characteristics; thus, excellent temperature stability is realized. The device is fast enough to work with core sizes down to 20 mils. Independent strobing of both comparator channels is provided and pulse stretching at the output is easily accomplished. Other uses of the dual comparator are as a window discriminator in pulse height detectors and as a double-ended limit detector for automatic go/no-go test equipment. Applications requiring two 7710's are well suited for the 7711.

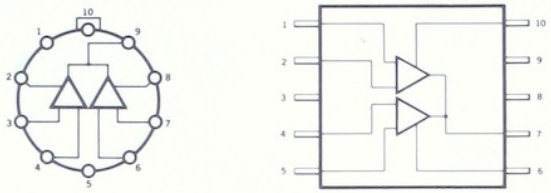
TYPICAL CHARACTERISTICS

Working supply voltage	+12V, −6V
Input offset voltage	1 mV
Thermal drift	3 μV/°C
Input offset current	0.5 μA
Input voltage range	±5 V
Voltage gain	1500
Response time (5 mV overdrive)	40 nsec
Strobe release time	12 nsec
Output voltage swing	−0.5 to +4.5V
Power consumption	130 mW

TEMPERATURE RANGE	PACKAGE
−55°C to +125°C (31)	TO-5 (5B)
0°C to 70°C (39)	Flat Pack (3G)



Schematic



Logic Diagram

7712 WIDEBAND D-C AMPLIFIER

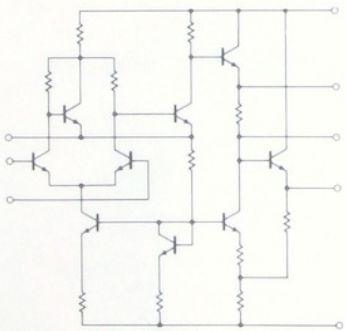
The 7712 is useful as a general purpose a-c or d-c amplifier to frequencies as high as 30 MHz. It is a high-gain operational amplifier meant for use with external feedback elements to determine operating characteristics. Applications include amplifying the output of transducers such as resistive bridges, thermocouples, hall-effect devices and photodevices. With proper feedback elements, it can also perform the integrating, differentiating, summing and subtracting functions required in an analog computer. The 7712 is specified over a wide range of supply voltages to fit varying requirements.

The 7712 takes advantage of the excellent matching and close thermal coupling inherent in monolithic construction to achieve low offset, low drift, and nearly instantaneous thermal stabilization.

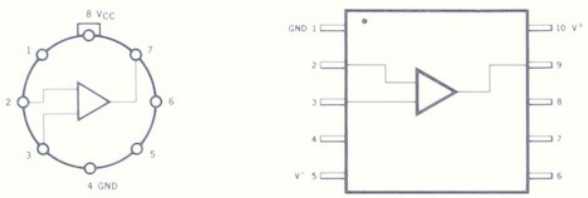
TYPICAL CHARACTERISTICS

Working supply voltage	+12V, −6V
Input offset voltage	2 mV
Thermal drift	5 μV/°C
Input offset current	0.7 μA
Input bias current	4 μA
Input resistance	25 KΩ
Voltage gain	2600
Output resistance	200Ω
Output swing	±5.3 V
Power consumption	70 mW

TEMPERATURE RANGE	PACKAGE
−55°C to +125°C (31)	TO-5 (5B)
0°C to 70°C (39)	Flat Pack (3H)



Schematic



Logic Diagram

Hybrid Circuits

TOTAL CAPABILITY

HYBRID

INTEGRATED CIRCUITS

Standard monolithic integrated circuits may not always represent the best solution to a design problem. For this reason, Fairchild Semiconductor has expanded its capabilities in hybrid and custom circuits to provide customers with a circuit specifically tailored to meet the needs of any application.

The circuits shown in this section illustrate the flexibility attainable with Fairchild Hybrids — both Standard and Custom. Design criteria and options are outlined so that customers may judge for themselves whether hybrid circuits would be more desirable than custom monolithic circuits, which are described in a later section.

Fairchild defines a hybrid circuit as a single element tested as a circuit, and constructed using multiple interconnected chips.

Hybrids are valuable in a number of applications. Generally speaking, they should be given careful consideration if a requirement falls into any of the following categories:

$BV_{CBO} > 12$volts

$I_C > 75$ mA

Speed greater than 40 MHz

Bandwidth greater than 25 MHz

Use of PNP transistors

Special device application, such as analog switch, etc.

Tight component tolerances

Assembly cost savings

Any custom design order of less than 10,000 units

Various requirements from this list can be met by a great number of suppliers. Only Fairchild, however, can supply the complete range of capabilities, from discrete components to hybrids to integrated circuits.

Pursuing the concept of total capability, Fairchild now manufactures three hybrid families:

Linear Hybrid Elements
Digital Hybrid Elements
Complex Hybrids

The combination of multiple monolithic chips in a single package gives the design engineer maximum flexibility in choosing the right circuit to do the job, as well as the ability to interconnect these circuits to perform a specific custom logic function.

With linear elements, the concept of total capability has been extended to the linear circuit design engineer, who can now design a complete transfer function into a single package, using multiple monolithic operational amplifiers.

The step from custom digital integrated circuits to complex circuits is easily traversed using digital hybrid elements. The logic designer has the flexibility of designing custom logic patterns without being hampered by the inflexible logic patterns of standard arrays.

"Trade-off" is not a word often used by engineers using Fairchild complex hybrids. Linear and digital monolithic circuits can be combined with other active and passive components to form complex circuits which give the engineer the performance of discrete devices in a very small package.

STANDARD HYBRID CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SH2001	High-Voltage, High-Current Driver	800 mV	80 nsec	50 mW	100

DESCRIPTION

Incorporates a DTμL element driving a high-current NPN transistor.

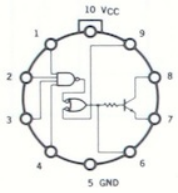
Sinks up to 250 mA from a power source of 40 volts or less.

Features a four-input NAND gate for decoding purposes, plus a NOR input.

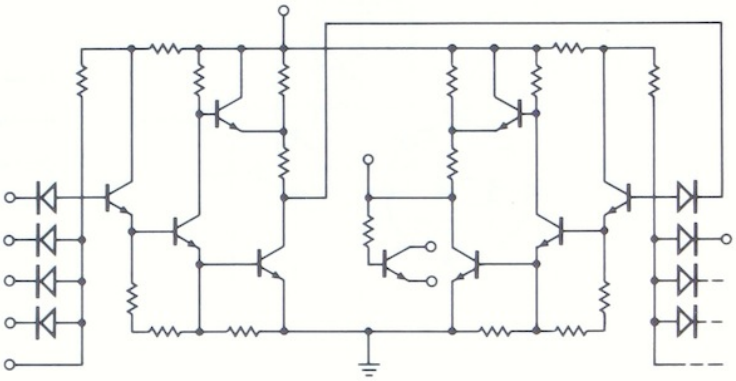
Buffer output can be connected back to one of the NAND inputs to form a three-input latch circuit with NOR input used as a set input.

Applications include decoder / lamp driver, relay driver, core driver for small arrays, or clock driver.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
4 to 5 volts ±10%	−55°C to +125°C	Flat Pack
	0°C to +70°C	TO-5
		Custom Packaging



Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SH2100	High Current Driver	400 mV	25 nsec	65 mW	200

DESCRIPTION

Consists of an RTμL buffer circuit driving a high-current transistor.

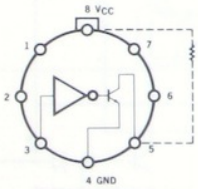
Designed for driving RTμL elements and other high-current driver applications.

Interfaces with DTμL and Low Power RTμL.

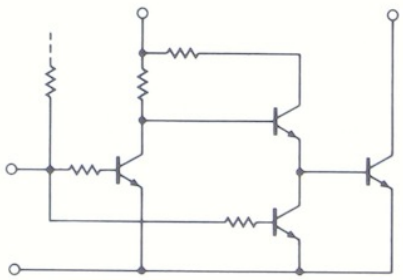
Input characteristics are compatible with all RTμL circuits.

Output can drive loads up to a maximum voltage of 12 volts and a maximum current of 250 mA.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.0 volts ±10%	−55°C to +125°C	Flat Pack
3.7 volts ±10%	0°C to +70°C	TO-5



Logic Diagram



Schematic

STANDARD HYBRID CIRCUITS

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SH2101	High Voltage Driver	500 mV	35 nsec	10 mW	50

DESCRIPTION

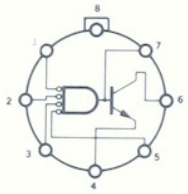
Consists of an integated four-input Low Power RTμL gate driving a high-voltage transistor.

Sinks up to 10 mA with output of 100 volts.

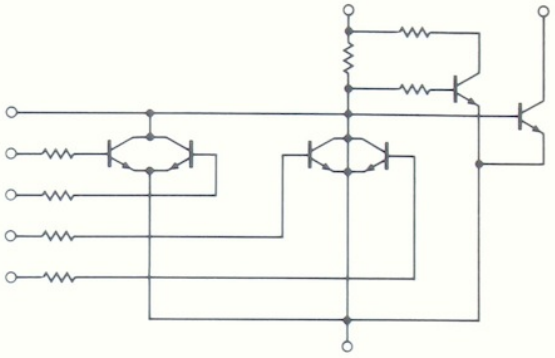
Input compatible with all members of RTμL, DTμL, and CTμL families.

Applications include neon bulb and gas readout tube driver, and high-voltage interfacing.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
3.6 volts ±10%	−55°C to +125°C 0°C to +70°C	TO-5



Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SH2510	Two-Stage Counter-Register	1.1 V	60 nsec	100 mW	7

DESCRIPTION

Consists of two DTμL 9948 Flip-Flop chips.

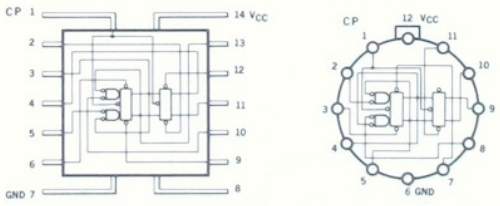
Features individual asynchronous set and clear inputs.

6 MHz typical counting rate.

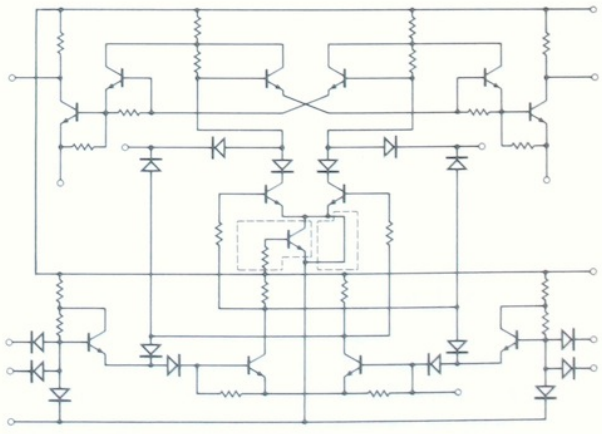
Compatible with Fairchild DTμL family.

Applications include shift register, modulo 3 or 4 shift counter/register, and parallel input, serial output register.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±10%	−55°C to +125°C 0°C to +70°C	Flat Pack TO-5



Logic Diagram



(Shows single stage)

Schematic

SH3000 High Impedance Wideband DC Amplifier

Two high-gain, matched transistors connected as emitter-followers at the inputs of a μA7712 operational amplifier.

Features protected latch-up.

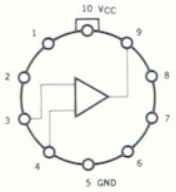
5 MΩ typical input impedance.

.3 μA typical input bias current.

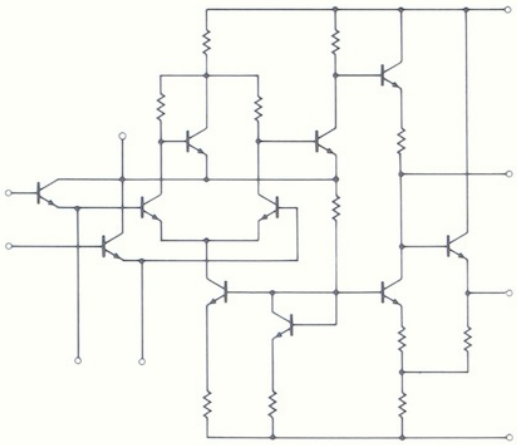
Useful bandwidth DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage Between V+ and V− Terminals	21 volts
Peak Load Current	50 mA
Input Voltage	+0.5 volts to −6.0 volts
Differential Input Voltage	±5 volts
Internal Power Dissipation	300 mW
Operating Temperature Range	−55°C to +125°C



Logic Diagram



Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	ON RESISTANCE
SH3001	Analog Switch	700 mV	120 nsec	60 mW	300Ω

DESCRIPTION

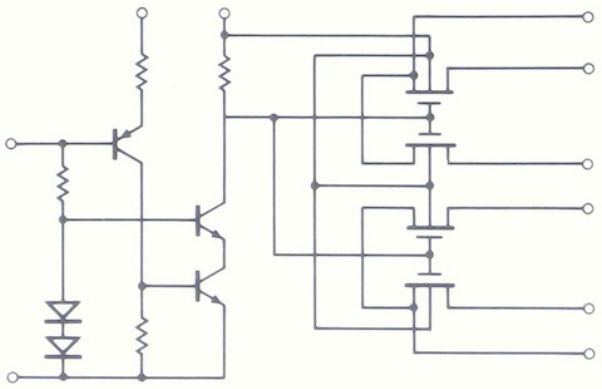
Incorporates three bipolar transistors and two dual-drain MOS transistors.

Input can be driven from any DTμL element, or any RTμL unloaded output.

Use of MOS transistors allows more complete isolation between switch drive and switch contacts.

Applications include scanning, multiplexing, A/D conversion and other telemetry circuitry, as well as many high-level switching or chopper uses.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
+10 volts, −20 volts	−55°C to +125°C	TO-5



Schematic

SH3005 High Impedance Differential Comparator

The SH3005 consists of a pair of high current gain, matched transistors connected as emitter-followers at the inputs of a μA7710 comparator.

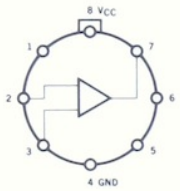
2 MΩ input impedance.

8 μA input bias current.

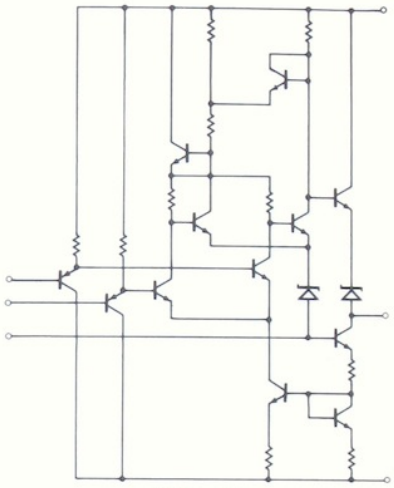
Applications include variable threshold Schmitt trigger, pulse height discriminator, high noise immunity line receiver, and memory sense amplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+14 volts, −7 volts
Peak Output Current	10 mA
Input Voltage	±7.0 volts
Differential Input Voltage	±5.0 volts
Internal Power Dissipation	300 mW
Operating Temperature Range	−55°C to +125°C 0°C to +70°C



Logic Diagram



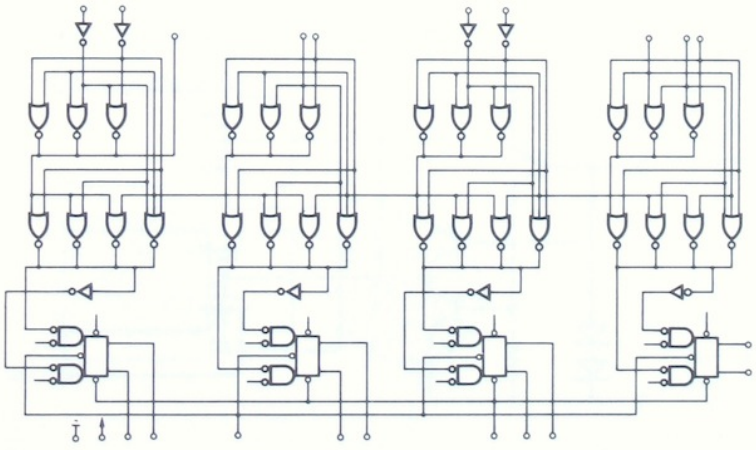
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
SH8080	Four-Bit Arithmetic Unit	1 volt	Input of 1st Carry or 1st Addends to carry output of 4th Adder: 100 nsec Sum: 150 nsec on last summer	525 mW	4 (min)

DESCRIPTION

A DTμL compatible four-bit fast-carry serial adder combined with a four-stage accumulator register.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5 volts ±10%	0°C to +70°C	32-lead Flat Pack



Logic Diagram

CUSTOM HYBRID CIRCUITS

AVAILABLE COMPONENTS

Custom hybrid circuits can be constructed using any combination of the following Fairchild components:

RESISTORS

1. Nickel-chromium on silicon (10Ω to 500kΩ)
   Standard RETMA values
   Temperature coefficient = 100 ppm/°C
   Absolute tolerance ±2%
2. Nickel-chromium on ceramic (Al_2O_3)
   Custom resistor patterns
   Temperature coefficient = ±20 ppm/°C
   Resistor match 0.1%
   Absolute tolerance ±2%
   Resistivity = 150Ω/square

CAPACITORS

1. MOS (20 pf to 1,000 pf)
   Temperature coefficient = 250 ppm/°C
   Absolute tolerance ±20%
2. Tantalum (500 pf to 4,000 pf)
   Temperature coefficient = 250 ppm/°C
   Absolute tolerance ±20%

TRANSISTORS

Any silicon transistor listed in our current catalogue.

MICROCIRCUITS

RTμL, Low Power RTμL, DTμL, LPDTμL, Linear Microcircuits, and other monolithic integrated circuits

DIODES

Fairchild's complete line of ultra fast silicon Planar* diodes, zener diodes, and diode assemblies

AVAILABLE PACKAGES

Any Fairchild package can be used for custom hybrid circuits, and unusual packaging requirements will be considered:

TO-5:	8, 10, 12 lead O_{i-c} 60°C/W with insert, capable of handling up to 12 chips
Flat pack:	10 to 14 lead, O_{i-c} 80° C/W, capable of handling up to 9 chips.
Flat pack ⅜" x ⅜"	14 lead, capable of handling up to 15 chips
Flat pack .75 x .9	32 lead, capable of handling linear or digital circuits.
Dual in-line (Dip):	16 lead, capable of handling 4 to 10 chips.

*Planar is a patented Fairchild Process

SH9002 Series Voltage Regulator

Consists of multiple discrete transistors, diodes, and resistors.

For use in all regulated power supplies.

Provides a constant voltage to specified loads independent of fluctuations in the power supply.

CIRCUIT CHARACTERISTICS:

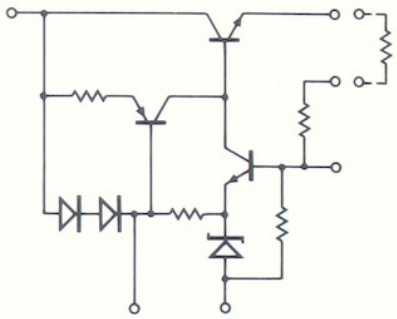
Greater than 0.1% accuracy

8 V_{DC} to 20 V_{DC} voltage regulator

Adjustable by varying external resistor R_X

$$\text{Output Voltage} = \frac{7.3\ (9.0\,K + R_X)}{7.5\ K}$$

Available in a TO-5 package



Schematic

SH9004 RF/IF Amplifier

Incorporates discrete component chips in a single circuit.

Circuit components shielded from external signal noise by a grounded TO-5 case.

Used in all communications equipment for amplification of RF signals (100 MHz to 300 MHz).

Also used for amplification of IF signals (Radio: 455 kHz, Television: 45 MHz, and Radar: 60 MHz).

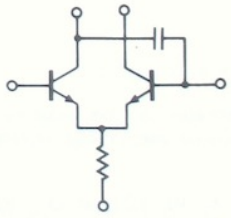
CIRCUIT CHARACTERISTICS:

30 db gain

Bandwidth from DC - 300 MHz

AGC capabilities

Available in TO-5 and ¼" x ¼" Flat Pack



Schematic

SH9006 Sense Amplifier

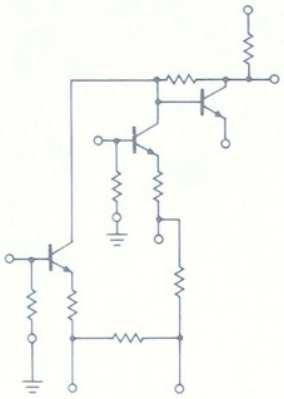
Incorporates discrete component chips in a single circuit.

Features common mode rejection.

CIRCUIT CHARACTERISTICS:

Greater than 28 db gain up to 60 MHz

Available in TO-5 and ¼" x ¼" Flat Pack



Schematic

SH9007 Dual Low Power DTμL Flip-Flop

Incorporates two LPDTμL 9040 chips in a single circuit.

Characterized by low power and medium speed.

Especially useful for satellite and missile applications.

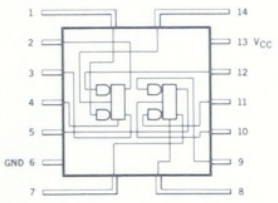
NOISE IMMUNITY	PROPAGATION DELAY	POWER DISSIPATION
(TYP., 25°C) 1.1 volts	(TYP., 25°C) 40 nsec	(TYP., 25°C) 6 mW/flip-flop

FAN-OUT	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
10	4 to 7 volts	−55°C to +125°C	Flat Pack TO-5 Dual In-Line

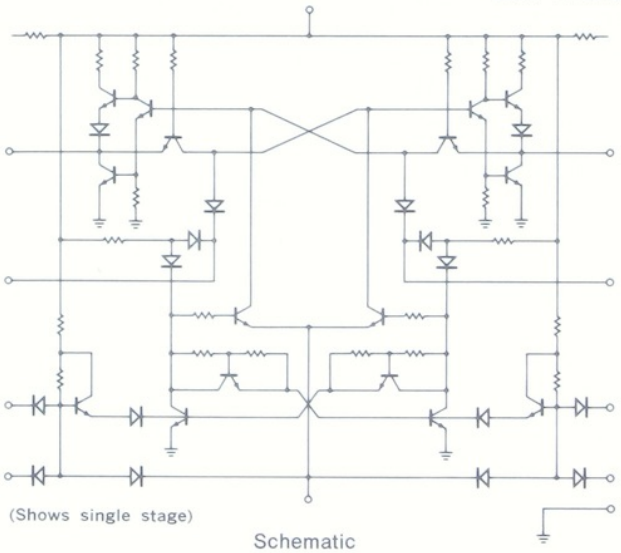
Circuit Characteristics:

8 mW power drain

2.5 MHz binary clock rate



Logic Diagram



(Shows single stage)

Schematic


Custom Circuits

TOTAL CAPABILITY
CUSTOM
INTEGRATED CIRCUITS

Fairchild Custom Microcircuits are a natural outgrowth of proven success in the production of high reliability, off-the-shelf Planar* Micrologic® integrated circuits.

Fairchild's philosophy in designing custom integrated circuits is to utilize a total capability in monolithic construction to the best advantage, without directly adapting discrete component design. Many of the restrictions imposed by monolithic construction can be overcome at the circuit design level. At this stage, it is possible to avoid the restrictions imposed by limited types of components, loose tolerances, and the limited range of many component values, while capitalizing on the inherent advantages of integrated circuits. Specifically, these include:

- Close matching of active and passive devices over a wide temperature range
- Excellent thermal coupling throughout the circuit
- Economy of using a large number of active devices
- Freedom of selection of active device geometries
- Availability of devices that have no exact discrete element counterpart

Careful circuit design is of practical significance because it is a non-recurring cost in a particular microcircuit, and because well-designed integrated circuits are no more difficult to manufacture than individual transistors. Restrictive component tolerances or extra processing steps, however, represent a continuing expense throughout production.

The basic success of Custom Microcircuits lies in Fairchild's ability to optimize circuits by using many transistors and minimizing passive elements such as resistors and capacitors. As cost is proportional to circuit area, the number of functional circuits per unit area must be maximized. Since transistors utilize considerably less area than passive elements, they are preferable in integrated circuit design.

Another important design consideration is the minimization of the number of separate isolations. As each isolated collector requires an isolation area half again as large as a transistor, circuits designed to use common collector transistors require significantly less area.

Fairchild engineers work closely with customers in the design of all custom microcircuits. Following acceptance of a proposed circuit, a breadboard prototype of the circuit is built employing integrated circuit kit parts to simulate the final monolithic device as closely as possible. After thorough testing, Fairchild designs diffusion masks and special test equipment for the custom circuit, and proceeds with full characterization and volume production. The reliability of standard Micrologic® integrated circuits is assured in every custom microcircuit through utilization of the same proven production methods and technology.

The custom integrated circuits which follow are illustrative of Fairchild's ability to design a custom circuit for almost any application.

*Planar is a patented Fairchild Process

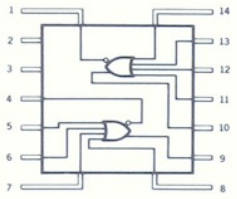
CUSTOM

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1116	CML Gate	50 mV	5 nsec	200 mW	10

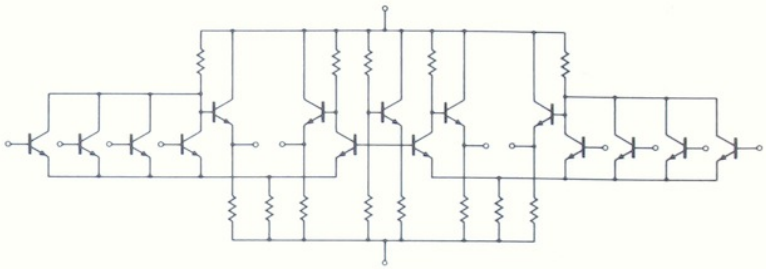
DESCRIPTION

Dual four-input gate with emitter-follower resistors.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±1%	0°C to +75°C	Flat Pack



Logic Diagram



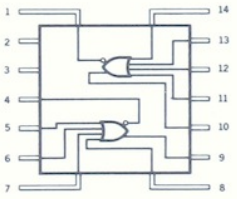
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1117	CML Gate	50 mV	5 nsec	200 mW	10

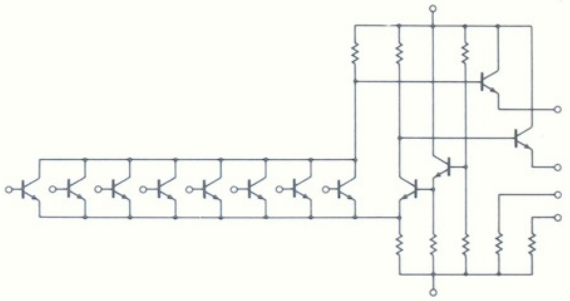
DESCRIPTION

High-speed eight-input Current Mode logic gate.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±1%	0°C to +75°C	Flat Pack



Logic Diagram



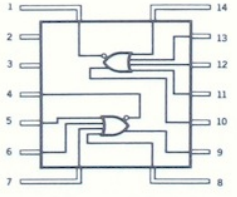
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1126	CML Gate	50 mV	5 nsec	200 mW	10

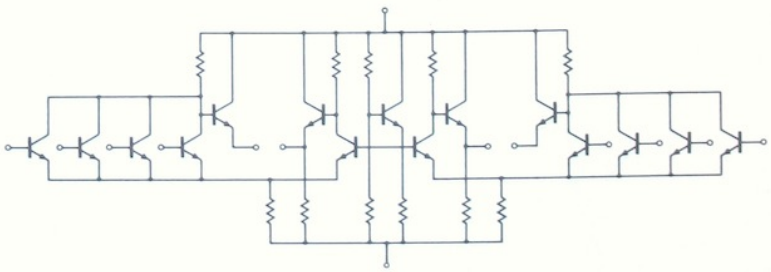
DESCRIPTION

Dual four-input gate without emitter-follower resistors.

SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
5.0 volts ±1%	0°C to +75°C	Flat Pack



Logic Diagram

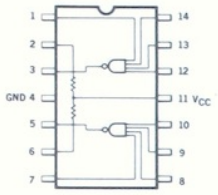


Schematic

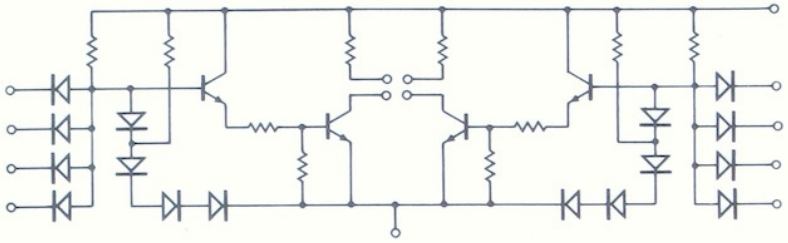
CUSTOM

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1140	Dual Four-Input Gate	750 mV	10 nsec	125 mW/Gate	8

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
High-speed saturated switch for high-speed asynchronous digital computers.	4.0 volts ±10%	+15°C to +55°C	Dual In-Line



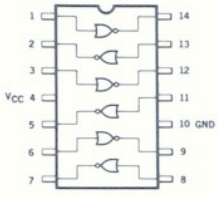
Logic Diagram



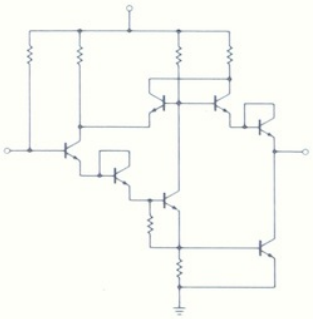
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1155	DT^2L Gate	1.3 volts	25 nsec	150 mW	14

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Hex Inverter.	6.0 volts ±10%	+15°C to +70°C	Dual In-Line



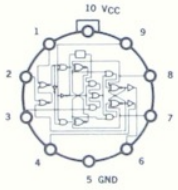
Logic Diagram



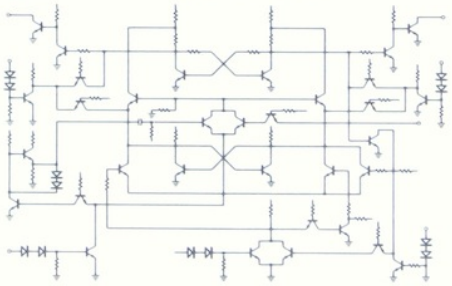
Schematic

PART NUMBER	ELEMENT TYPE	NOISE IMMUNITY (TYP., 25°C)	PROPAGATION DELAY (TYP., 25°C)	POWER DISSIPATION (TYP., 25°C)	FAN-OUT
1169	Dual-Speed DTμL Flip-Flop	1 volt	High-Speed Mode: 15-65 nsec Low-Speed Mode: 85-250 nsec	150 mW	60 mA at V_{sat} =0.5 V max.

DESCRIPTION	SUPPLY VOLTAGE	TEMPERATURE RANGE	PACKAGE
Set-dominant DTμL flip-flop whose output delay can be logically controlled.	4.0 volts ±10%	+5°C to +75°C	TO-5



Logic Diagram



Schematic

TESTING

Fairchild Semiconductor makes the most complete line of integrated circuits in the world. But fabrication is only part of the story. Before these integrated circuits can be shipped, they must be thoroughly tested to assure the customer that they fully meet specifications.

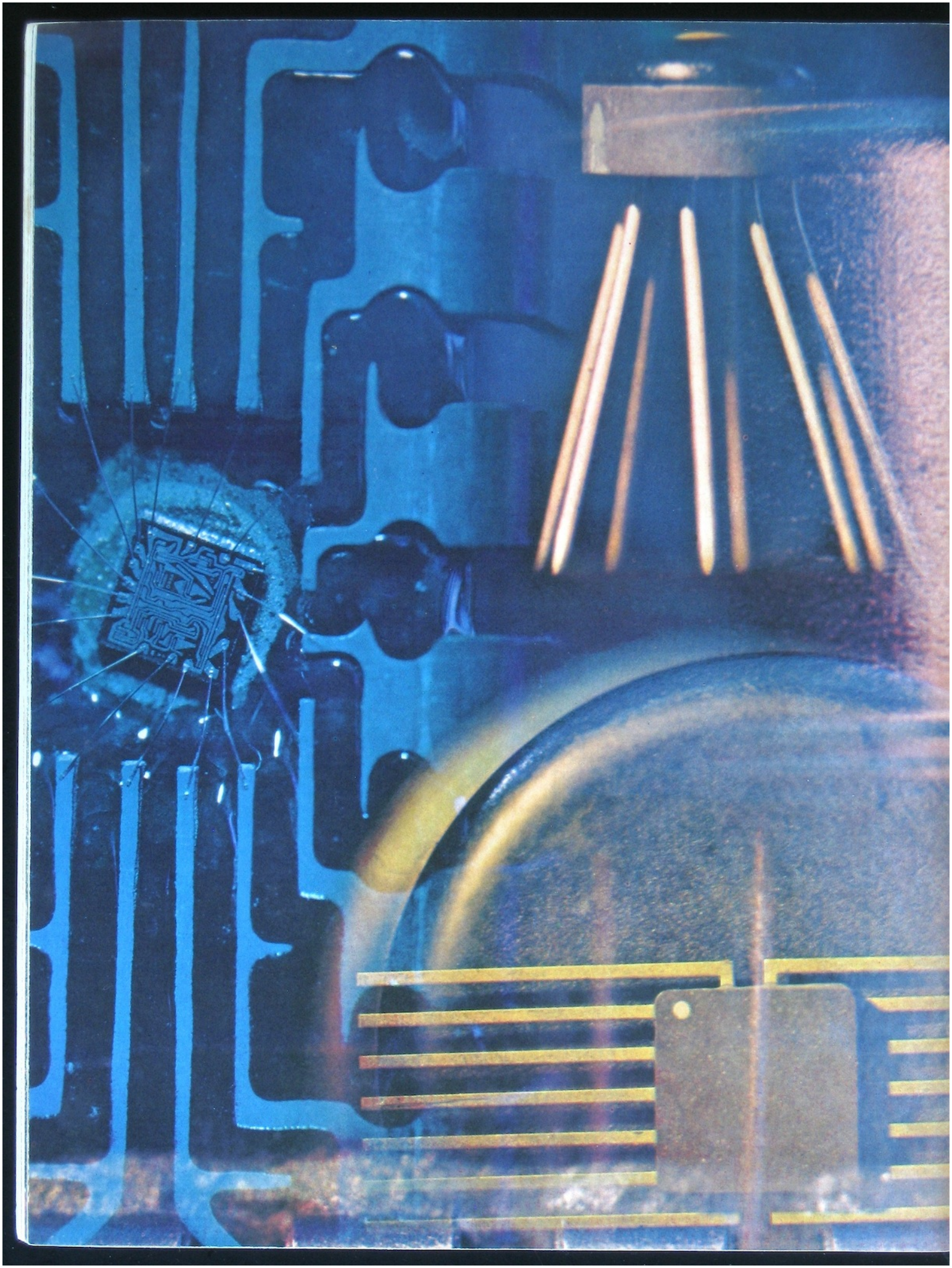
All integrated circuits undergo a series of electrical tests on the Fairchild 4000, the finest automatic tester in the industry. Manufactured by Fairchild Instrumentation, the Series 4000 can conduct as many as 60 tests per second on a device. Instructions are stored in the 4000's magnetic disc storage unit, eliminating the need for manual operation.

The Series 4000's magnetic disc can store information for up to 20 tests (Current, Drive, Sink, Voltage, or Function) on each of its 36 tracks, permitting exhaustive electrical testing of each device in a matter of seconds. Random access capability allows sequence or test changes according to the electrical characteristics of the device being tested. The multiplexing option of the 4000 permits simultaneous testing of two devices, doubling the speed with which circuits can be tested.

In all testing operations, manual handling is kept to a minimum to eliminate the possibility of damage to leads or package. Units are fed into the machine automatically, tested automatically according to programmed instructions, and sorted automatically on a Go/No-Go basis.

Fairchild's long-standing reputation for reliability is due, in part, to this thorough testing with extra care on superior equipment.

With an eye to the future, Fairchild Instrumentation recently announced the Series 8000 tester, a system designed to perform functional logic tests on complex digital circuits such as printed circuit cards, potted modules, integrated circuits, thin-film circuits, multi-chip circuits, complex arrays, and system subassemblies. The Series 8000's great speed - up to 1000 tests per second - will ensure the reliable performance of these circuits of the future, already under development at Fairchild's Research and Development Laboratories, and help maintain Fairchild's unquestioned position as the leader in integrated circuit technology.



PACKAGING

Fairchild Semiconductor offers the widest choice of packages in the industry. Almost all Fairchild microcircuits are available in several package configurations, each designed to meet a particular customer need.

The standard TO-5 package provides the most economical assembly for Linear, Custom, and RTL-type circuits where the circuit termination requirements do not exceed 10. In addition to the conventional metal can versions of the TO-5, Fairchild manufactures an epoxy equivalent; several RTμL circuits are available in this package at a considerable savings. The epoxy packages are intended primarily for systems in the Industrial and Consumer categories where environmental temperatures are limited.

For high-density systems, the "Cerpak" flat pack is recommended. Fairchild's flat packs, with up to 14 leads, are distinguished from those of other manufacturers in that body material and seal are all-ceramic. Excellent thermal characteristics are a direct result. And, since the non-metallic body will not interfere with any associated circuit conductor on the interconnecting board, considerable design flexibility can be realized.

The Dual In-Line - the most significant contribution to microcircuit packaging in recent years - is a Fairchild concept. Its mechanical design incorporates the ultimate in design balance: thermal resistance is optimum, packaging density can be maximized without economic burden, and the cost of interconnection and attachment typically runs 10% of the cost of similar assembly with flat packs. The Dual In-Line package is fully hermetic, and although designed primarily to meet the economic objective of most Industrial applications, it meets all the environmental requirements imposed by Military systems.

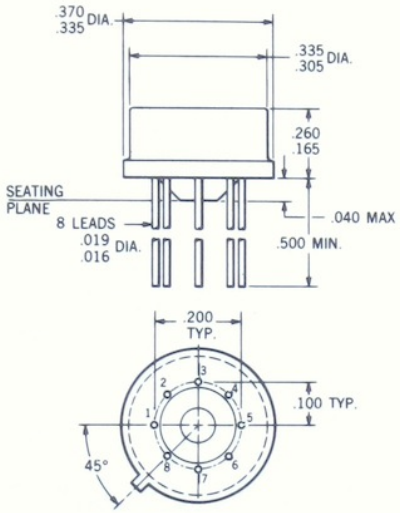
A further refinement in integrated circuit packaging is Fairchild's second generation Dual In-Line, the FAIRPAK™. This new package, using face-down bonding, will become the standard of mechanical configuration for the industry. From the standpoint of economics, it has no equal.

The primary element of cost reduction lies in the implementation of face-down bonding technology for the interconnection of the microcircuit die to the external leads of the package. Applied to a typical 14-lead package, this technique eliminates 28 operator-sensitive welds, replacing them with automatic simultaneous attachment of all microcircuit terminating pads.

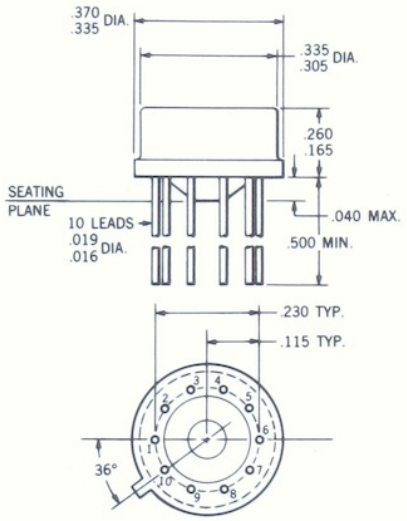
Over and above the obvious economic advantages, this combination of flip-chip technology with the proven superiority of the Dual In-Line results in an appreciably higher degree of reliability. The FAIRPAK meets the economic requirements of Industrial and Consumer customers, yet provides a level of environmental protection consistent with the most stringent requirements of Military applications.

These packages are the most advanced the industry has to offer, and again demonstrate Fairchild's leadership in the introduction of product innovations which increase reliability while lowering costs.

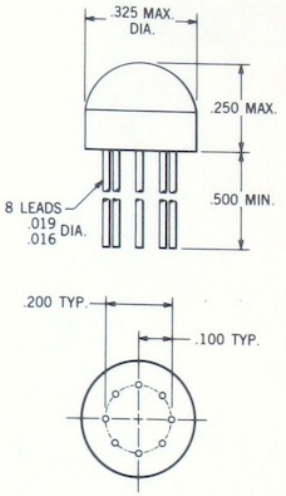
Metal Can Package 8 lead



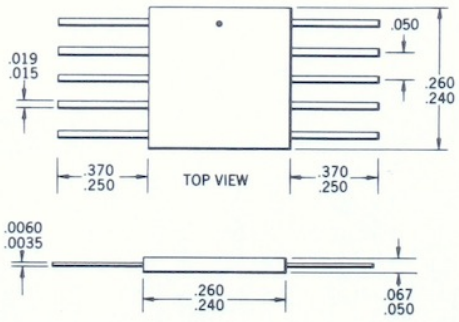
Metal Can Package 10 lead



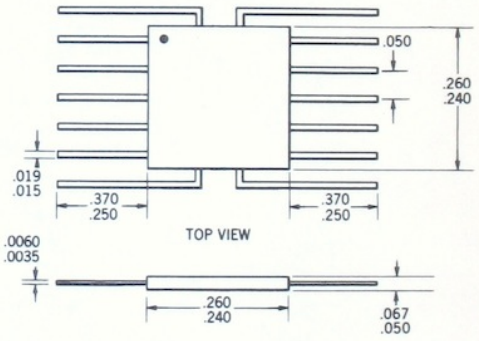
Epoxy Package 8 lead



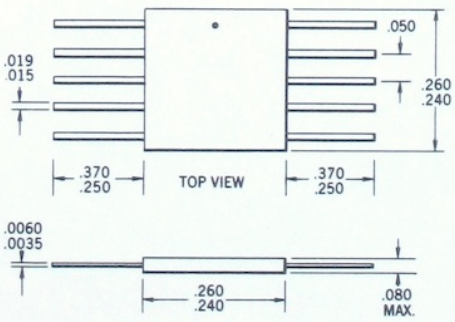
CERPAK I 10 lead
TO-91



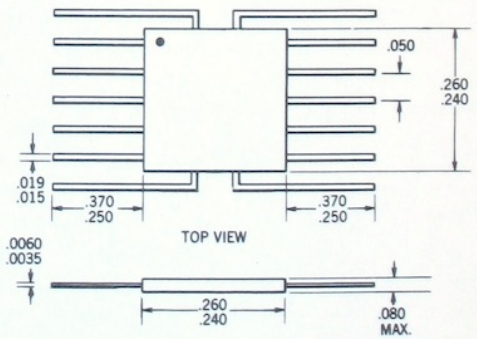
CERPAK I 14 lead
TO-86



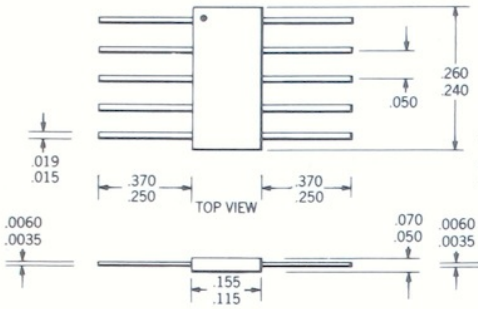
CERPAK II 10 lead



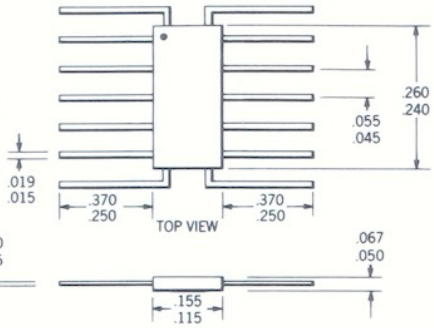
CERPAK II 14 lead



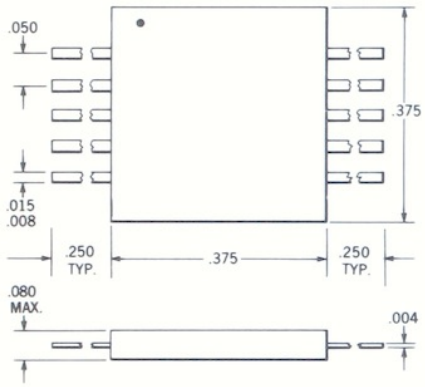
Flat Pack (1/8 x 1/4) 10 lead
TO-89



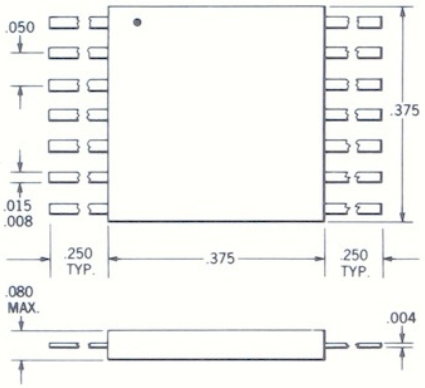
Flat Pack (1/8 x 1/4) 14 lead
TO-84



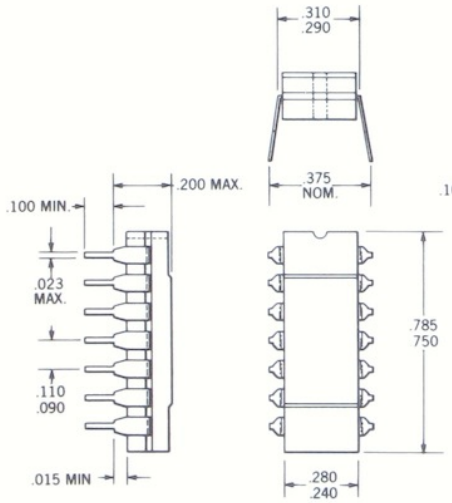
Flat Pack (3/8 x 3/8) 10 lead



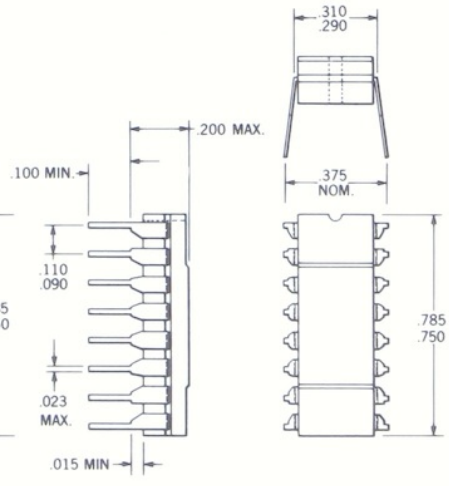
Flat Pack (3/8 x 3/8) 14 lead



Dual In-Line Package 14 lead



Dual In-Line Package 16 lead



PACKAGING CROSS-REFERENCE GUIDE

Flat Pack ■ TO-5 ● Dual In-Line ▲ E = Also available in epoxy package

RTμL	9940 ■ ●	9963 ■ ● ▲	9971 ▲
9900 ■ ● E	**CμL**	**DTμL, Low Power**	**MOS FET's**
9901 ■ ●	9958 ● ▲	9040 ■ ▲	3400 ■
9902 ■ ●	9959 ▲	9041 ■ ▲	3700 ■
9903 ■ ●	9960 ▲	9042 ■ ▲	**Memory**
9904 ■ ●	9989 ▲	**DTL, Other**	9030 ▲
9905 ■ ●	**TTμL**	SE101 ■ ●	9032 ▲
9906 ■ ●	9000 ■ ▲	SE102 ■ ●	9033 ▲
9907 ■ ●	9001 ■ ▲	SE105 ■ ●	1128 ●
9914 ■ ● E	9002 ■ ▲	SE110 ■ ●	**Linear**
9915 ■ ●	9003 ■ ▲	SE115 ■ ●	7703 ■ ● E
9923 ● E	9004 ■ ▲	SE124 ■ ●	7709 ■ ●
9926 ■ ●	9005 ■ ▲	SE150 ■ ●	7710 ■ ●
9927 ■ ●	9007 ■ ▲	SE160 ■ ●	7711 ■ ●
9970 ■ ▲	9009 ■ ▲	CS700 ■ ●	7712 ■ ●
9991 ■ ▲	**DTμL**	CS701 ■ ●	**Hybrid**
9992 ■ ▲	9930 ■ ● ▲	CS704 ■ ●	2001 ■ ●
9993 ■ ▲	9931 ■ ● ▲	CS705 ■ ●	2100 ■ ●
9994 ■ ▲	9932 ■ ● ▲	CS709 ■ ●	2101 ●
9995 ■ ▲	9933 ■ ● ▲	**CTμL**	2510 ■ ●
9996 ■ ▲	9936 ■ ▲	9952 ▲	3000 ■ ●
9997 ▲	9937 ■ ▲	9953 ▲	3001 ●
RTμL, Low Power	9944 ■ ● ▲	9954 ▲	3005 ■ ●
9908 ■ ●	9945 ■ ● ▲	9955 ▲	8080 ■
9909 ■ ●	9946 ■ ● ▲	9956 ▲	9002 ●
9910 ■ ●	9948 ■ ● ▲	9957 ▲	9004 ■ ●
9911 ■ ●	9949 ■ ● ▲	9964 ▲	9006 ■ ●
9912 ■ ●	9950 ■ ● ▲	9965 ▲	9007 ■ ● ▲
9913 ■ ●	9951 ■ ● ▲	9966 ▲	
9921 ■ ●	9961 ■ ● ▲	9967 ▲	
9938 ■ ●	9962 ■ ● ▲	9968 ▲	

PRODUCT CODE EXPLANATION

As Fairchild integrated circuits are available in a wide variety of package configurations and operating temperature ranges, it is essential that customers specify the exact circuit, package, and temperature range desired.

Throughout this brochure, numbers have been given in parentheses after temperature and package specifications. These numbers comprise part of a ten-digit product code used by all Fairchild distributors and field sales offices to identify integrated circuits in a particular package and temperature range. Proper use of this product code, explained in detail below, will ensure the expeditious handling of all customer orders.

A full range RTμL 9900 in a TO-5 package is designated by code number U5D990021X. Breakdown of the code is as follows:

U	5D	9900	21	X
A	B	C	D	E

A. Generic Device Type—U for all monolithics, H for hybrids

B. Package Code (See table below)

C. Basic Circuit Code, as throughout this brochure.

D. Temperature Range (See table below)

E. Currently, this is an open digit for future expanded classification, and is filled with an X.

B. Package Code

Flat Packages

SIZE	MAXIMUM LEADS	NAME	CODE	USED IN
1/4 x 3/16	10	Cerpak	3D	RTμL 9929
1/4 x 3/16	14	Cerpak	3E	
1/4 x 1/4	10	Cerpak	3F	Series 5500, RTμL
1/4 x 1/4	10	Flat Pack	3G	Hybrids
1/4 x 1/4	10	Glass	3H	Linear Circuits
1/4 x 1/4	14	Cerpak	3I	DTμL & TTμL
1/4 x 1/4	14	Flat Pack	3J	Hybrids
1/4 x 3/8	14	Cerpak	3K	
1/4 x 3/8	14	Glass	3L	
Custom			3S	Customer Special Hookups

Plug-in Packages

SIZE	MAXIMUM LEADS	NAME	CODE	USED IN
1/4 x 3/4	14	DIP	6A	CTμL, DTμL, TTμL
1/4 x 3/4	16	DIP	6B	Counting Family

TO-5

MAXIMUM LEADS	PINS USED	PINS SHORTED TO CAN	CODE	USED IN
8	All 8 Pins	None	5A	Hybrids
8	All 8 Pins	4	5B	Low Power RTμL
8	1, 2, 3, 4, 6 & 8 pins	4	5C	RTμL 9903
8	1, 3, 4, 5, 7 & 8 pins	4	5D	RTμL 9900, 9902
10	All 10 Pins	None	5E	Series 5500
10	All 10 Pins	5	5F	DTμL & TTμL
12	All 12 Pins	None	5G	
14	All 14 Pins	None	5H	
Custom			5S	Customer Special Hookups

TO-47

8	All 8 Pins	4	7A
8	1, 3, 4, 5, 7 & 8 Pins	4	7B
Custom			7S

EPOXY

8	All 8 Pins	8A
8	1, 3, 4, 5, 7 & 8 Pins	8B
Custom		8S

D. Temperature Range

Two digits determine the temperature range. The code for a specified range varies from one Micrologic® integrated circuit family to another:

21. RTμL	−55°C to +125°C
22. RTμL	0°C to +100°C
28. All Epoxy	+15°C to +55°C (V_{CC}= +3.6 V)
29. RTμL	0°C to +70°C
31. Linear (μA)	−55°C to +125°C
39. Linear (μA)	0°C to +70°C
51. TTμL, DTμL, LPDTμL	−55°C to +125°C
59. TTμL, DTμL, CμL	0°C to +75°C
59. CTμL	+15°C to +55°C
79. CTμL	+15°C to +55°C

INDEX

PATENT INFORMATION

Leadership in industry is generally evidenced by the contributions a particular company makes in advancing the technology of its field of endeavor. The semiconductor industry is no exception, and Fairchild, as its leader, has developed more critical patented processes than any other integrated circuit producer.

The manufacture of all silicon monolithic circuits requires the use of several of the following U.S. patents - all held by Fairchild Semiconductor.

PATENT NO.	FILING DATE	DESCRIPTION
2981877	7/30/59	The use of a deposited metal interconnection pattern atop a silicon oxide layer on a semiconductor surface to achieve interconnections between regions on opposite sides of P-N junctions which extend to the wafer surface.
3025589	5/1/59	Planar process - the fundamental process used in the manufacture of integrated circuits, by which all critical junctions are formed under a passivated layer of silicon oxide, protecting them from any environmental contaminants.
3064167	5/1/59	Planar construction of transistors and integrated circuits.
3108359	6/30/59	Double-diffusion process, utilizing photo-etched contacts.
3117260	9/11/59	The use of islands of one conductivity type diffused into a wafer of extrinsic semiconductor material of the opposite conductivity type for isolation of semiconductor devices within each of the islands from devices in the other islands.
3150299	9/11/59	Intrinsic material isolation.
3158788	8/15/60	Dielectric isolation structure.
3184347	7/19/62	Gold-doping technique to improve transistor switching time.
3199002	4/17/61	Diffused lead crossovers - the basic lead-crossing technique used in all monolithic circuits.
3260902	10/5/62	Buried-layer epitaxial structure.

Fairchild Semiconductor has licensed several manufacturers permitting them to use certain Fairchild patents and processes.

LIST OF PHOTOGRAPHS

FAIRCHILD
SEMICONDUCTOR

A Division of Fairchild Camera and Instrument Corporation
313 Fairchild Drive, Mountain View, Calif. 94040
(415) 962-5011 / TWX: 910-379-6435 / 2310-109-46 / 50M / Printed in U.S.A.

Fairchild Semiconductor Integrated Circuits
1966

This Digitised Version
2023 Nov

Digitised via manual photography with Canon A590 camera in Manual mode.
Post processing and PDF'd using Apple Preview 5.5.3.

Photographs originally 2448 • 3264.

White pages photographed with some overexposure, Auto-Leveled.
Some White-level decrease to brighten and clean white background. Minor Sharpness and Tint increment on some.

Colour-photo pages photographed with underexposure then brightness increased with Auto-Level. Some White-level increase. Minor Sharpness increment.

/bhilpert