

Univac Core Memory Module

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Section: Title & Notes

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DOCUMENT LOG

- Based on reverse engineering of unit with Serial Numbers 2311, 1706.
Unit has date stamps of: JUN 7 1971, 7128, 7129.
- 2024 Apr: This drawing / bhilpert.
- 2026 Apr: Some reorganisation & clarifications / bh.

DESCRIPTION

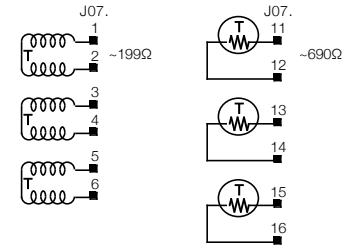
Array size

- The module is a planar array with one fold in the horizontal.
There are 160 sense-arrays in an (8+12) • 8 matrix.
- Each sense-array : $64 * 64 = 4096$ cores
- Total number of physical cores (bits) : $160 * 4096 = 655,360$ (81,920 bytes equivalent)
- 1 column of 8 bit planes is not used (sense pairs are not connected in connector).
Cores in use: $(160-8)*4096 = 622,592$ (77,824 bytes equivalent)

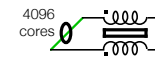
Origin

Some investigation suggests this is likely a module from a UNIVAC 1108. The UNIVAC 1100 family is based on 36-bit words. The parameters above would fit for a 2-1/2D array format of 32,768 18-bit half-words with parity bit.

Temperature Sensors



Each Sense-Array



Sense-Array Pair Outputs

J23,25,26,
27::30

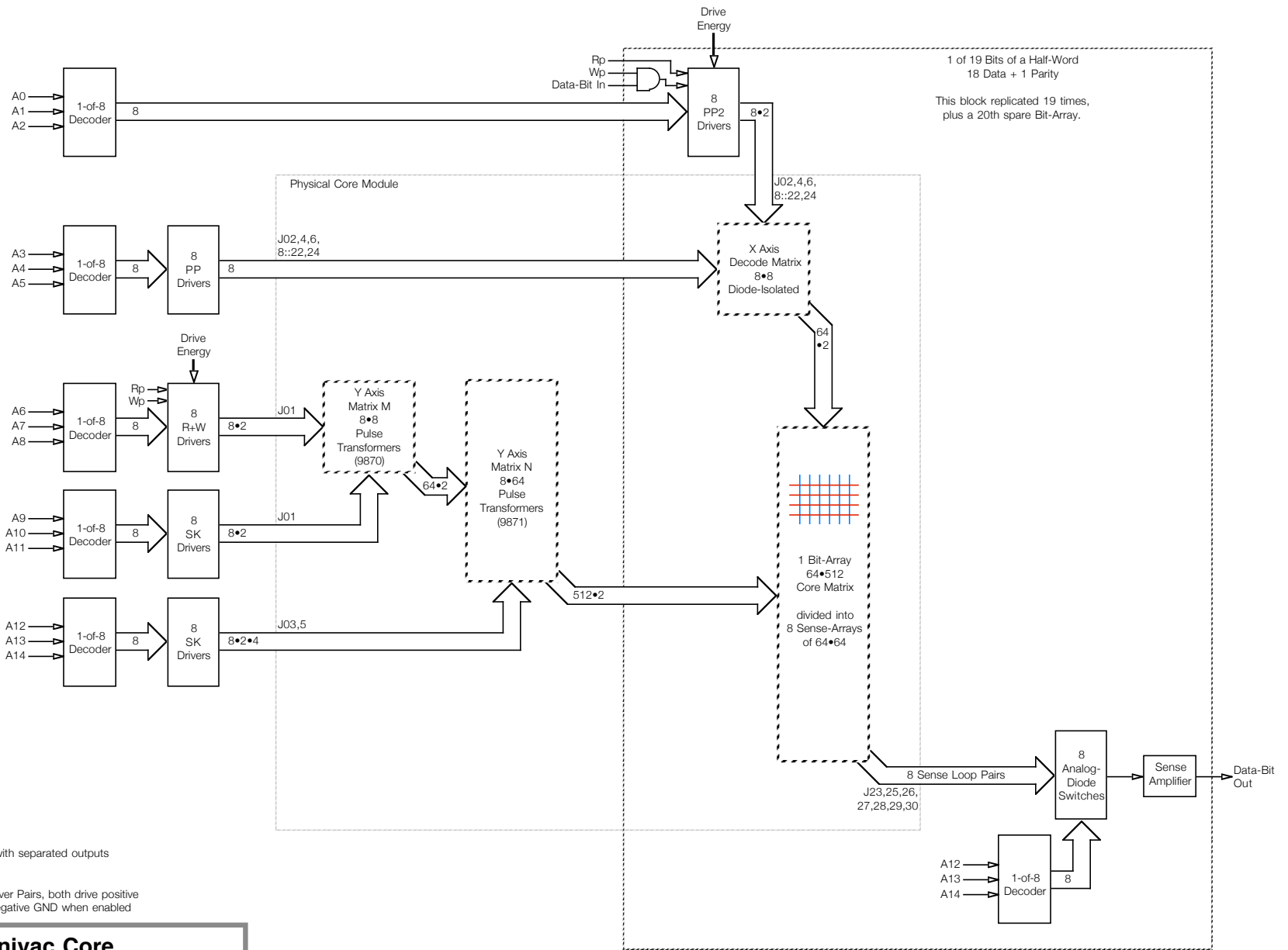
	A	D	B
C	03b	05b	07b
01b	E	J	F
H	03y	05y	07y
01y	K	N	L
M	02b	04b	06b
00b	P	R	
S	02y	04y	06y
00y	U	V	
W	13b	15b	17b
11b	Y	Z	
a	13y	15y	17y
11y	c	d	
e	12b	16b	
10b	h	j	
k	12y	16y	
10y	n	p	
r	t		
21b	s	25b	u
v	23b	27b	
21y	x	25y	y
z	23y	27y	
20b	BB	24b	CC
DD	22b	26b	
20y	FF	24y	HH
	22y	26y	

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32 Decoder-Driver Boards implementing Matrices M & N.
Each board drives 16 Y-Axis wires.

- X-Axis Wire (Independent Axis)
- Y-Axis Wire (Shared Axis)



A_n = Address Bit

R_p = Read pulse
W_p = Write pulse

PP2 = Push-Pull driver with separated outputs
PP = Push-Pull driver

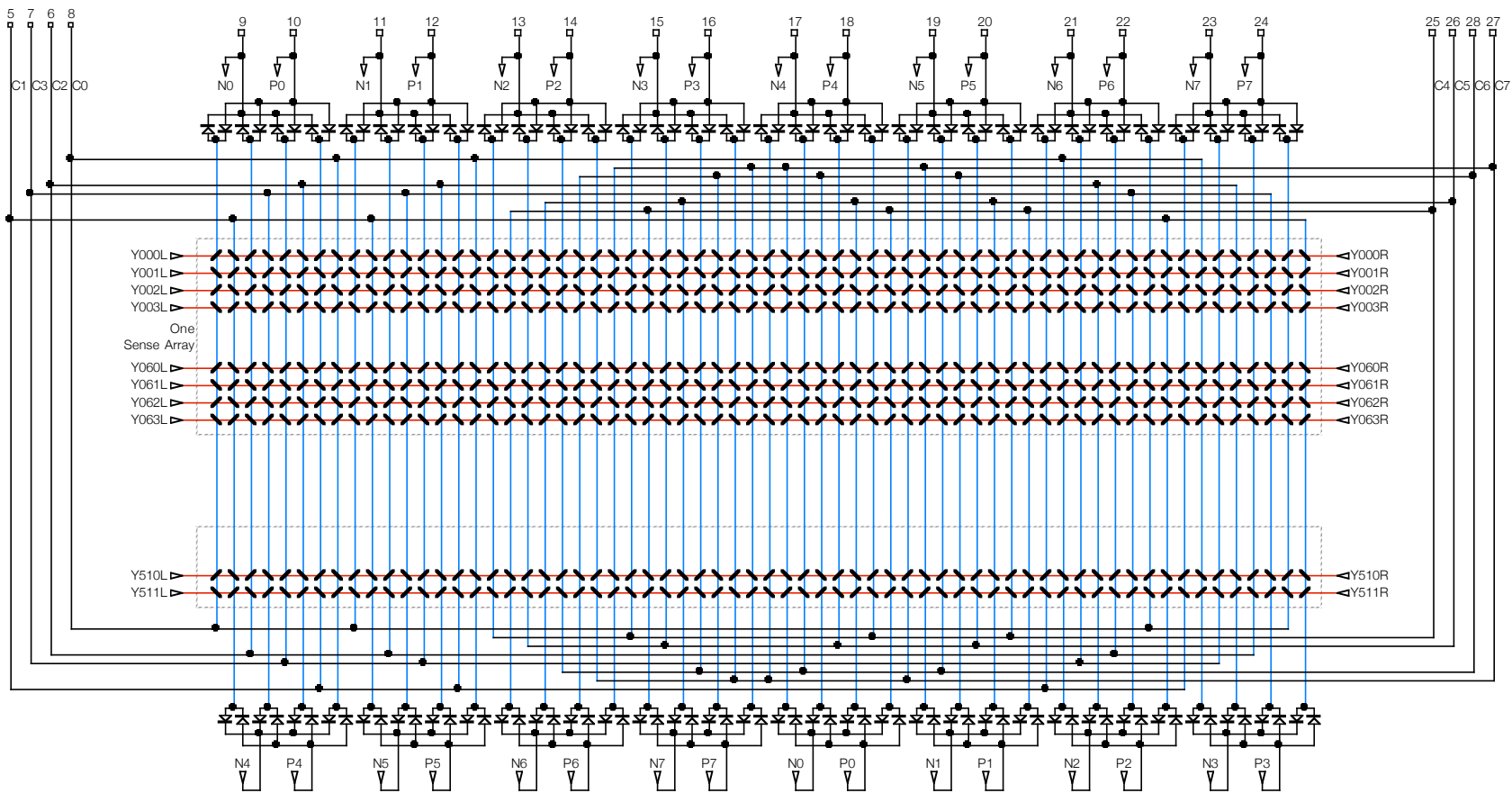
R+W = Read & Write Driver Pairs, both drive positive
SK = Driver shunts to negative GND when enabled

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Section: Block Diagram

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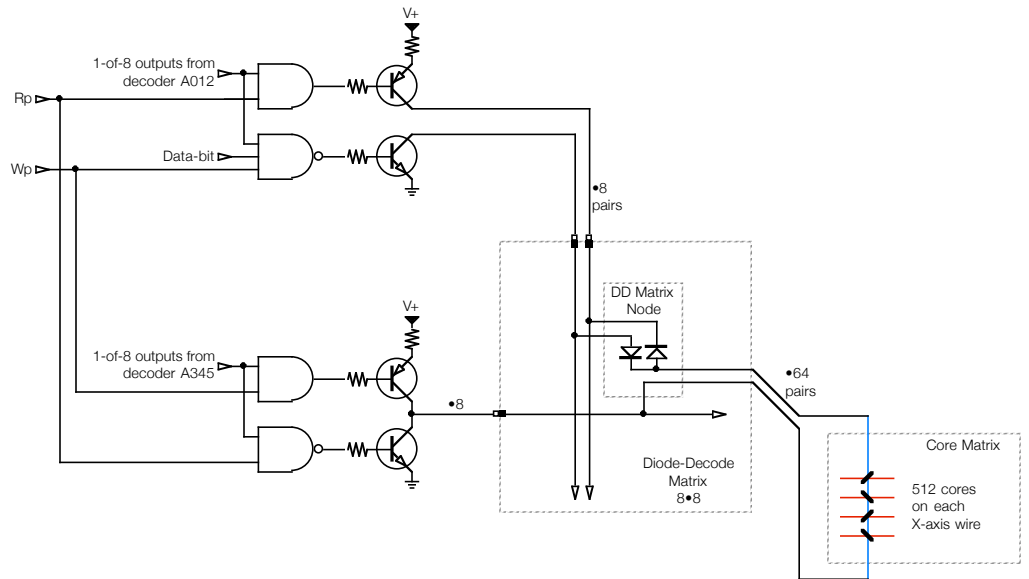
Rendition: May 11, 2026



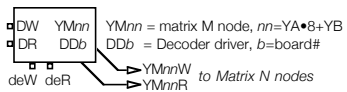
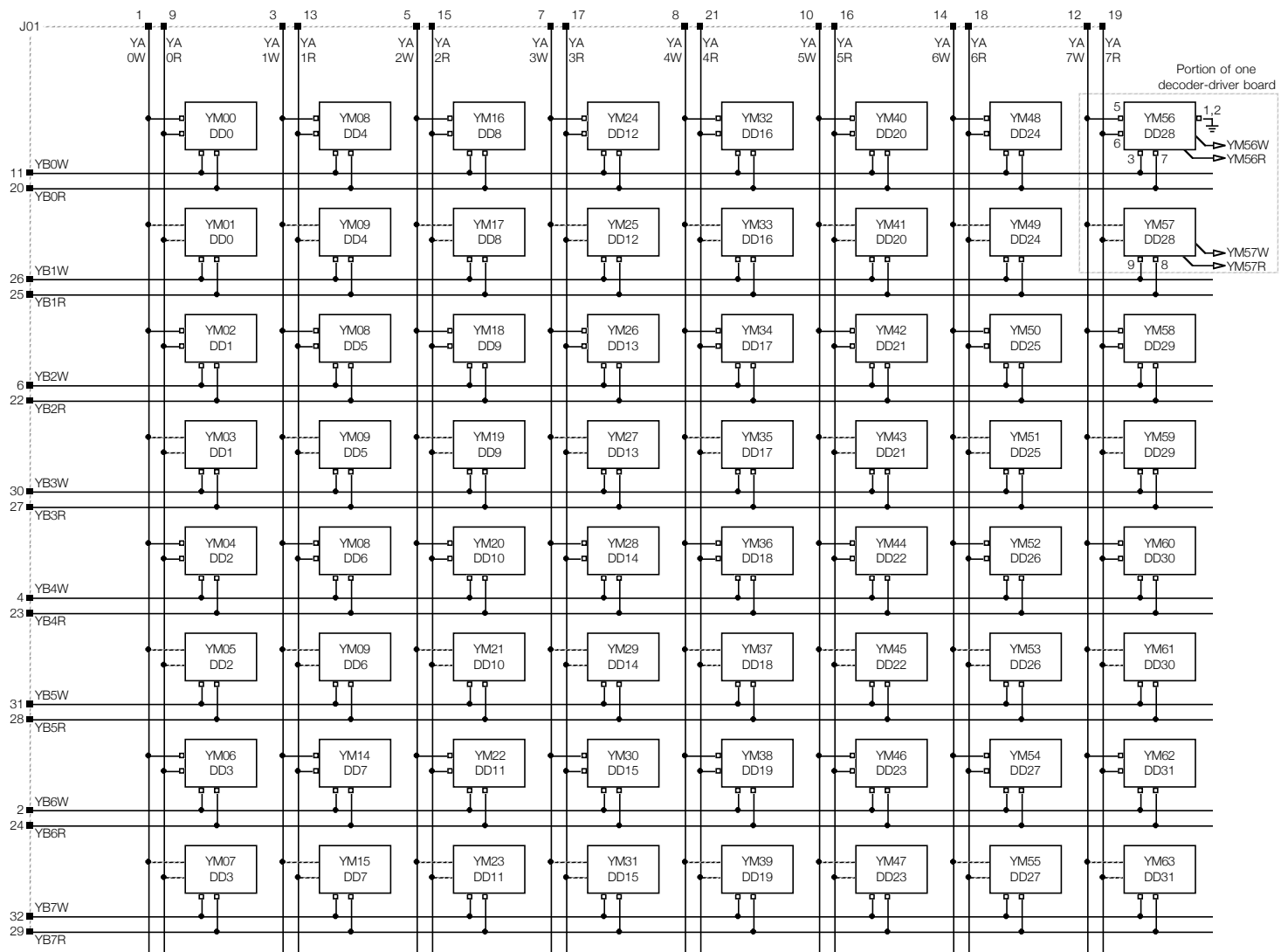
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 Section: X-Axis of each Bit-Array
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J09::22,24

x	x	C1	C3	N0	N1	N2	N3	N4	N5	N6	N7	C4	C7	x	x
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32
x	x	C2	C0	P0	P1	P2	P3	P4	P5	P6	P7	C5	C6	x	x

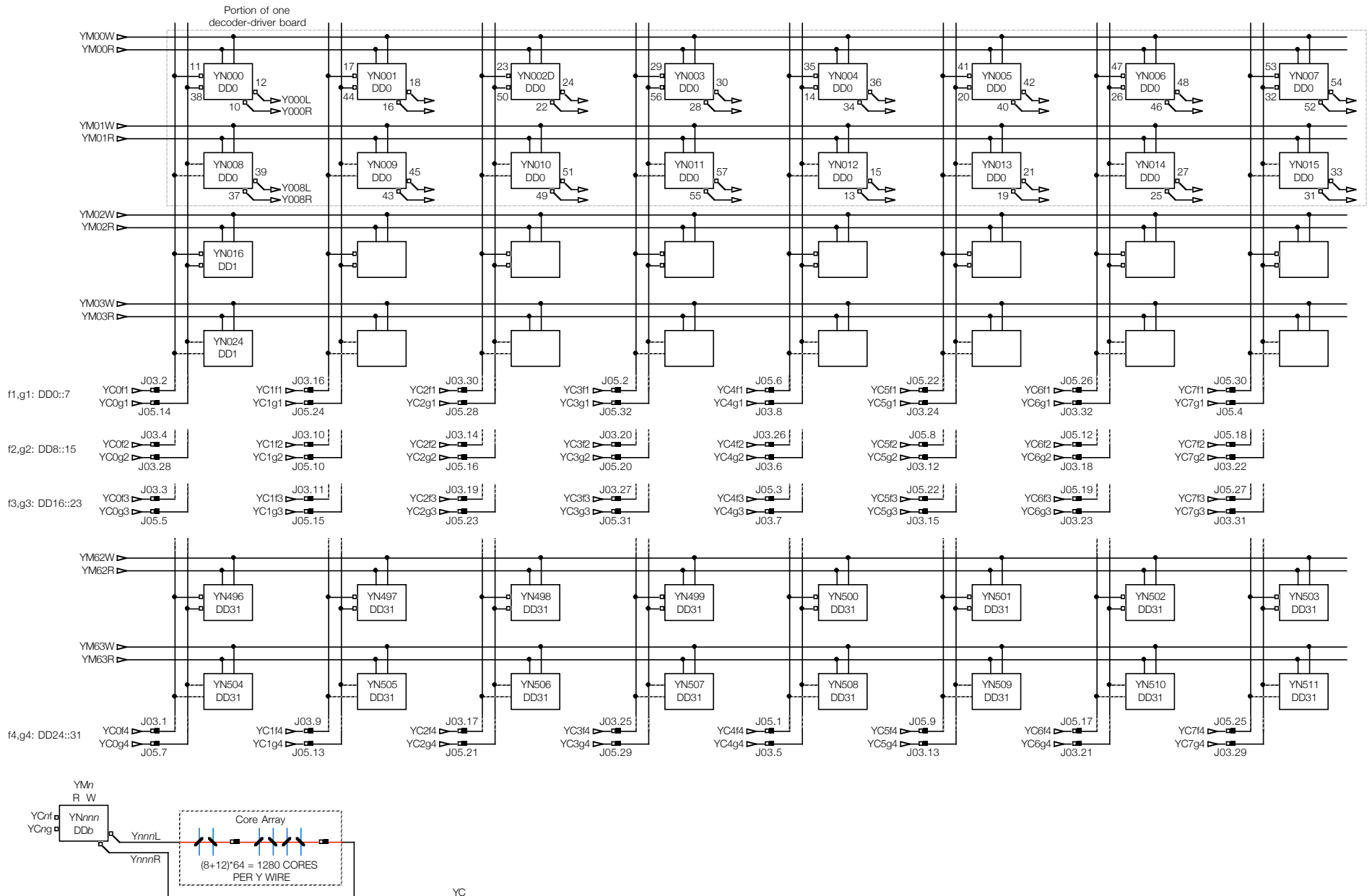


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 Section: Y-Axis Organisation (8•8 Matrix M)
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	YA0	YA1	YA2	YA3	YA0	YA0	YA1	YA2	YA3	YA7	YA4	YB4	YB1	YB3	YB7	YB5
J01	W	W	W	W	R	W	R	R	R	R	R	R	R	R	R	W
	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31
	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32
	YB6	YB4	YB2	YA4	YA5	YA7	YA6	YA5	YA6	YB0	YB2	YB6	YB1	YB5	YB3	YB7
J01	W	W	W	W	W	W	W	R	R	R	R	R	W	R	W	W

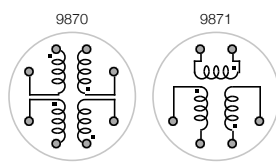
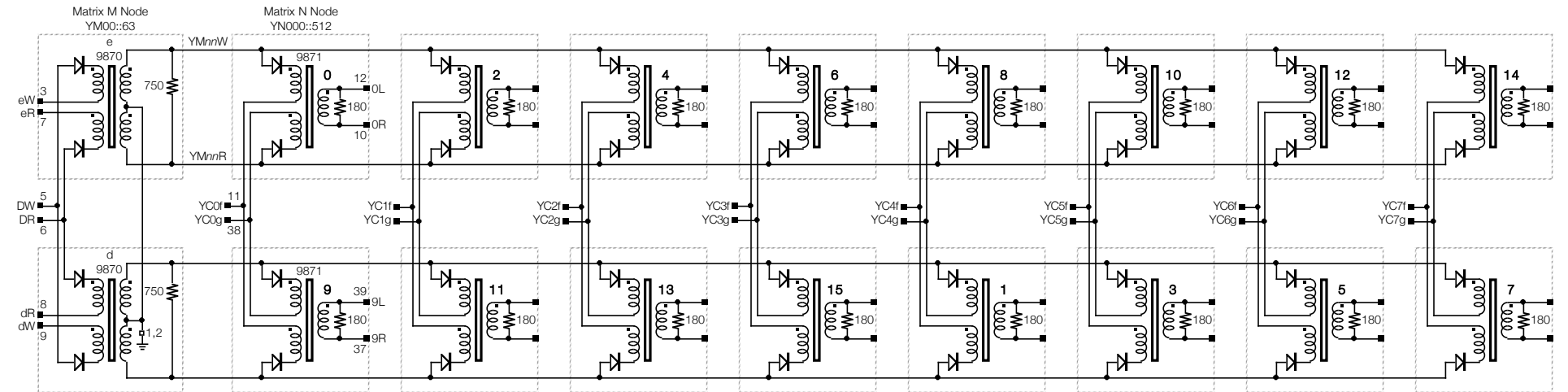
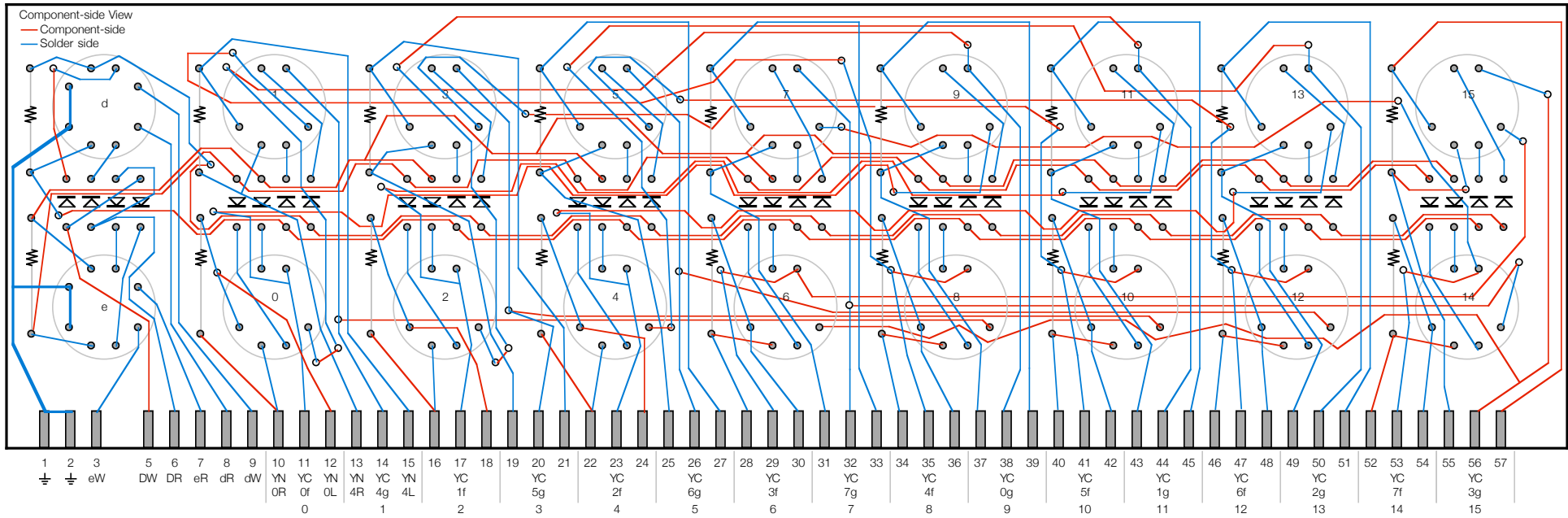


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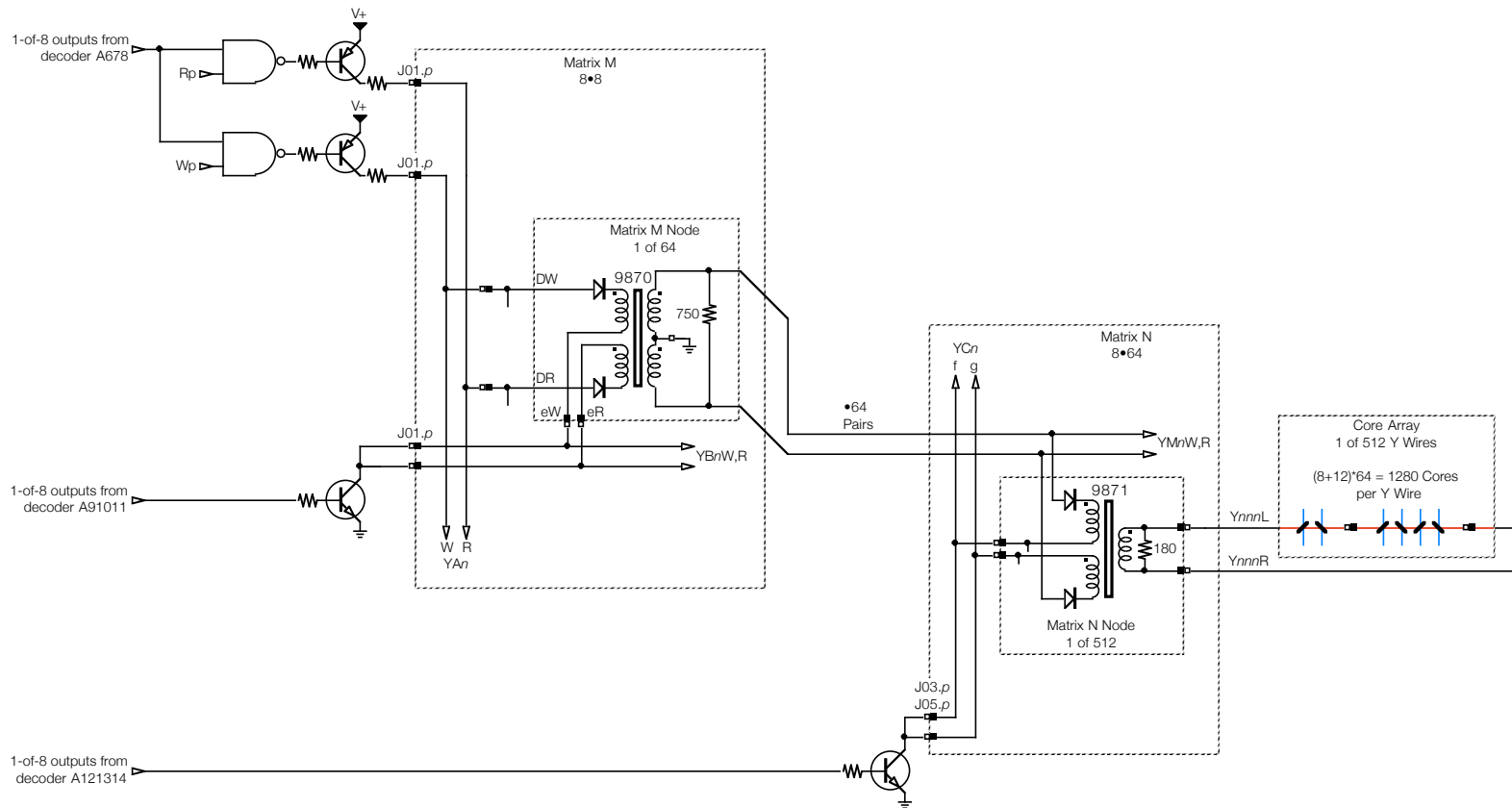
Section: Y-Axis Organisation (8*64 Matrix N)
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		YC																J05															
		0f4	0f3	4g4	4g3	1f4	1f3	5g4	5g3	2f4	2f3	6g4	6g3	3f4	3f3	7g4	7g3	4f4	4f3	0g4	0g3	5f4	5f3	1g4	1g3	6f4	6f3	2g4	2g3	7f4	7f3	3g4	3g3
J03	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	
	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	
		0f1	0f2	4g2	4g1	1f2	1f1	5g2	5g1	2f2	2f1	6g2	6g1	3f2	3f1	7g2	7g1	4f1	4f2	0g1	0g2	5f1	5f2	1g1	1g2	6f1	6f2	2g1	2g2	7f1	7f2	3g1	3g2

(* not on expected connector)



Out	Addr	Out	Addr L	Out	Addr L	Addr R	Out	Addr L	Addr R
0	: 0	8	: 4	0	: 0	9	8	: 8	1
1	: 12	9	: 8	1	: 1	8	9	: 9	0
2	: 1	10	: 5	2	: 2	11	10	: 10	3
3	: 13	11	: 9	3	: 3	10	11	: 11	2
4	: 2	12	: 6	4	: 4	13	12	: 12	5
5	: 14	13	: 10	5	: 5	12	13	: 13	4
6	: 3	14	: 7	6	: 6	15	14	: 14	7
7	: 15	15	: 11	7	: 7	14	15	: 15	6



Y-AXIS NOMENCLATURE

- YAn 1-of-8 signals pairs decoded from 3 bits of address, driving one axis of the M matrix.
- YBn 1-of-8 signals pairs decoded from 3 bits of address, driving one axis of the M matrix.
- YCn 1-of-8 signal pairs decoded from 3 bits of address, driving one axis of the N matrix.
- YMnW,R 1-of-64 R/W signals pairs from the nodes of the M matrix, driving one axis of the N matrix.
- YnnnL,R 1-of-512 left/right signal pairs from nodes of the N matrix, driving the Y-axis of the core array.
- YCnf1,2,3,4 YCnf & g are left & right enable lines for the 8-wide axis of Matrix N.
- YCng1,2,3,4 However, there are transpositions between L & R and the address, that is, the f & g lines carry both read/write & address information. These lines are each split into 4 segments, which may have been just due to driver limitations.

NOTE:

The driver diagrams are intended only to present the effective electrical circuit involved in driving the X or Y axis. The actual driving circuit details are not known. In practice, the YBd,e and YCa,b drive lines - shown here paired to the same driver - were likely separated and driven in a manner to effect some transposition in the addressing.

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