Canon 161 Calculator

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Notes

- Gate symbols and signal names are presented in accordance with:
  logic 0 = 0V, GND, E
  logic 1 = –10V
- The symol Nbbcp denotes a physical connector pin. *bb*=board, *c*=connector, and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- ⟶ ⟶ Arrows indicate direction of signal or energy flow.
- The symbol ▼ with no label denotes –10V.
- The symbol ⏃ with no label denotes +10V.
- Capacitance in microfarads unless otherwise indicated.
- See the associated Theory of Operation document.
  A blue dot ▪ in these drawings indicates the associated element is referenced by name in that document.
- Display lamps are 12V / 70mA (based on measurement).
- These drawings based on unit with Serial No. 700369.

Revision Log

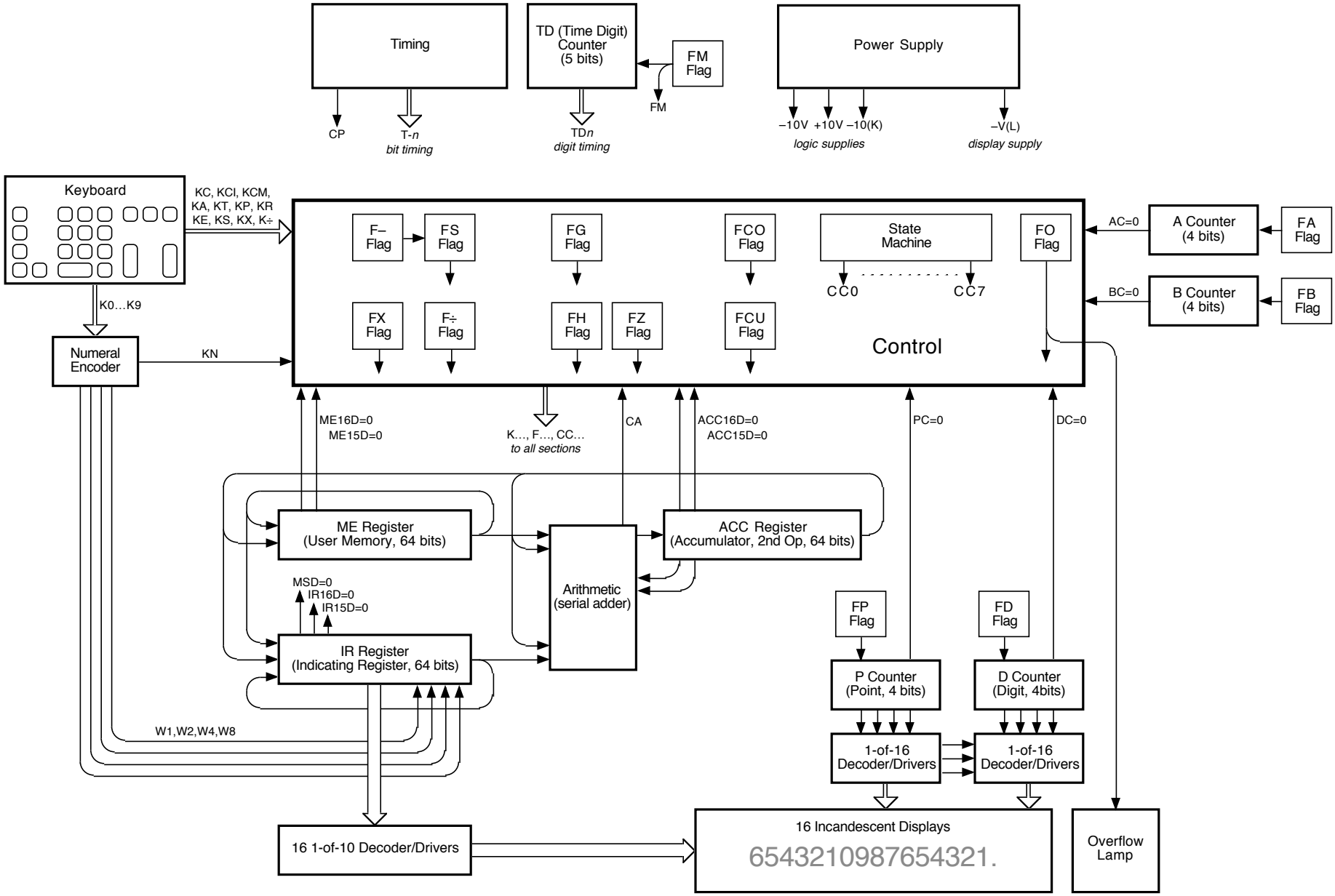
- 2000 Dec: Initial drawing / bhilpert.
- 2019 Jan: Format revisions / bh.
- 2021 Nov:
  - Corrections re MJ: Timing diagram scale corrected, nK(E+S)-->K(E+S) at B Counter.
  - Monostable diagrams reorganised / bh.
  - Initial version of State Diagram added.
  - Numeral-entry & addition procedure descriptions added.
  - Corrections to F÷, FG, FZ flags: JK input sources were swapped.
  - Correction to gate 38A20: F÷ corrected to nF÷.
- 2021 Dec:
  - Flags reorganised.
  - Correction to signal direction between 36A34 & 36O20.
  - DP alignment description added.
  - Gate names corrected:
    30O1 => 34O9
    30B5 => 34B3
    31V5 => 34V12
    34A45::49 => 37A45::49
    34A47 => 36A47
    A4 => 32A11
    36B6 => 35B8
    37A14 => 34A30

Signal Names

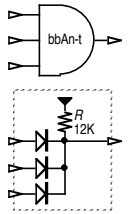
Signal names are based on the labels on the printed circuit boards.

Section	Signal	Description
Timing	CP	Master clock.
	T-…	Bit timing (4 bits constitutes a digit).
	TD…	Digit timing to count out a number cycle. Clocking of the TD counter is controlled by FM.
	FL	TD16 delayed one clock period. Used in part to trigger state transitions at the end of number cycles.
Keyboard	K…	Keyboard signals.
	W1,W2,W4,W8	Signals from the keyboard numeral encoder to the IR register.
Control	CC0::CC7	The states of the state machine.
	F…	Flag (single-bit) registers.
	F–	A subtract operation is pending or active.
	FS	DIrects Arithmetic to perform subtract rather than add.
	FX	A multiply operation is pending or active.
	F÷	A divide operation is pending or active.
	FO	Overflow / error flag.
	FG	- In CC4 of multiplication, indicates shift period of final digit to adjust product. - Indicates divide pending while dividend is shifted up. - In division, transfers termination indication in CC4.
	FH	- Used to catch an occurrence of AC=0 during CC1 for DP alignment.
	FZ	- In CC3 of multiplication, indicates to add multiplicand digits of IR to ACC. - In CC4 of multiplication, indicates to shift multiplicand digits of IR. - In division, records termination event from CC3.
	FCO	Sign from last operation-result arithmetic (out of CC3).
	FCU	Sign from last totalising arithmetic (out of CC6).
	FM	Controls clocking of the registers and TD,A,B,D & P Counters.
	FA	Controls clocking of the A Counter.
	FB	Controls clocking of the B Counter.
	FD	Controls clocking of the D Counter.
	FP	Controls clocking of the P Counter.
IR Register	IR…	Indicating Register. The operand being displayed.
	IR	Bit stream output.
	IR15D=0	
	IR16D=0	
ACC Register	ACC…	Accumulator, contains the second operand. Arithmetic is incorporated in this register.
	ACC	Bit stream output.
	ACC15D=0	
	ACC16D=0	
ME Register	ME…	User memory controlled by the A switch and T key.
	ME	Bit stream output.
	ME15D=0	
	ME16D=0	
P Counter	PC…	Point Counter. Holds the position of the displayed decimal point.
	PC=0	
D Counter	DC…	Digit-Mark Counter. Holds the position of the multiply digit marker.
	DC=0	
A Counter	AC…	Counter to calculate the difference in DP positions between IR and ACC.
	AC=0	
B Counter	BC…	Counter to recover the DP position of a recalled operand.
	BC=0	

- A lowercase “n” in a signal name indicates the logical NOT operation.

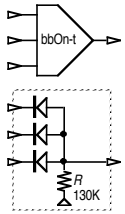

Timing
TD (Time Digit) Counter (5 bits)
FM Flag
FM
Power Supply
CP
T-n
bit timing
TDn
digit timing
–10V +10V –10(K)
logic supplies
–V(L)
display supply
Keyboard
KC, KCl, KCM, KA, KT, KP, KR KE, KS, KX, K÷
K0…K9
Numeral Encoder
KN
F– Flag
FS Flag
FG Flag
FCO Flag
State Machine
FO Flag
CC0
CC7
FX Flag
F÷ Flag
FH Flag
FZ Flag
FCU Flag
Control
AC=0
A Counter (4 bits)
FA Flag
BC=0
B Counter (4 bits)
FB Flag
ME16D=0
ME15D=0
K..., F..., CC...
to all sections
CA
ACC16D=0
ACC15D=0
PC=0
DC=0
ME Register (User Memory, 64 bits)
ACC Register (Accumulator, 2nd Op, 64 bits)
Arithmetic (serial adder)
MSD=0
IR16D=0
IR15D=0
IR Register (Indicating Register, 64 bits)
FP Flag
FD Flag
P Counter (Point, 4 bits)
D Counter (Digit, 4bits)
W1,W2,W4,W8
1-of-16 Decoder/Drivers
1-of-16 Decoder/Drivers
16 1-of-10 Decoder/Drivers
16 Incandescent Displays
6543210987654321.
Overflow Lamp

AND Gates



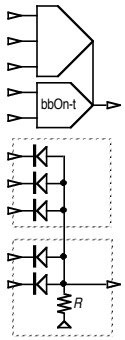
t	R
0	3.9K
1	4.7K
2	5.6K

OR Gates

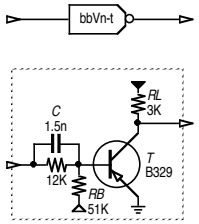


t	R
0	4.7K
1	5.6K
2	8.2K
4	33K
6	300K
7	330K

Distributed OR gate.

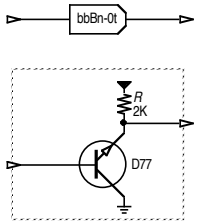


Inverters

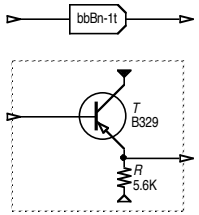


t	Variations
0	C=none
1	
2	C=none RL=1.8K
3	RL=1.8K
4	C=none RL=820
5	RL=820
6	C=none T=A538
7	C=1nF T=A538
8	C=none RL=1.8K T=A538
9	C=1nF RB=68K T=A538

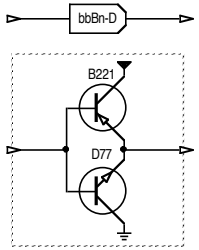
Buffers



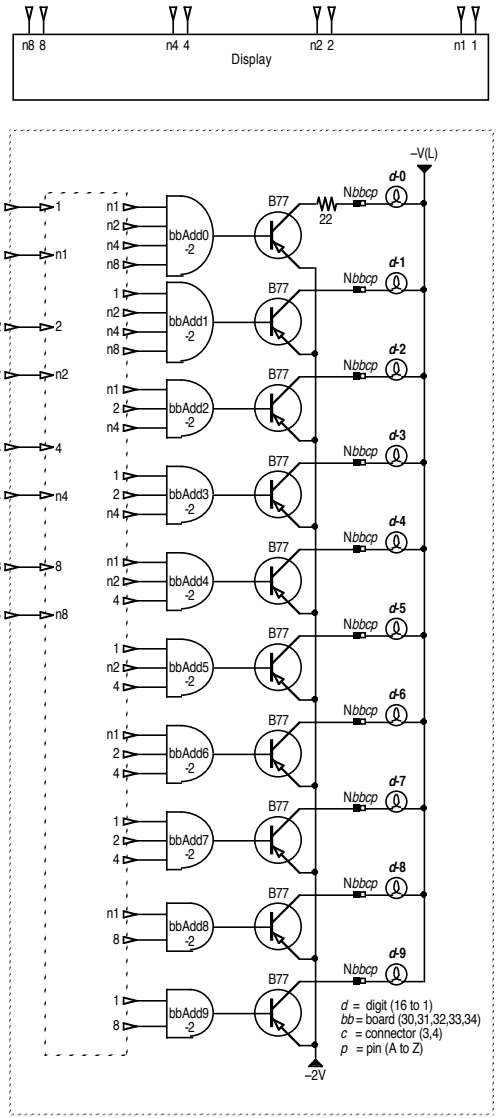
0t	Variations
01	R=1K



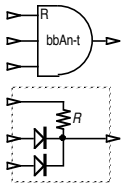
1t	Variations
10	
11	T=A538
12	T=B222
13	R=3K
14	R=3K T=B222
15	R=2K T=B222
16	R=2K B=221
17	R=5.6K to E



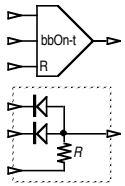
Display



AND gate with controlled pull-up.
Used in marker decoders.



OR gate with controlled pull-down.
Used in marker decoders.

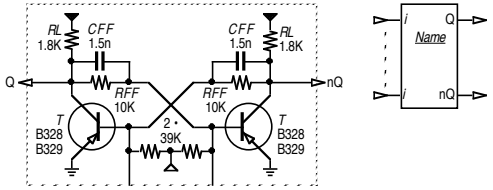


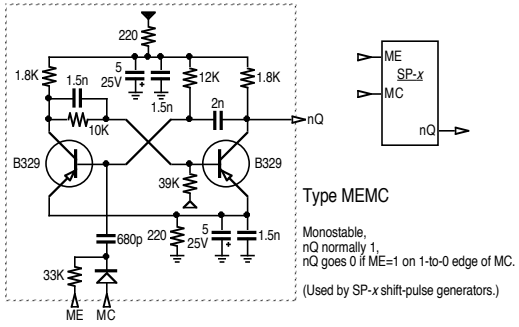
Notes

- Gates are identified with a label of the form:
  bbgn-t
  where:
  bb = board [30-40]
  g = gate type (And,Or,inVerter,Buffer)
  n = enumeration
  t = type variation (see tables above)

- Logic 0 = 0V, GND, E
  Logic 1 = –10V

Flip-Flops

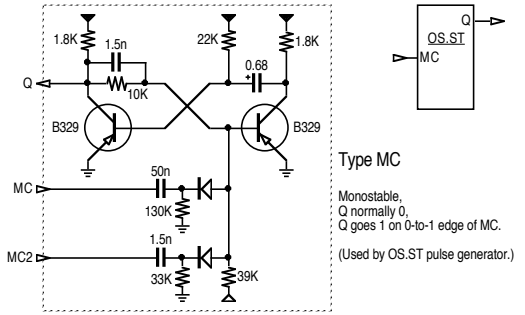




Type MEMC

Monostable,
nQ normally 1,
nQ goes 0 if ME=1 on 1-to-0 edge of MC.

(Used by SP-*x* shift-pulse generators.)

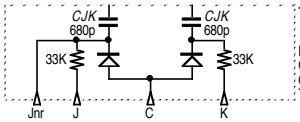


Type MC

Monostable,
Q normally 0,
Q goes 1 on 0-to-1 edge of MC.

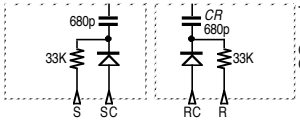
(Used by OS.ST pulse generator.)

Flip-Flop Input Options



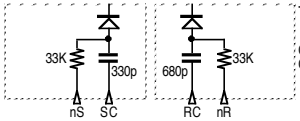
Type JK

No change if J=0 and K=0.
Q goes 1 if J=1 and K=0 on 1-to-0 edge of C.
Q goes 0 if J=0 and K=1 on 1-to-0 edge of C.
Toggle Q if J=1 and K=1 on 1-to-0 edge of C.



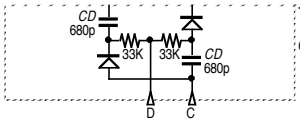
Types S and R

Q goes 1 if S=1 on 1-to-0 edge of SC.
Q goes 0 if R=1 on 1-to-0 edge of RC.



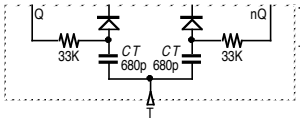
Types nS and nR

Q goes 1 if nS=0 on 1-to-0 edge of SC.
Q goes 0 if nR=0 on 1-to-0 edge of RC.



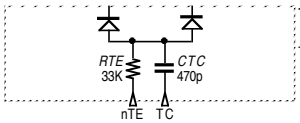
Type D

Q follows D on 1-to-0 edge of C.



Type T

Toggle Q on 1-to-0 edge of T.



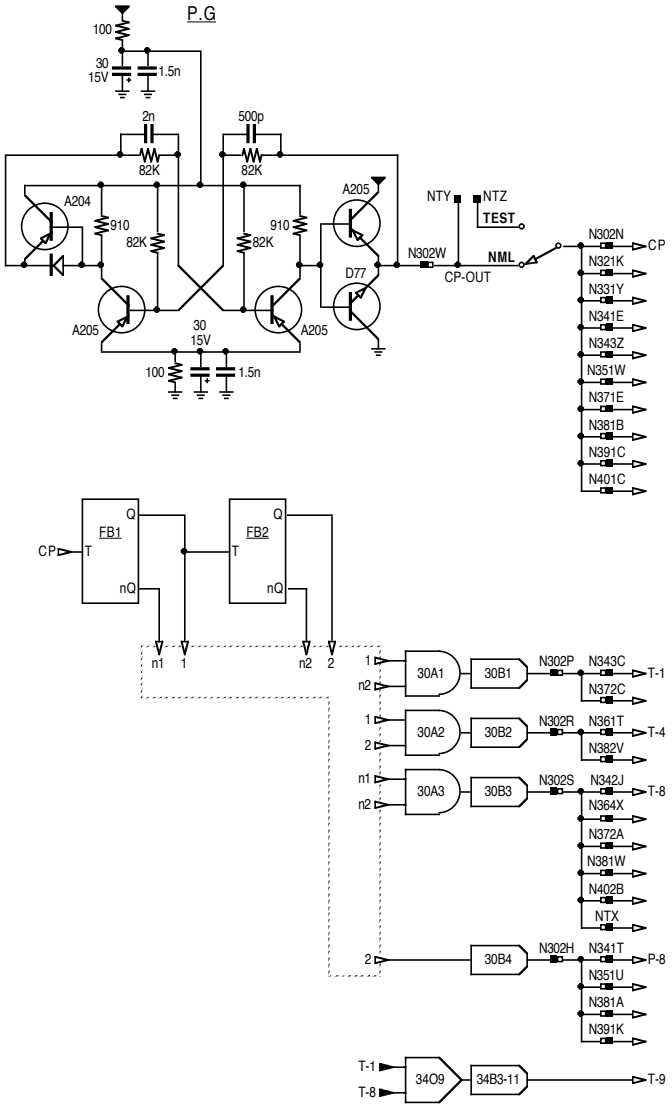
Type TETC

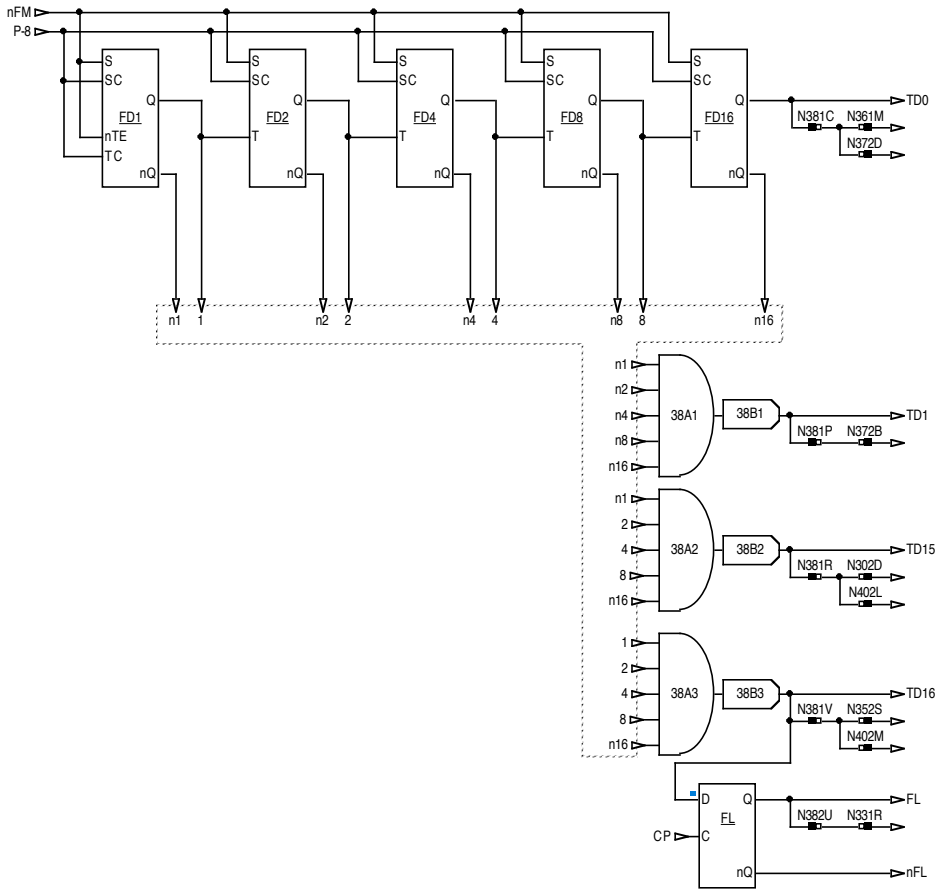
Toggle Q if nTE=0 on 1-to-0 edge of TC.

Note: Logic 0 = 0V, GND, E
Logic 1 = –10V

Section	Name	Types	Variations
Timing			
	FB1	T	
	FB2	T	
	FD1	TETC, S	RTE=22K CTC=680pF
	FD2	T, S	
	FD4	T, S	
	FD8	T, S	
	FD16	T, S	
	FL	D	
Keyboard			
	OS.ST	MC	
	FK	D	
	OS	nS, nR	
Control			
	FA	JK	
	F–	JK	
	FS	JK	
	FX	JK	CJK=470pF CFF=1nF T=A538
	F÷	JK	
	FO	JK	
	FM	JK	
	FG	JK	
	FH	JK	
	FP	JK	
	FZ	JK	
	FCO	JK	CJK=470pF CFF=1nF T=A538
	FCU	JK	
	FC1	JK, TETC	RTE=22K
	FC2	JK, TETC	RTE=22K
	FC4	JK, TETC	
AC Counter			
	AC1	JK, R	CJK=330pF T=A538
	AC2	TETC, R	
	AC4	TETC, R	
	AC8	TETC, R	
BC Counter			
	FB	JK	CJK=470pF CFF=1nF T=A538
	BC1	JK, R	CJK=470pF CR=470pF T=B221
	BC2	TETC, R	CR=470pF T=B221
	BC4	TETC, R	CR=470pF T=B221
	BC8	TETC, R	CR=470pF T=B221

Section	Name	Types	Variations
Arithmetic			
	CA	D, nR	
ACC Register			
	S1	D	CD=470pF CFF=1nF RFF=12K RL=3K
	S2	D	CD=470pF CFF=1nF RFF=12K RL=3K
	S3	D	CD=470pF CFF=1nF RFF=12K RL=3K
	S4	JK	CJK=470pF CFF=1nF RFF=12K RL=3K
	ACC11-8	D	CD=470pF CFF=1nF RFF=12K RL=3K
	ACC5-8	D	CD=470pF CFF=1nF RFF=12K RL=3K
	ACC*-*	JK	CJK=470pF CFF=1nF RFF=12K RL=3K
IR Register			
	IR16-8	D	
	IR16-4	D	
	IR16-2	D	
	IR16-1	D	
	IR2-8	D	
	IR1-8	D, S	
	IR1-4	JK, S	
	IR1-2	JK, S	
	IR1-1	JK, S	
	IR*-*	JK	
ME Register			
	ME16-8	D	CD=470pF CFF=1nF RFF=12K RL=3K
	ME*-*	JK	CJK=470pF CFF=1nF RFF=12K RL=3K
Shift Pulse Generators			
	SP-A	MEMC	
	SP-M	MEMC	
	SP-I	MEMC	
PC Counter			
	PC1	JK, R	CJK=820pF
	PC2	T, R	CT=820pF
	PC4	T, R	CT=820pF
	PC8	T, R	CT=820pF
DC Counter			
	FD	JK	
	DC1	JK, R	CJK=820pF
	DC2	T, R	CT=820pF
	DC4	T, R	CT=820pF
	DC8	T, R	CT=820pF





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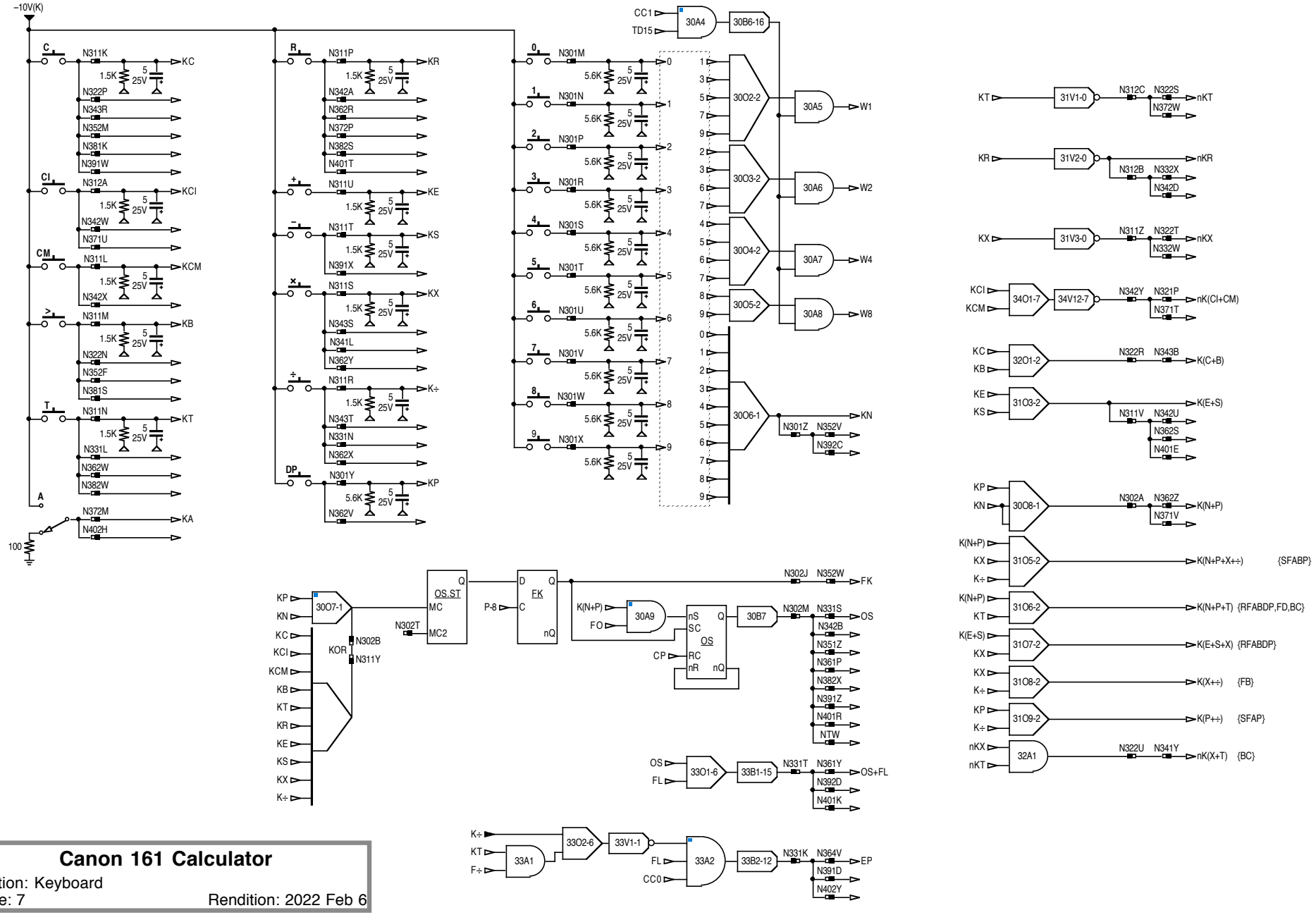
Section: Timing

Page: 6

Rendition: 2022 Feb 6



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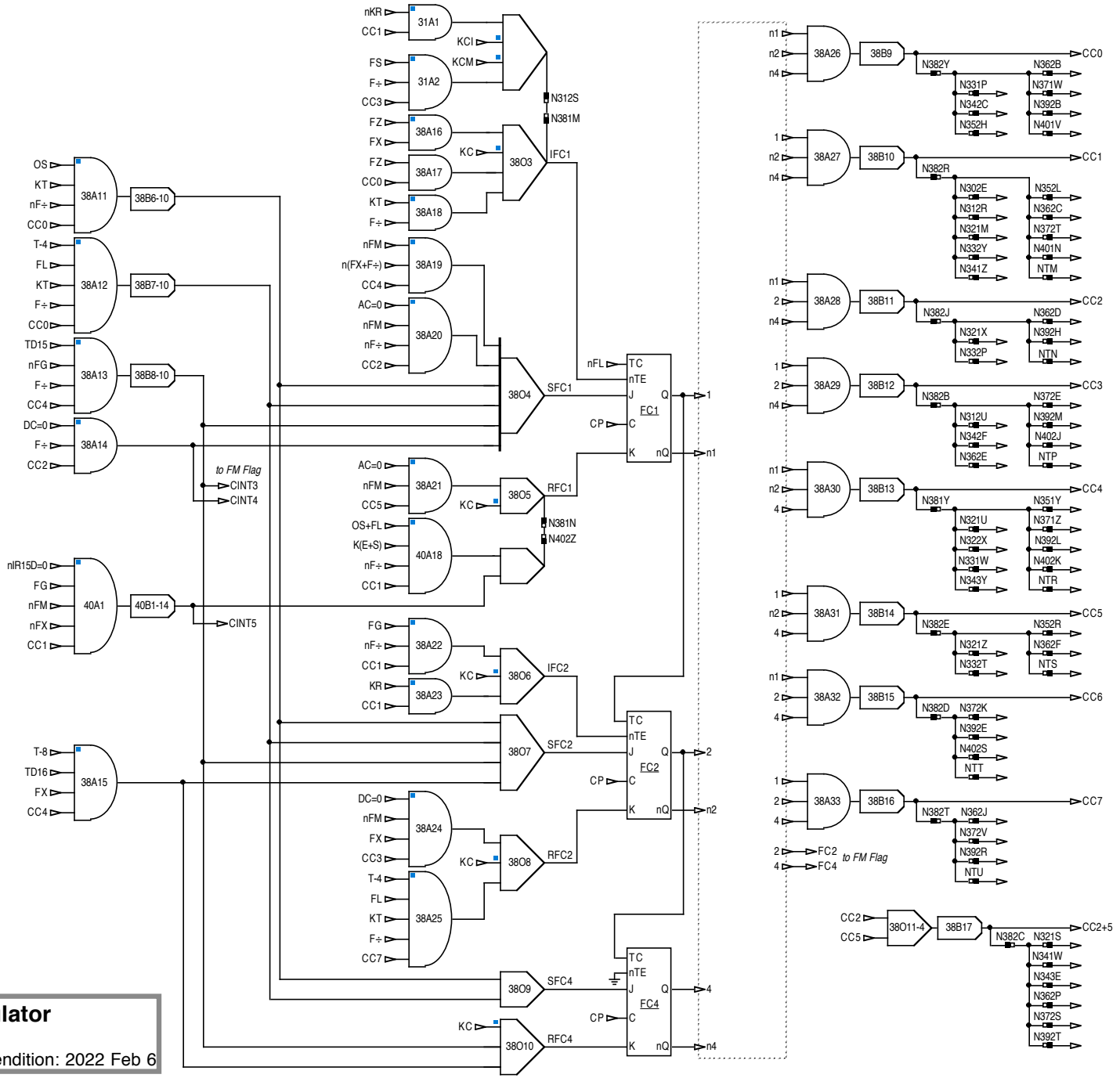
Section: Keyboard

Page: 7

Rendition: 2022 Feb 6



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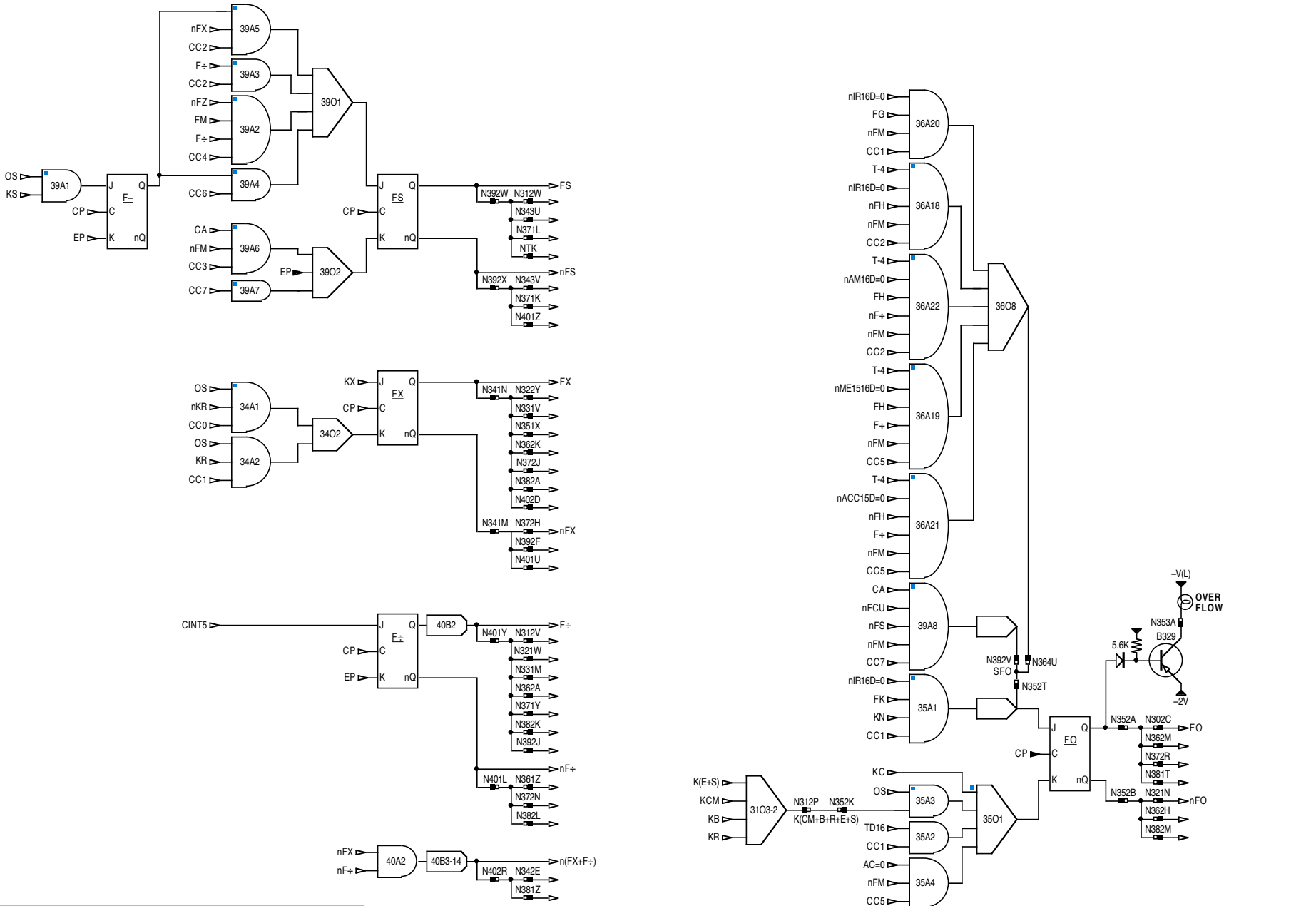
Section: Control State Machine

Page: 8 Rendition: 2022 Feb 6



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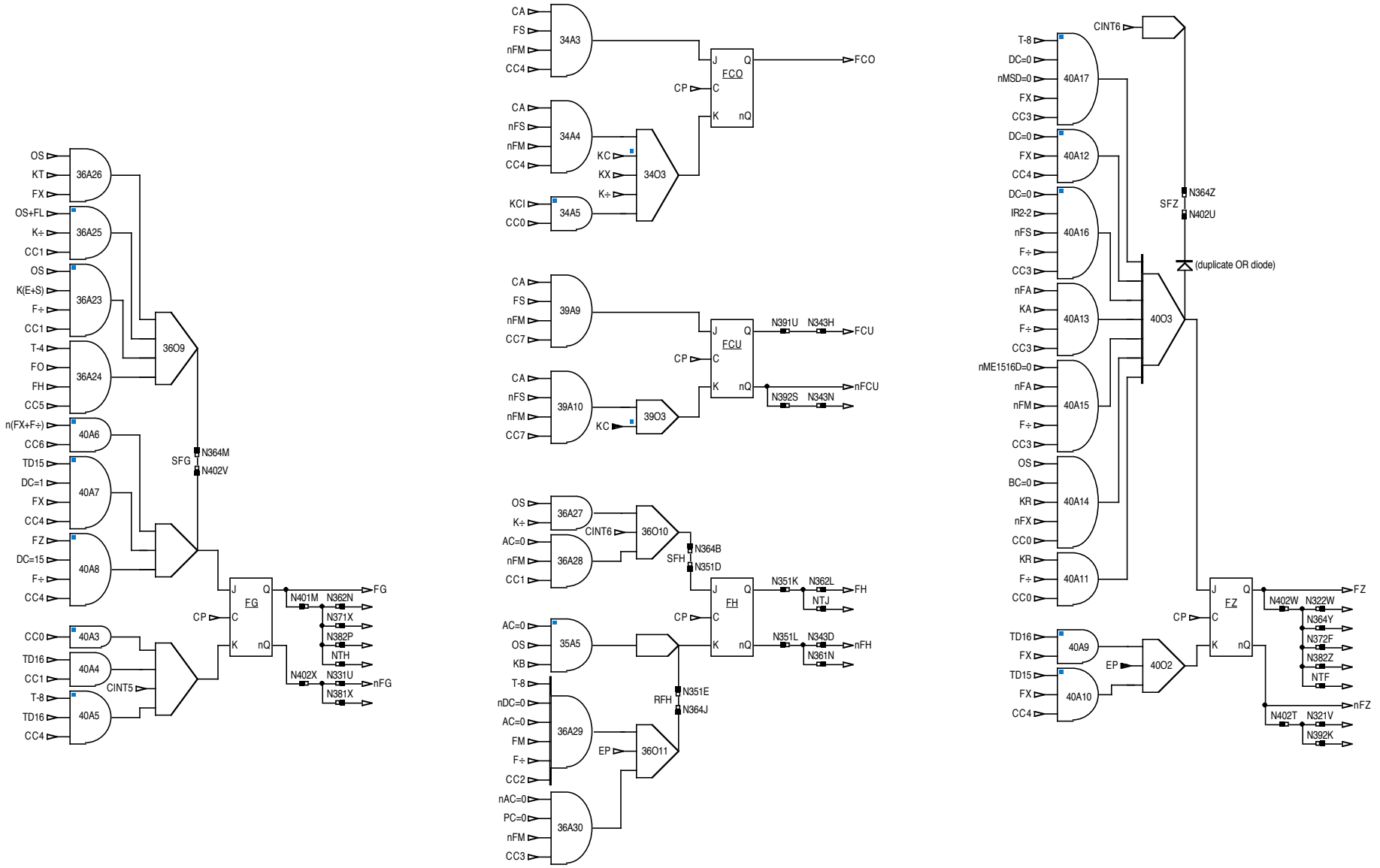
Section: Flags F–, FS, FX, F÷, FO

Page: 9 Rendition: 2022 Feb 6



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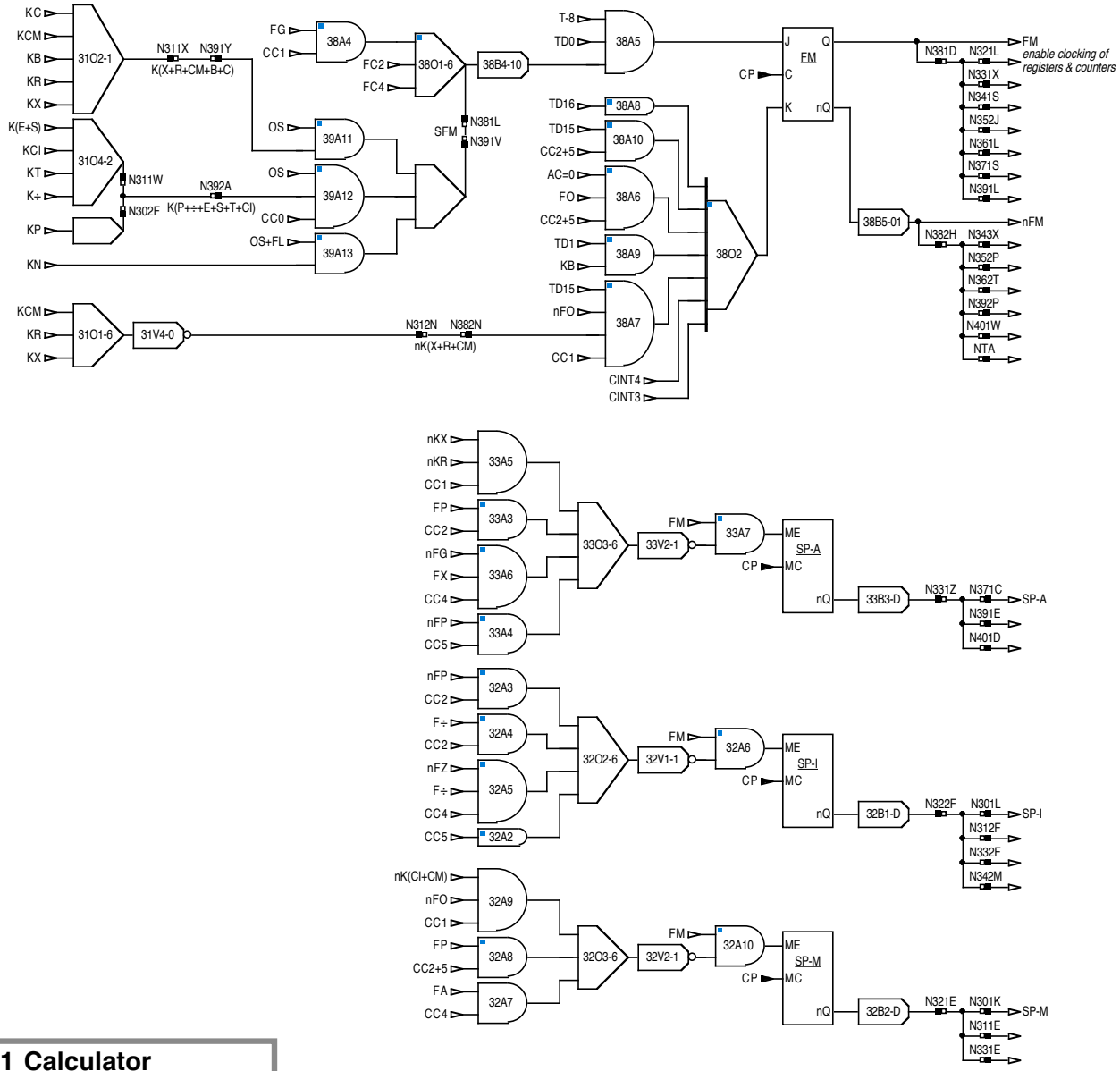
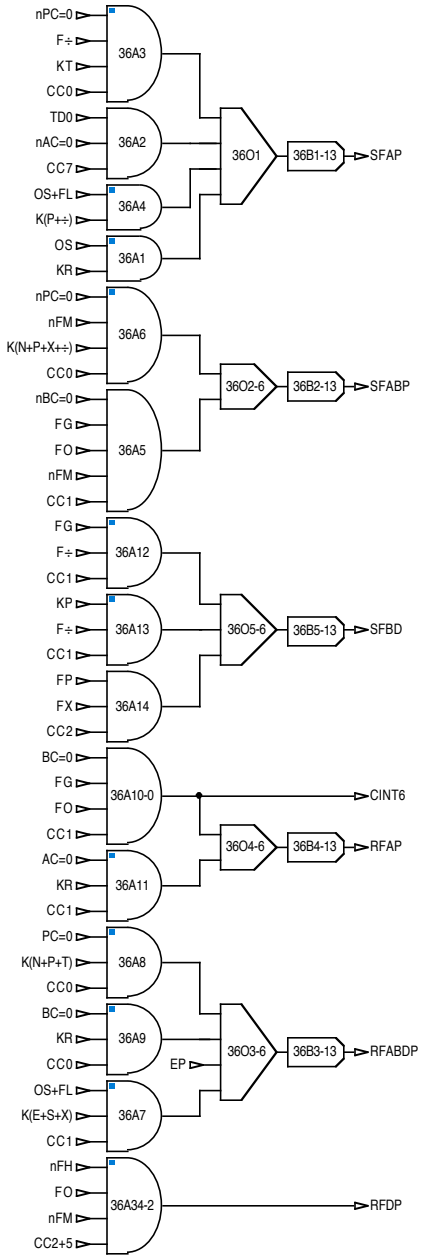
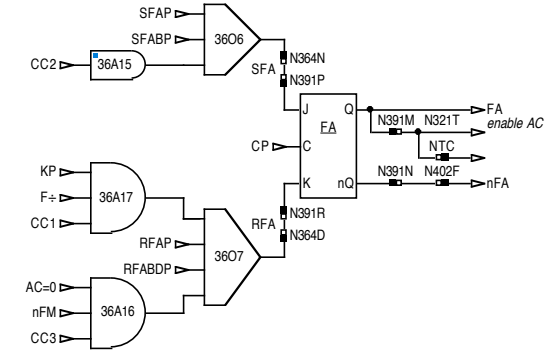
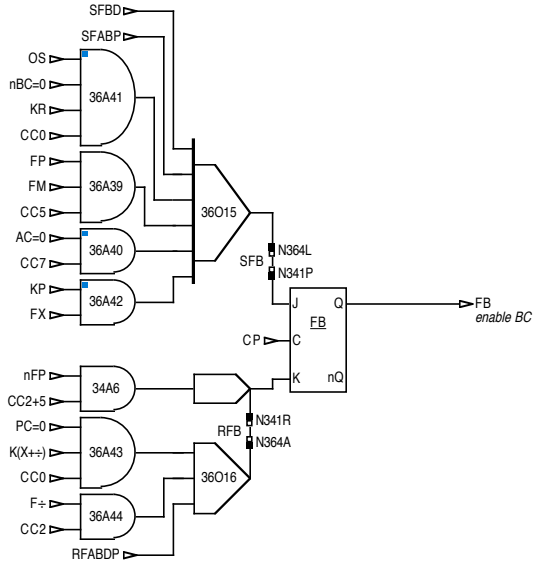
Section: Flags FG, FH, FZ, FCO, FCU

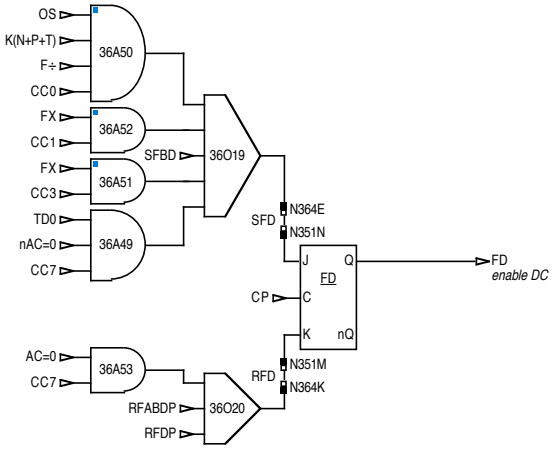
Rendition: 2022 Feb 6

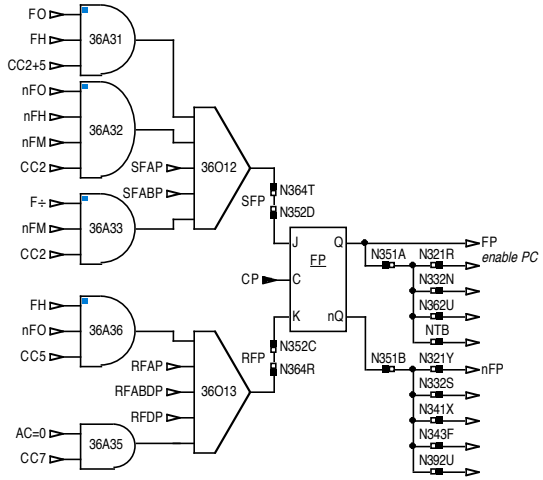

KC
KCM
KB
KR
KX
31O2-1
N311X
N391Y
K(X+R+CM+B+C)
K(E+S)
KCI
KT
K÷
31O4-2
N311W
N392A
N302F
K(P+÷+E+S+T+CI)
KP
KN
FG
CC1
38A4
FC2
FC4
38O1-6
38B4-10
OS
39A11
OS
39A12
CC0
OS+FL
39A13
SFM
N381L
N391V
T-8
TD0
38A5
TD16
38A8
TD15
38A10
CC2+5
AC=0
38A6
FO
CC2+5
TD1
38A9
KB
TD15
nFO
38A7
CC1
CINT4
CINT3
38O2
J
Q
FM
CP
C
K
nQ
38B5-01
N381D
N321L
FM
enable clocking of
registers & counters
N331X
N341S
N352J
N361L
N371S
N391L
N382H
N343X
nFM
N352P
N362T
N392P
N401W
NTA
KCM
KR
KX
31O1-6
31V4-0
N312N
N382N
nK(X+R+CM)
nKX
nKR
CC1
FP
CC2
nFG
FX
CC4
nFP
CC5
33A5
33A3
33A6
33A4
33O3-6
33V2-1
FM
33A7
CP
ME
SP-A
MC
nQ
33B3-D
N331Z
N371C
SP-A
N391E
N401D
nFP
CC2
F÷
CC2
nFZ
F÷
CC4
CC5
32A3
32A4
32A5
32A2
32O2-6
32V1-1
FM
32A6
CP
ME
SP-I
MC
nQ
32B1-D
N322F
N301L
SP-I
N312F
N332F
N342M
nK(CI+CM)
nFO
CC1
FP
CC2+5
FA
CC4
32A9
32A8
32A7
32O3-6
32V2-1
FM
32A10
CP
ME
SP-M
MC
nQ
32B2-D
N321E
N301K
SP-M
N311E
N331E









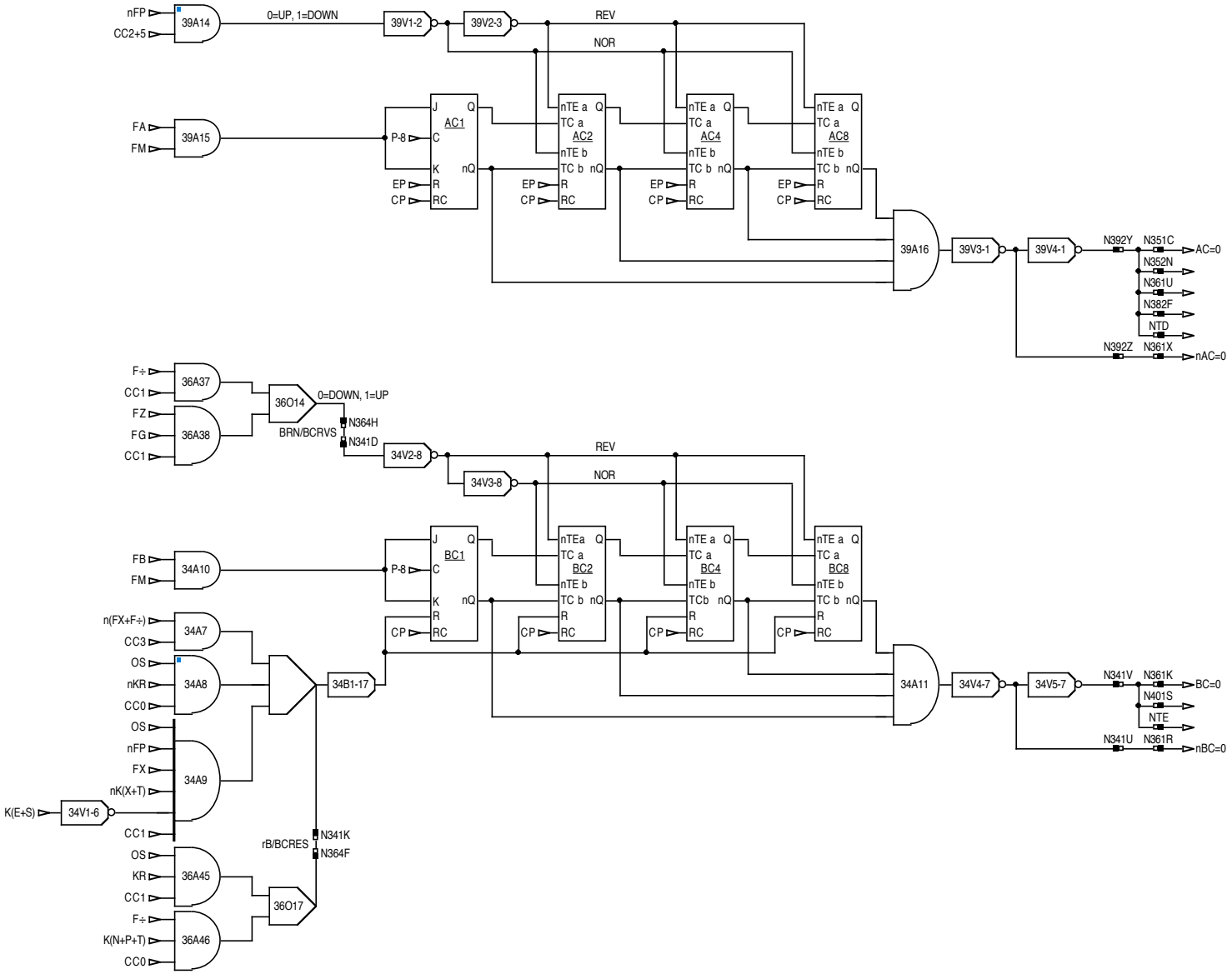


• CC2+5 input to gate 34A6 labeled on board as CC5.

• OR Diode for connection between 36A34 & 36O20 is labeled and installed as AND (DA/red) rather than DO/green).

Canon 161 Calculator

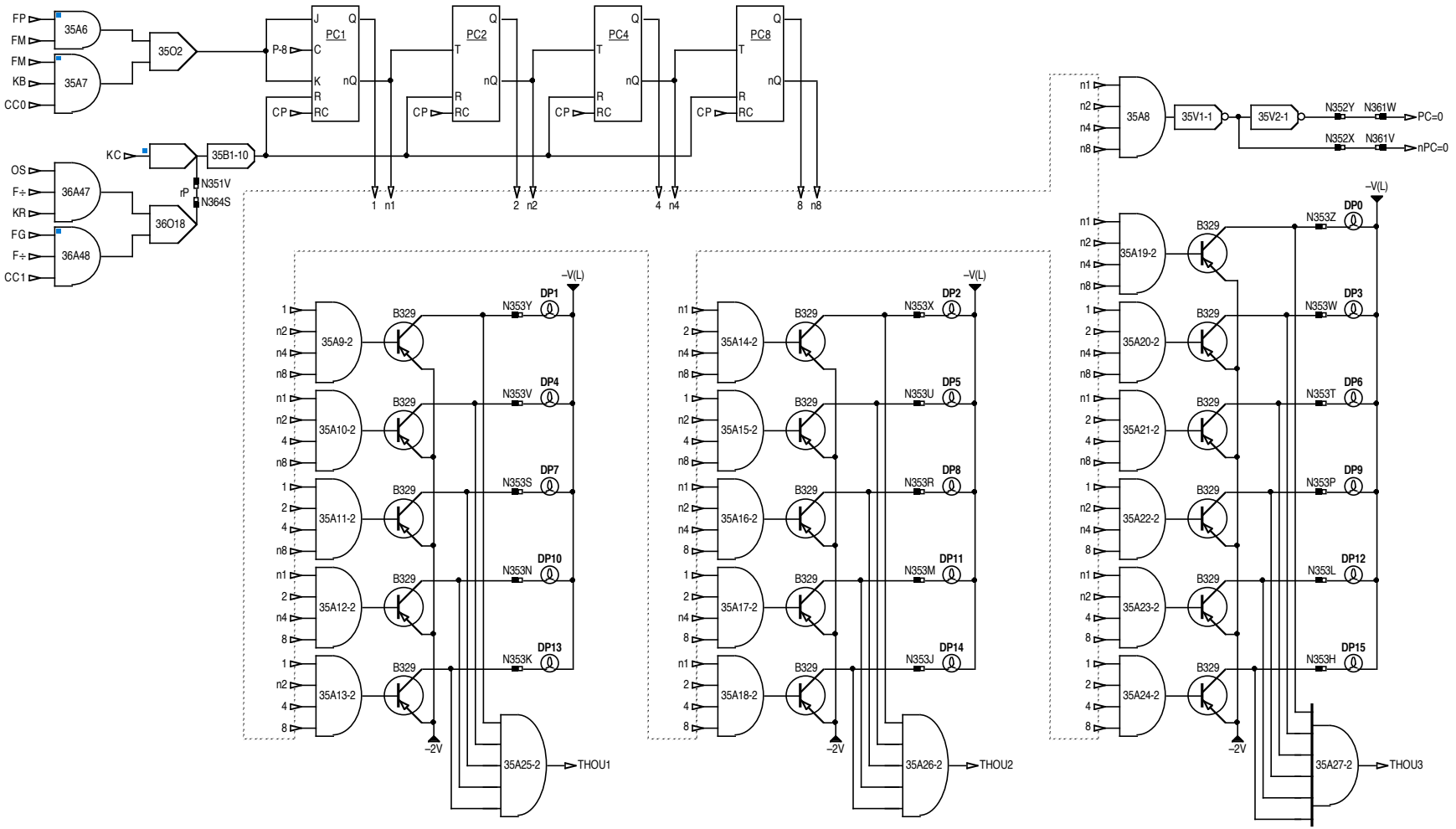
Section: Counter Enable Flags FA, FB, FD, FP

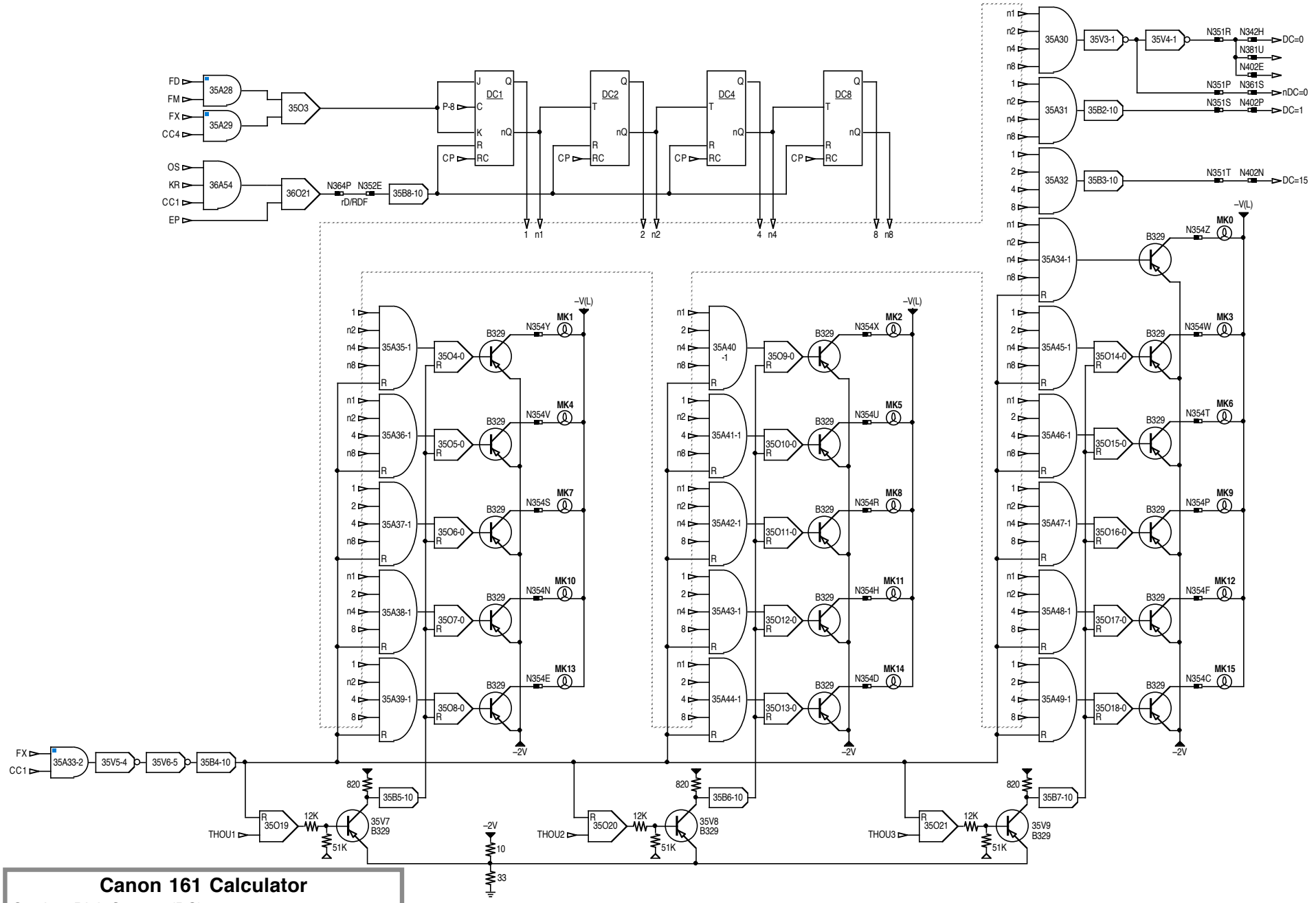


Canon 161 Calculator

Section: A & B Counters (AC & BC)

 Rendition: 2022 Feb 6

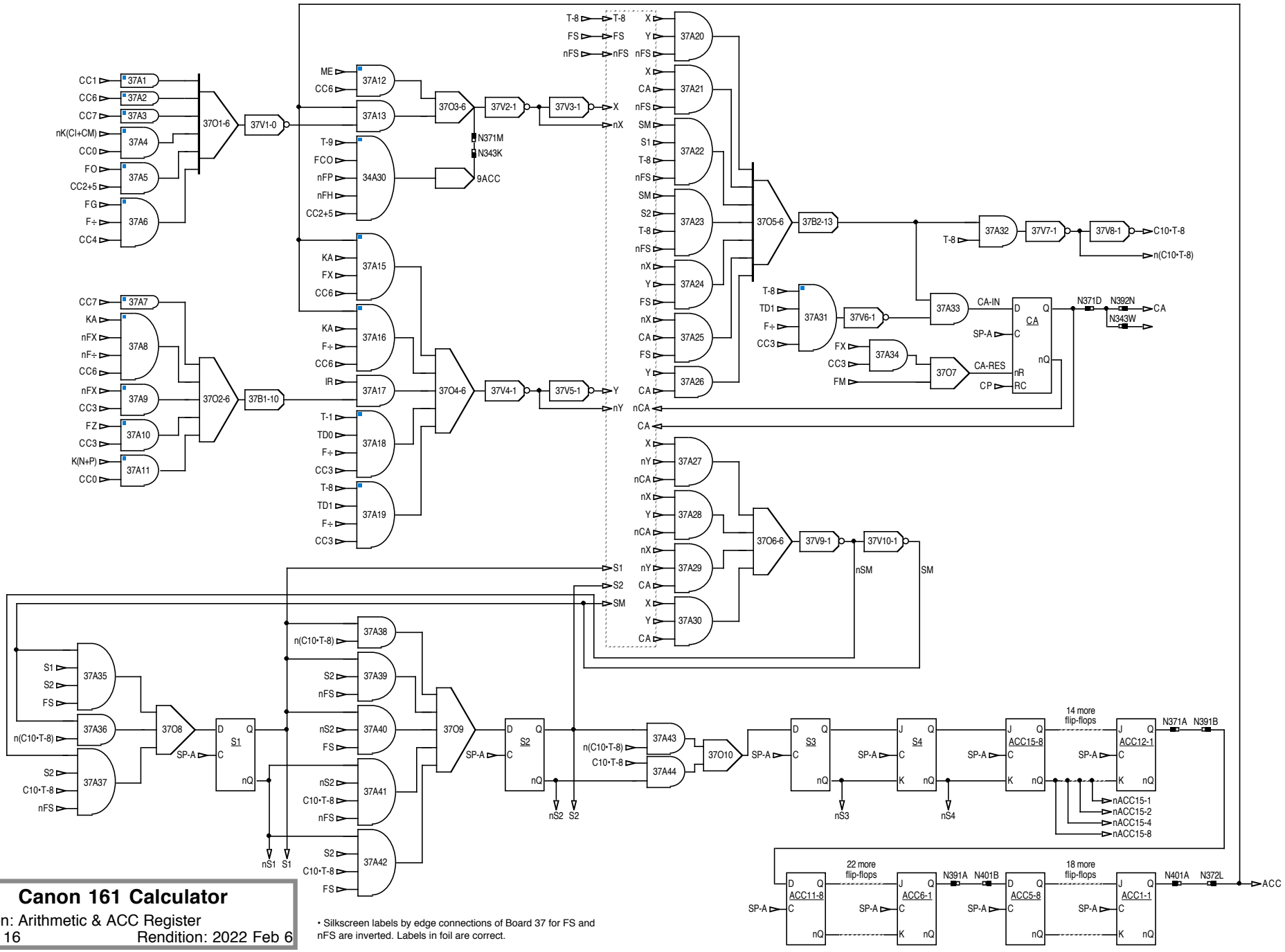

FP
FM
FM
KB
CC0
35A6
35A7
35O2
P-8
PC1
PC2
PC4
PC8
J
K
C
T
R
CP
RC
Q
nQ
KC
35B1-10
OS
F÷
KR
FG
F÷
CC1
36A47
36A48
36O18
N351V
N364S
rP
1 n1
2 n2
4 n4
8 n8
35A8
35V1-1
35V2-1
N352Y
N361W
PC=0
N352X
N361V
nPC=0
–V(L)
B329
35A9-2
35A10-2
35A11-2
35A12-2
35A13-2
35A14-2
35A15-2
35A16-2
35A17-2
35A18-2
35A19-2
35A20-2
35A21-2
35A22-2
35A23-2
35A24-2
DP1
DP2
DP3
DP4
DP5
DP6
DP7
DP8
DP9
DP10
DP11
DP12
DP13
DP14
DP15
DP0
N353Y
N353X
N353W
N353V
N353U
N353T
N353S
N353R
N353P
N353N
N353M
N353L
N353K
N353J
N353H
N353Z
–2V
35A25-2
35A26-2
35A27-2
THOU1
THOU2
THOU3



Canon 161 Calculator

Section: Digit Counter (DC)

Rendition: 2022 Feb 6

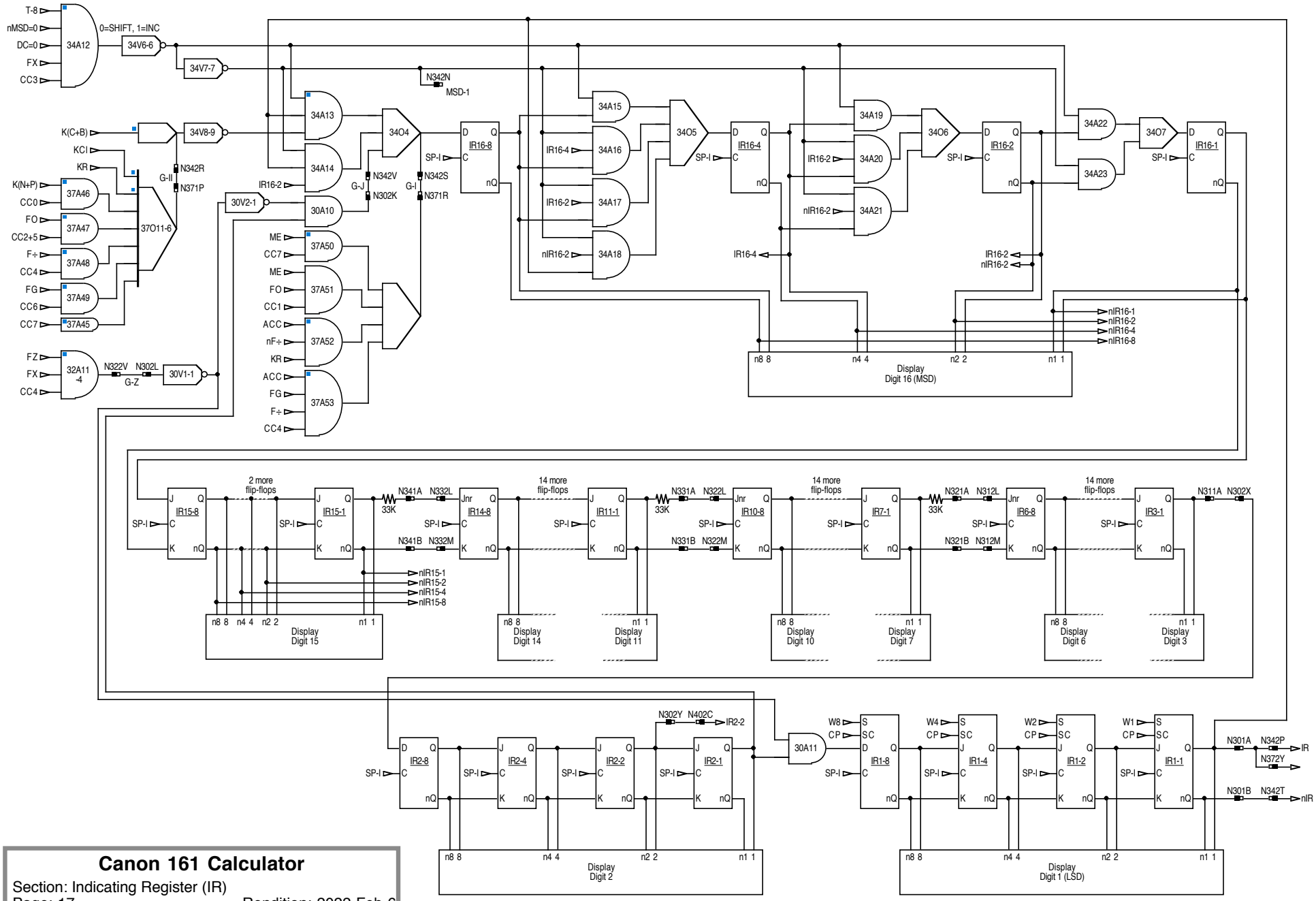


Canon 161 Calculator

Section: Arithmetic & ACC Register

Page: 16 Rendition: 2022 Feb 6

• Silkscreen labels by edge connections of Board 37 for FS and nFS are inverted. Labels in foil are correct.



Canon 161 Calculator

Section: Indicating Register (IR)

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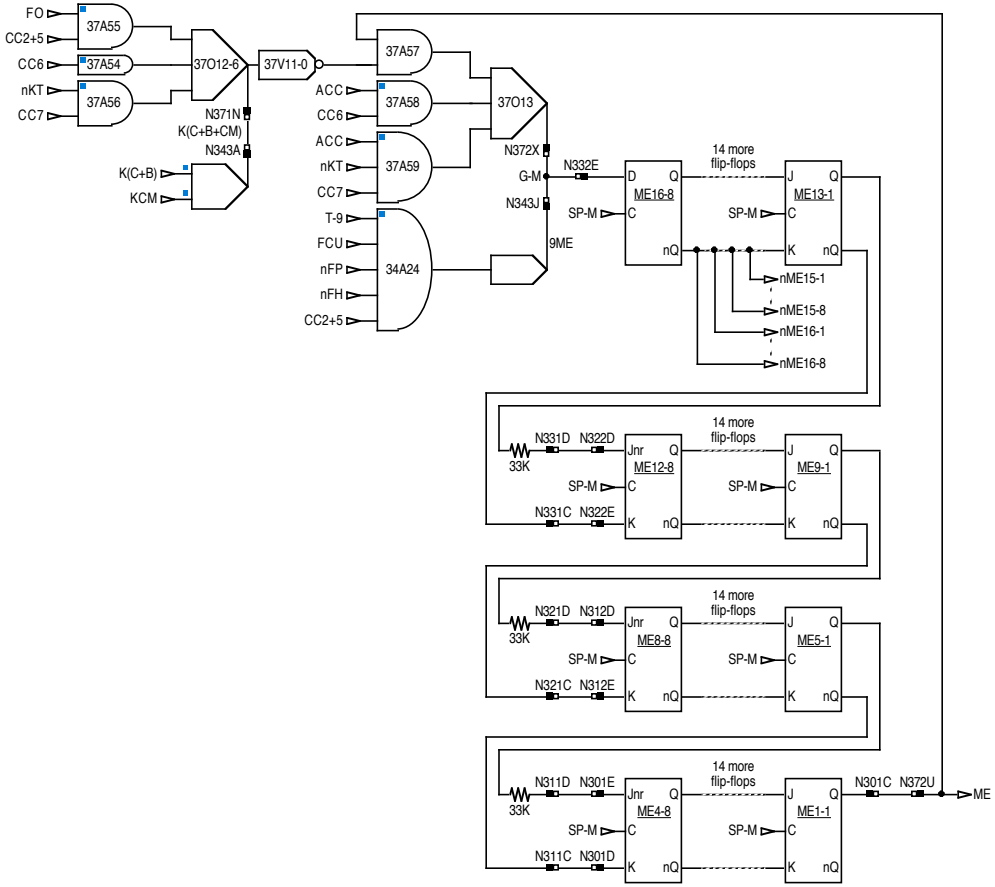
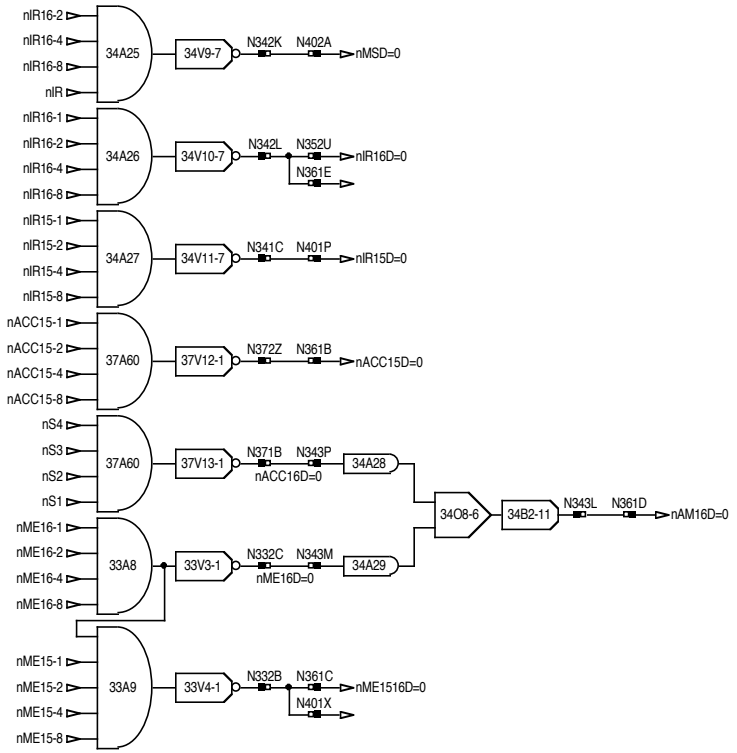
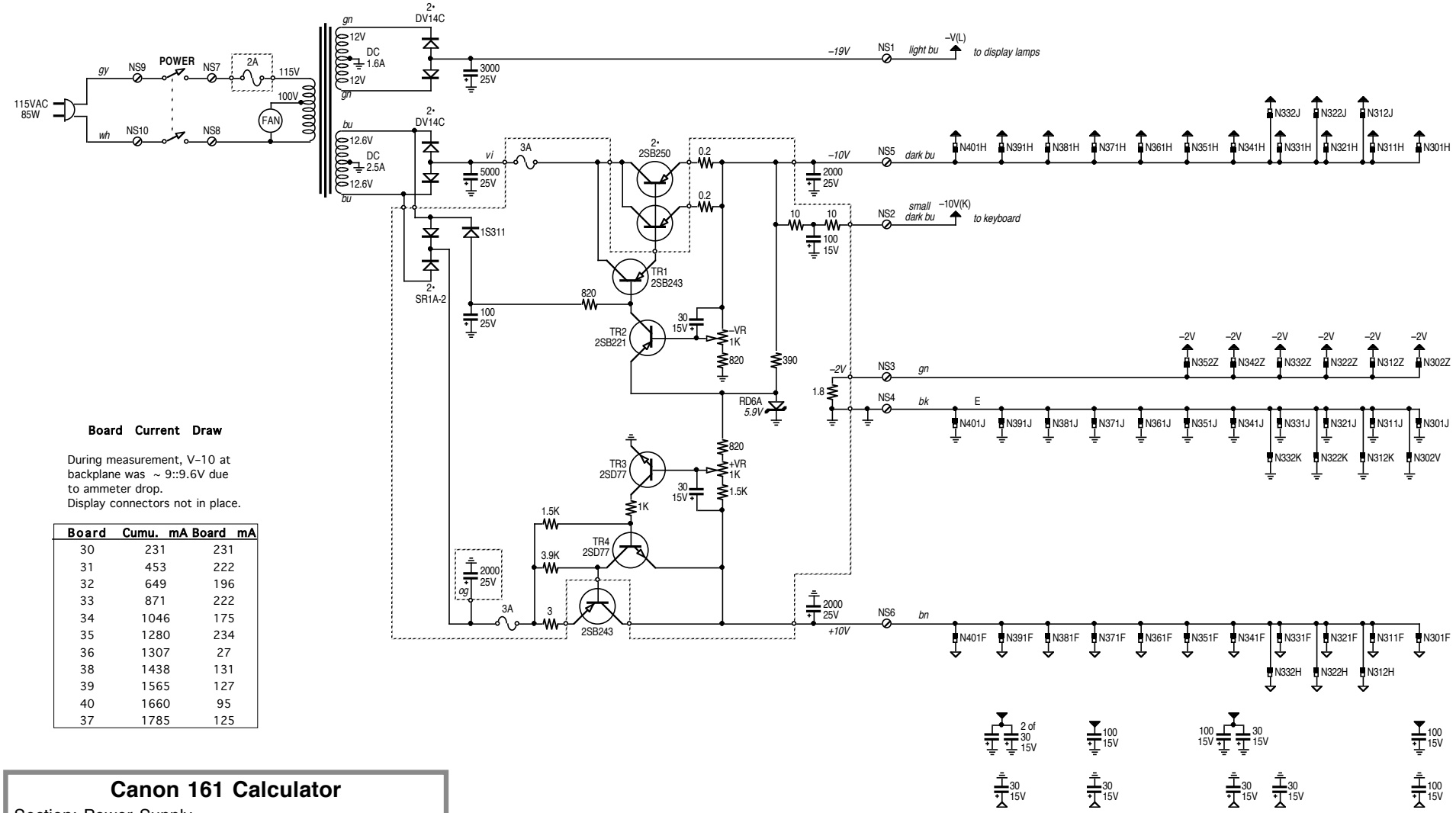




Canon 161 Calculator

Section: ME Register & Zero Gates

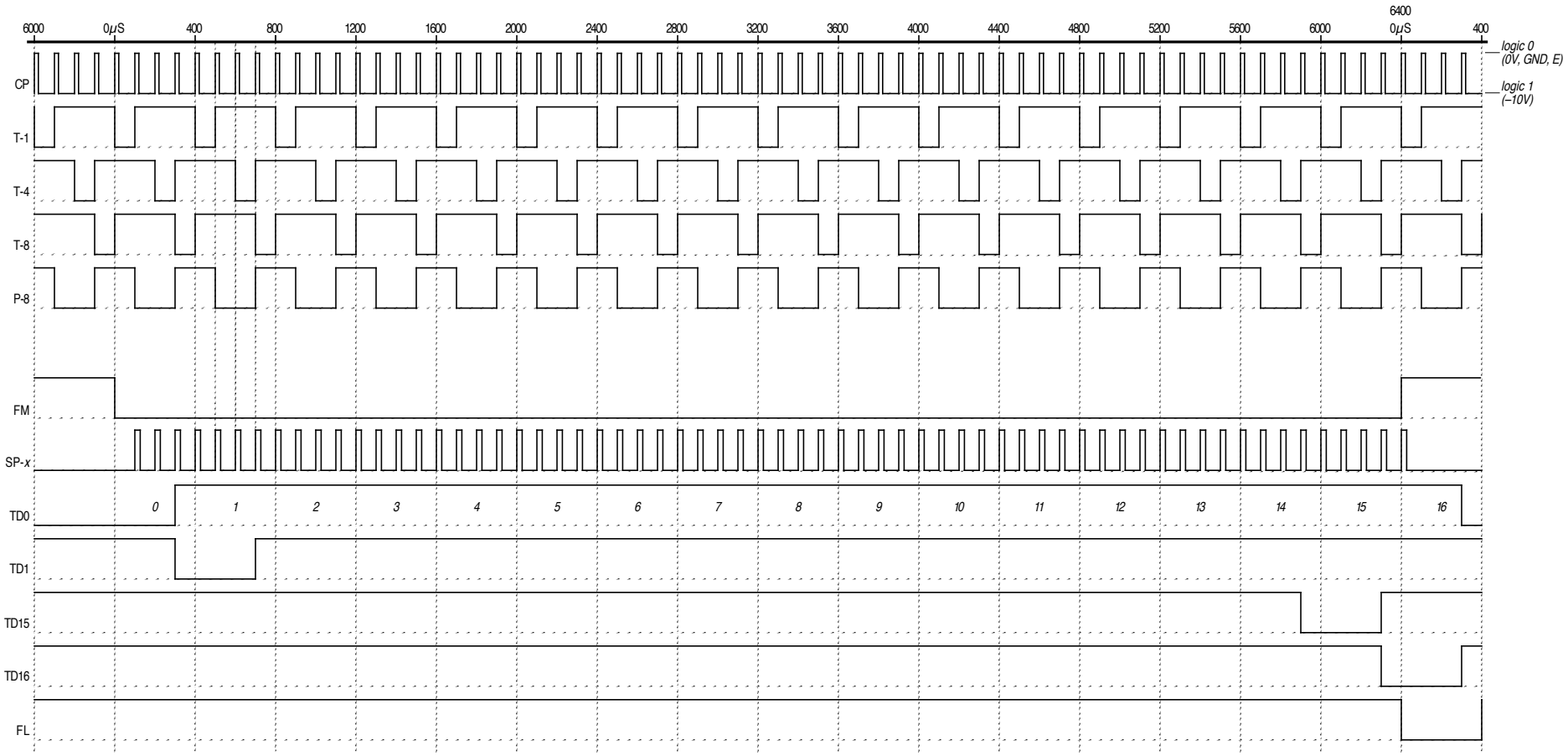
Rendition: 2022 Feb 6



Board Current Draw

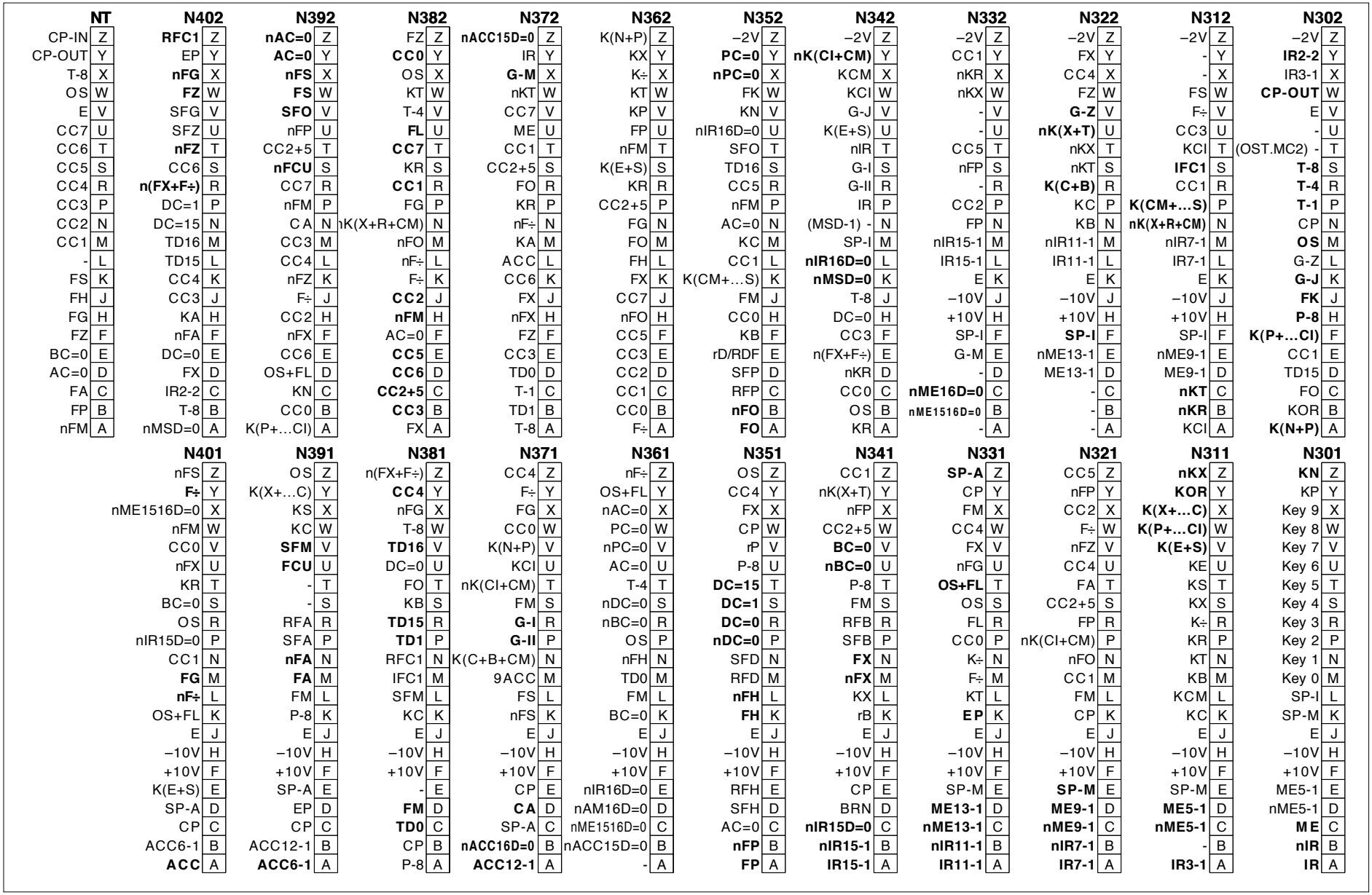
During measurement, V–10 at backplane was ~ 9::9.6V due to ammeter drop.
Display connectors not in place.

Board	Cumu. mA	Board mA
30	231	231
31	453	222
32	649	196
33	871	222
34	1046	175
35	1280	234
36	1307	27
38	1438	131
39	1565	127
40	1660	95
37	1785	125



Notes

- Signals are shown as they would typically appear on an oscilloscope, with more-positive voltage vertically higher on the trace. In contrast, for logic levels logic 1 is the lower level of a trace and logic 0 the higher level.
- One cycle of FM during an operation is shown here. SP-*x*, TD*x*, and FL are only active during FM. During some states, these signals may vary from those shown here .
- As measured, CP cycle time is 105 μS (9.6 KHz) with 0 pulse of 17 μS.
- As measured, SP-x 0 pulses are 20 μS.



NT		N402		N392		N382		N372		N362		N352		N342		N332		N322		N312		N302	
CP-IN	Z	**RFC1**	Z	**nAC=0**	Z	FZ	Z	**nACC15D=0**	Z	K(N+P)	Z	–2V	Z	–2V	Z	–2V	Z	–2V	Z	–2V	Z	–2V	Z
CP-OUT	Y	EP	Y	**AC=0**	Y	**CC0**	Y	IR	Y	KX	Y	**PC=0**	Y	**nK(CI+CM)**	Y	CC1	Y	FX	Y	-	Y	**IR2-2**	Y
T-8	X	**nFG**	X	**nFS**	X	OS	X	**G-M**	X	K÷	X	**nPC=0**	X	KCM	X	nKR	X	CC4	X	-	X	IR3-1	X
OS	W	**FZ**	W	**FS**	W	KT	W	nKT	W	KT	W	FK	W	KCI	W	nKX	W	FZ	W	FS	W	**CP-OUT**	W
E	V	SFG	V	**SFO**	V	T-4	V	CC7	V	KP	V	KN	V	G-J	V	-	V	**G-Z**	V	F÷	V	E	V
CC7	U	SFZ	U	nFP	U	**FL**	U	ME	U	FP	U	nIR16D=0	U	K(E+S)	U	-	U	**nK(X+T)**	U	CC3	U	-	U
CC6	T	**nFZ**	T	CC2+5	T	**CC7**	T	CC1	T	nFM	T	SFO	T	nIR	T	CC5	T	nKX	T	KCI	T	(OST.MC2)	- T
CC5	S	CC6	S	**nFCU**	S	KR	S	CC2+5	S	K(E+S)	S	TD16	S	G-I	S	nFP	S	nKT	S	**IFC1**	S	**T-8**	S
CC4	R	**n(FX+F÷)**	R	CC7	R	**CC1**	R	FO	R	KR	R	CC5	R	G-II	R	-	R	**K(C+B)**	R	CC1	R	**T-4**	R
CC3	P	DC=1	P	nFM	P	FG	P	KR	P	CC2+5	P	nFM	P	IR	P	CC2	P	KC	P	**K(CM+…S)**	P	**T-1**	P
CC2	N	DC=15	N	CA	N	nK(X+R+CM)	N	nF÷	N	FG	N	AC=0	N	(MSD-1)	- N	FP	N	KB	N	**nK(X+R+CM)**	N	CP	N
CC1	M	TD16	M	CC3	M	nFO	M	KA	M	FO	M	KC	M	SP-I	M	nIR15-1	M	nIR11-1	M	nIR7-1	M	**OS**	M
-	L	TD15	L	CC4	L	nF÷	L	ACC	L	FH	L	CC1	L	**nIR16D=0**	L	IR15-1	L	IR11-1	L	IR7-1	L	G-Z	L
FS	K	CC4	K	nFZ	K	F÷	K	CC6	K	FX	K	K(CM+…S)	K	**nMSD=0**	K	E	K	E	K	E	K	**G-J**	K
FH	J	CC3	J	F÷	J	**CC2**	J	FX	J	CC7	J	FM	J	T-8	J	–10V	J	–10V	J	–10V	J	**FK**	J
FG	H	KA	H	CC2	H	**nFM**	H	nFX	H	nFO	H	CC0	H	DC=0	H	+10V	H	+10V	H	+10V	H	**P-8**	H
FZ	F	nFA	F	nFX	F	AC=0	F	FZ	F	CC5	F	KB	F	CC3	F	SP-I	F	**SP-I**	F	SP-I	F	**K(P+…CI)**	F
BC=0	E	DC=0	E	CC6	E	**CC5**	E	CC3	E	CC3	E	rD/RDF	E	n(FX+F÷)	E	G-M	E	nME13-1	E	nME9-1	E	CC1	E
AC=0	D	FX	D	OS+FL	D	**CC6**	D	TD0	D	CC2	D	SFP	D	nKR	D	-	D	ME13-1	D	ME9-1	D	TD15	D
FA	C	IR2-2	C	KN	C	**CC2+5**	C	T-1	C	CC1	C	RFP	C	CC0	C	**nME16D=0**	C	-	C	**nKT**	C	FO	C
FP	B	T-8	B	CC0	B	**CC3**	B	TD1	B	CC0	B	**nFO**	B	OS	B	nME1516D=0	B	-	B	**nKR**	B	KOR	B
nFM	A	nMSD=0	A	K(P+…CI)	A	FX	A	T-8	A	F÷	A	**FO**	A	KR	A	-	A	-	A	KCI	A	**K(N+P)**	A

N401		N391		N381		N371		N361		N351		N341		N331		N321		N311		N301	
nFS	Z	OS	Z	n(FX+F÷)	Z	CC4	Z	nF÷	Z	OS	Z	CC1	Z	**SP-A**	Z	CC5	Z	**nKX**	Z	**KN**	Z
F÷	Y	K(X+…C)	Y	**CC4**	Y	F÷	Y	OS+FL	Y	CC4	Y	nK(X+T)	Y	CP	Y	nFP	Y	**KOR**	Y	KP	Y
nME1516D=0	X	KS	X	nFG	X	FG	X	nAC=0	X	FX	X	nFP	X	FM	X	CC2	X	**K(X+…C)**	X	Key 9	X
nFM	W	KC	W	T-8	W	CC0	W	PC=0	W	CP	W	CC2+5	W	CC4	W	F÷	W	**K(P+…CI)**	W	Key 8	W
CC0	V	**SFM**	V	**TD16**	V	K(N+P)	V	nPC=0	V	rP	V	**BC=0**	V	FX	V	nFZ	V	**K(E+S)**	V	Key 7	V
nFX	U	**FCU**	U	DC=0	U	KCI	U	AC=0	U	P-8	U	**nBC=0**	U	nFG	U	CC4	U	KE	U	Key 6	U
KR	T	-	T	FO	T	nK(CI+CM)	T	T-4	T	**DC=15**	T	P-8	T	**OS+FL**	T	FA	T	KS	T	Key 5	T
BC=0	S	-	S	KB	S	FM	S	nDC=0	S	**DC=1**	S	FM	S	OS	S	CC2+5	S	KX	S	Key 4	S
OS	R	RFA	R	**TD15**	R	**G-I**	R	nBC=0	R	**DC=0**	R	RFB	R	FL	R	FP	R	K÷	R	Key 3	R
nIR15D=0	P	SFA	P	**TD1**	P	**G-II**	P	OS	P	**nDC=0**	P	SFB	P	CC0	P	nK(CI+CM)	P	KR	P	Key 2	P
CC1	N	**nFA**	N	RFC1	N	K(C+B+CM)	N	nFH	N	SFD	N	**FX**	N	K÷	N	nFO	N	KT	N	Key 1	N
FG	M	**FA**	M	IFC1	M	9ACC	M	TD0	M	RFD	M	**nFX**	M	F÷	M	CC1	M	KB	M	Key 0	M
nF÷	L	FM	L	SFM	L	FS	L	FM	L	**nFH**	L	KX	L	KT	L	FM	L	KCM	L	SP-I	L
OS+FL	K	P-8	K	KC	K	nFS	K	BC=0	K	**FH**	K	rB	K	**EP**	K	CP	K	KC	K	SP-M	K
E	J	E	J	E	J	E	J	E	J	E	J	E	J	E	J	E	J	E	J	E	J
–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H	–10V	H
+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F	+10V	F
K(E+S)	E	SP-A	E	-	E	CP	E	nIR16D=0	E	RFH	E	CP	E	SP-M	E	**SP-M**	E	SP-M	E	ME5-1	E
SP-A	D	EP	D	**FM**	D	**CA**	D	nAM16D=0	D	SFH	D	BRN	D	**ME13-1**	D	**ME9-1**	D	**ME5-1**	D	nME5-1	D
CP	C	CP	C	**TD0**	C	SP-A	C	nME1516D=0	C	AC=0	C	**nIR15D=0**	C	**nME13-1**	C	**nME9-1**	C	**nME5-1**	C	**ME**	C
ACC6-1	B	ACC12-1	B	CP	B	**nACC16D=0**	B	nACC15D=0	B	**nFP**	B	**nIR15-1**	B	**nIR11-1**	B	**nIR7-1**	B	-	B	**nIR**	B
ACC	A	**ACC6-1**	A	P-8	A	**ACC12-1**	A	-	A	**FP**	A	**IR15-1**	A	**IR11-1**	A	**IR7-1**	A	**IR3-1**	A	**IR**	A

Canon 161 Calculator

Section: Connectors N*bb1p* & N*bb2p*
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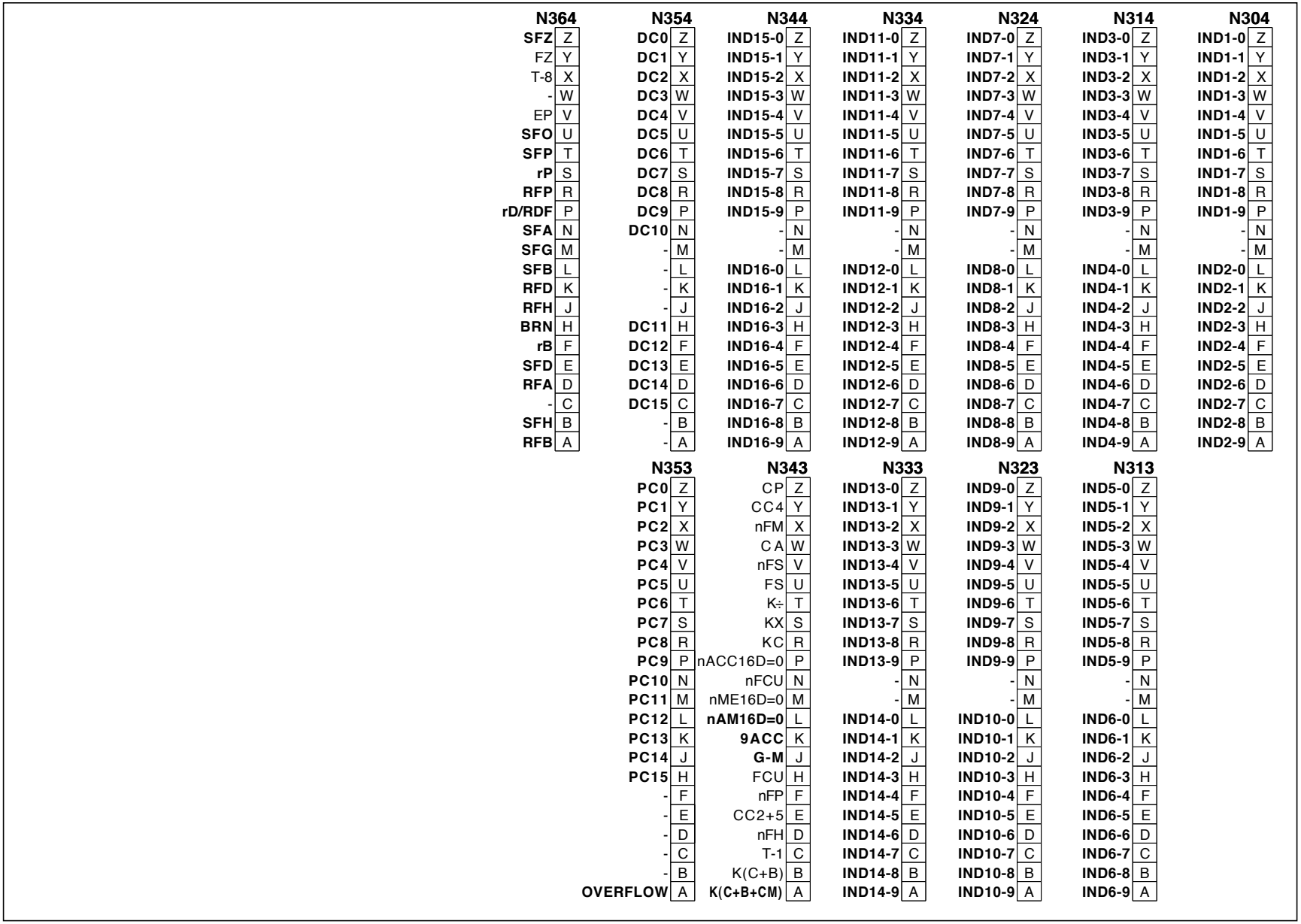
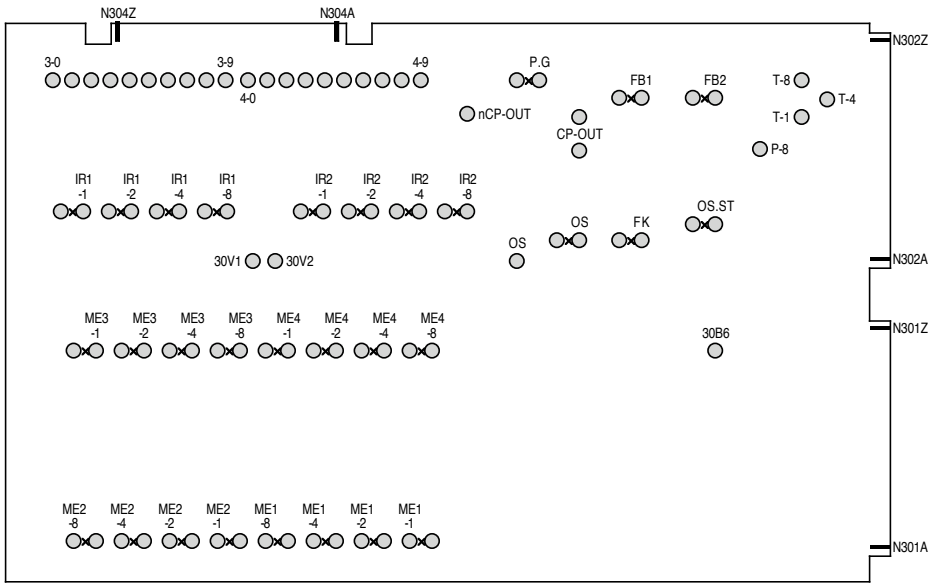
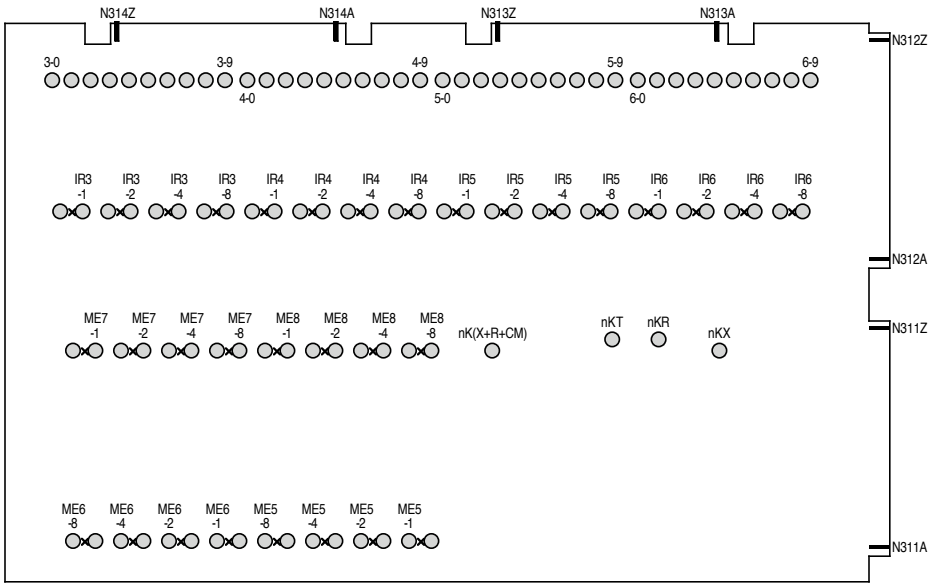
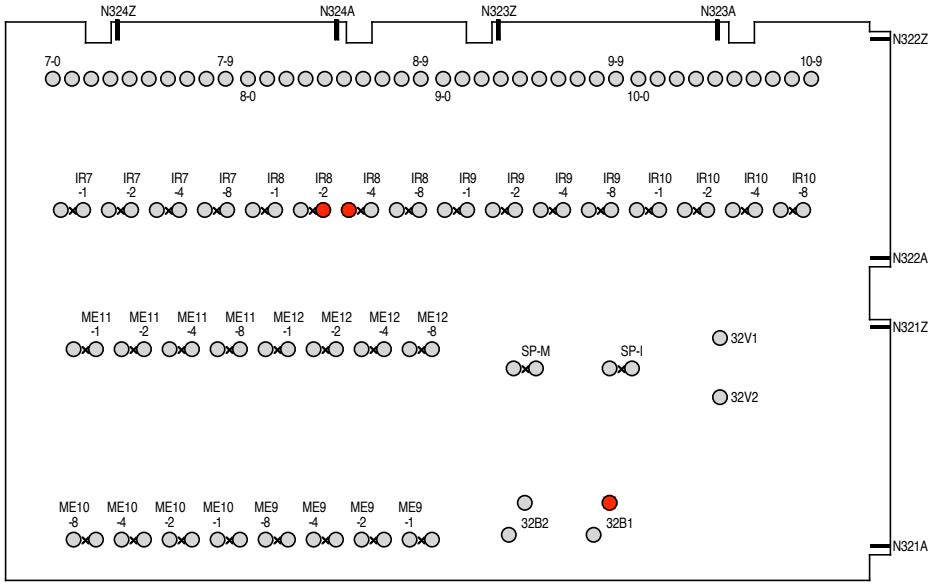
• Bold-faced expressions are signal sources.

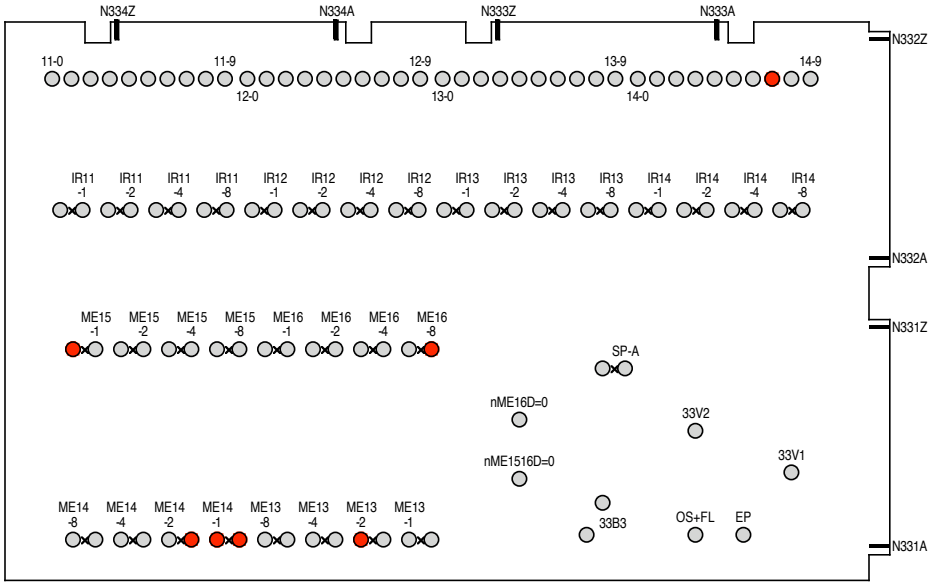


• Bold-faced expressions are signal sources.









Canon 161 Calculator

Section: Board Layout - 30::33

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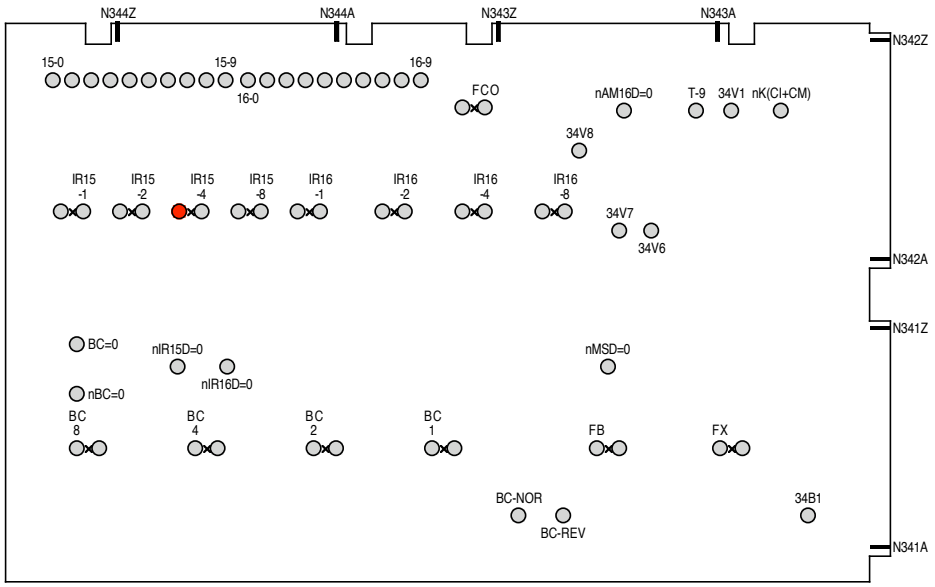
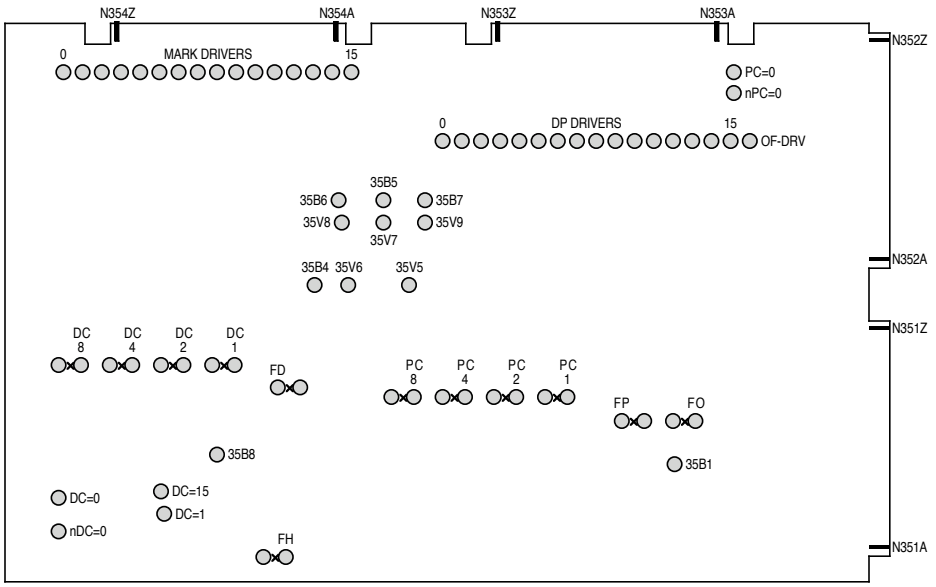
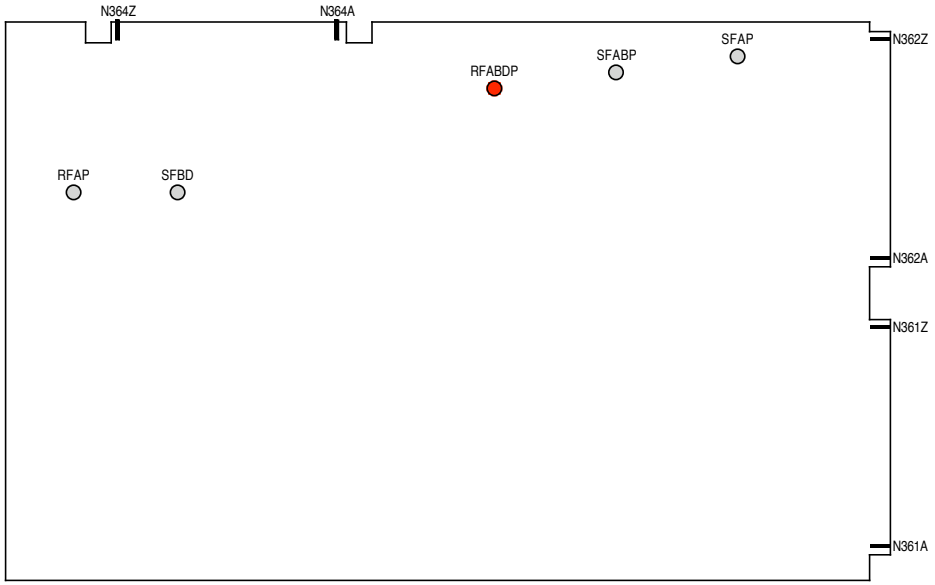
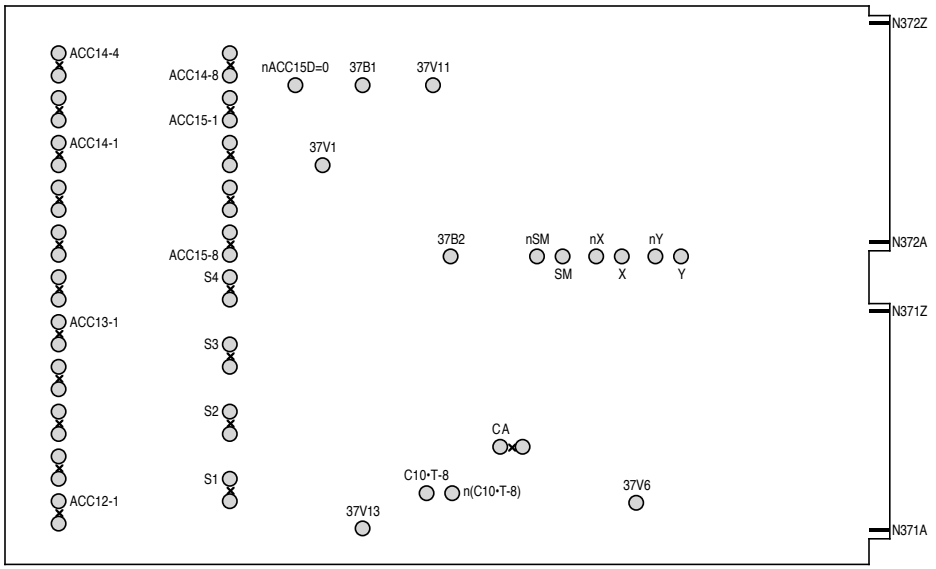
- Flip-flop transistors are labeled on the physical boards as 0 or 1. 1 is the Q transistor, 0 is the nQ transistor.
- In these diagrams, flip-flop names are closest to the Q transistor.
- Transistors marked in red are those found faulty and replaced in Unit 700369.





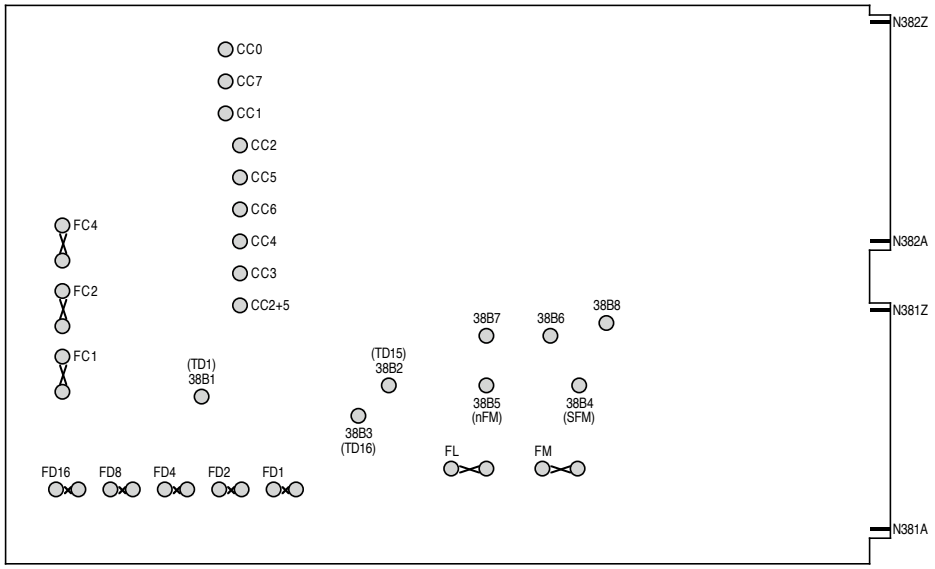


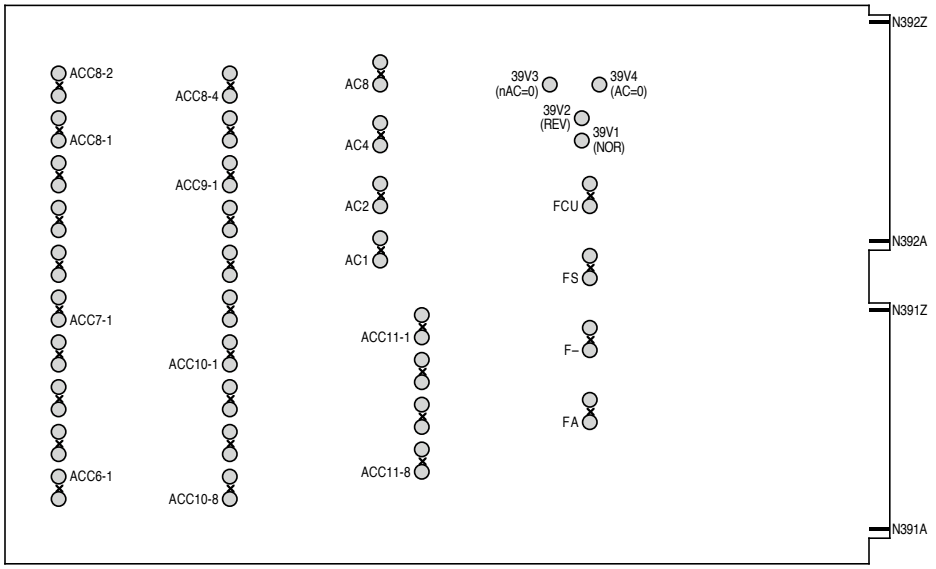


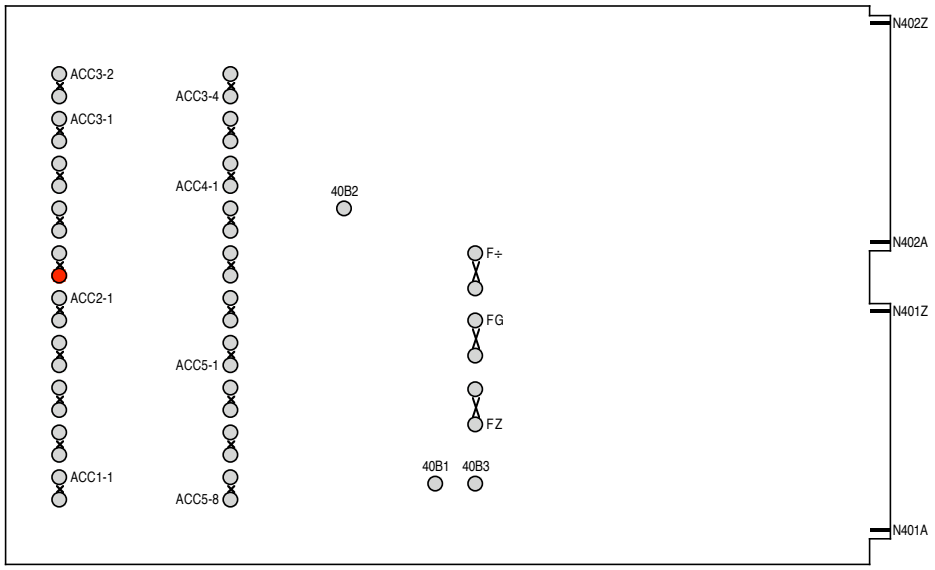
Canon 161 Calculator

Section: Board Layout - 34::37

Rendition: 2022 Feb 6



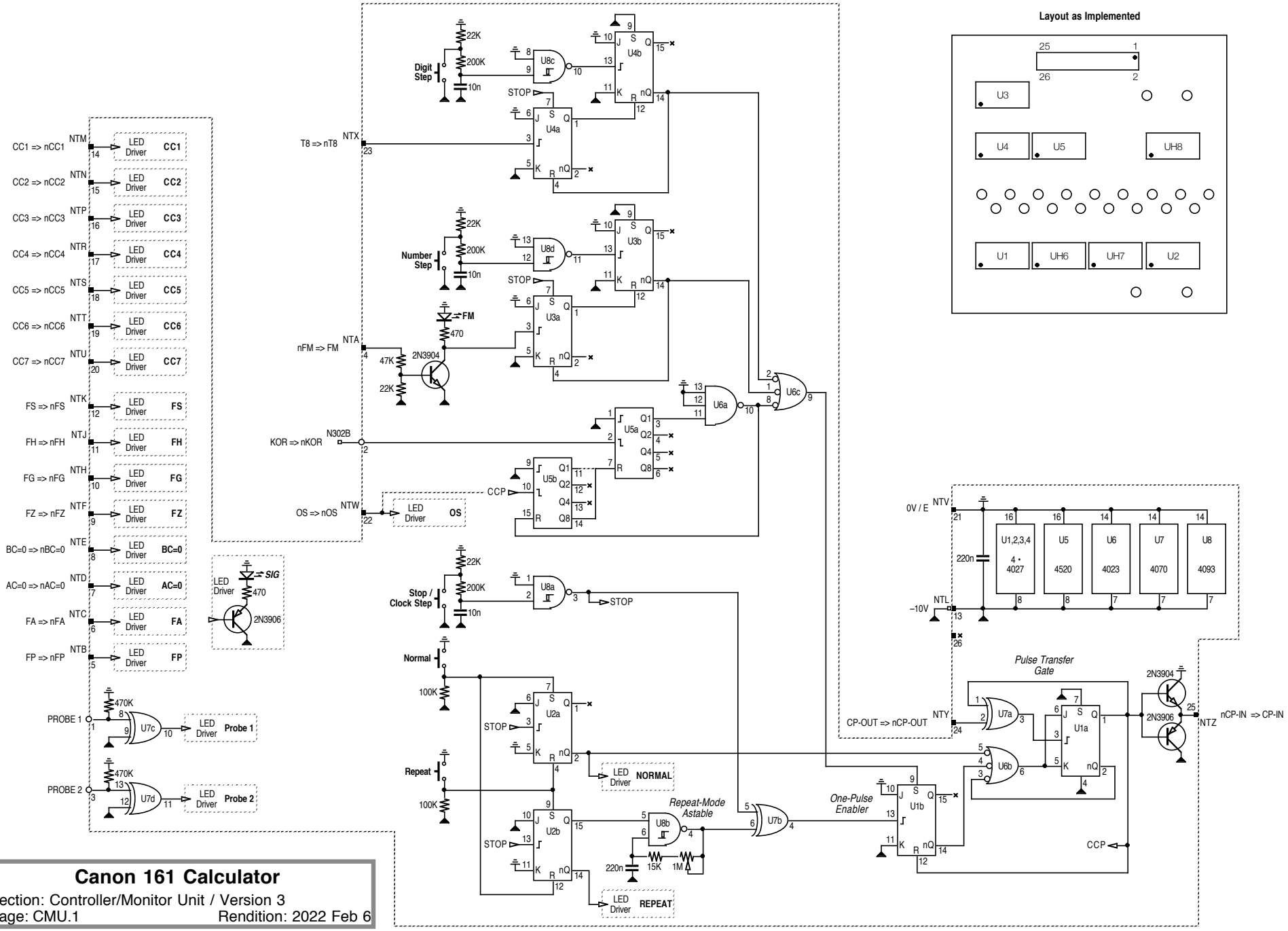




Canon 161 Calculator

Section: Board Layout - 38::40

Rendition: 2022 Feb 6



Canon 161 Calculator

Section: Controller/Monitor Unit / Version 3
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Notes

- This CMU diagram is drawn in terms of normal CMOS positive logic levels, in contrast to the negative levels of the 161. As such, there is an implicit logical inversion in the connection between the calculator and the CMU.

  CalcSig => nCmuSig

- Connector point NTL is unused on the calculator. It may be connected to –10V to supply the CMU, alternatively a clip-lead from the CMU may be used to connect to –10V.

- LED limiting resistors should be chosen appropriately for LEDs used.

- Alternatives to stop clock after keypress is registered:.
  - CP => U4.10, U4.14 => U4.7. Stop after 8 clock cycles.
  - OS => U4.10, U4.11 => U4.7. Stop on assertion of OS.

- Improvement: Add a Clock-Enabled LED driven by U6b.6.

- Bug: T-8 is derived from a ripple counter, glitches may stop the clock in the middle of the digit, requiring two presses per digit.

Other Servicing Notes

- A & B Counters may be monitored with LEDs with 2K resistors connected between the collector of the nQ transistors and –10V.

- The D Counter may be monitored by connecting 35B4 output (at 4.7K R near edge of board 35) to –10V.

Revision Log

- 2001 Jan: Version 1, original design and construction / bh.
- 2010 Nov: Version 2, Digit and Interval controls added / bh.
- 2021 Dec: Version 3, allow control over clocking when nFM / bh.

The Controller/Monitor Unit (CMU)

The 161 has an internal test connector which provides access to the master clock and most of the flag registers. Presumably there was originally a service unit to plug into this connector. The CMU is a newly-designed unit utilizing CMOS ICs. It provides monitors for the available flags along with manual control of the master clock.

The 161 uses a direct-drive display (not multiplexed) and static memory technology, consequently the clock can be slowed down or stopped without disrupting the display or state of the machine. The control aspect of the CMU functions by inhibiting the normal delivery of clock pulses in the 161. Installing the CMU and flipping the test-mode switch to the up position inserts a pulse transfer gate between the master clock of the 161 and the rest of the calculator. The functioning of this gate is controlled by the keys of the CMU and the keys of the calculator:

Calculator Keys:	The pressing of a calculator key enables clock pulses. This enables FK to clock and pick up the keypress from OS.ST. Clocking is disabled when OS is asserted.
Normal Calculator Mode (C):	Enables normal delivery of clock pulses.
Repeat Mode (R):	Repeatedly allows one clock pulse through the gate at a rate determined by the “Repeat Rate” control.
Stop / Clock Step (S):	Takes the CMU out of normal or repeat mode (stops continuous delivery of clock pulses) and allows one clock pulse through the gate per press.
Digit Step (D):	Enables clock pulse delivery till the end of the next digit cycle. Typically this will be 4 clock pulses, and will step the calculator thru one digit cycle.
Number Step (N):	Enables clock pulse delivery till the next end of a number cycle.

The pulse transfer gate is fully synchronised to the pulses from the master clock, permitting the mode to be changed at any time, between or during, execution of operations.

Using the CMU

1. Begin with the 161 turned off.
2. Plug the CMU edge connector into the test connector of the 161.
3. If NTL has not been connected to –10V, connect the CMU power lead to the blue (-10V) power supply connector.
4. Connect the KOR lead to N302B.
5. Flip the test-mode toggle switch of the 161 to the up position.
6. Turn the 161 on.
7. Press the “N” key of the CMU. The 161 should function normally.

When operating in other than normal mode, a key pressed on the 161 may need to be held down until the operation is complete. This is necessary for some operations because the calculator logic utilises the state of the keyboard during execution. The keyboard state is not fully latched at the beginning of an operation. Once the state machine makes it to CC2 and beyond, the key may be released, an exception being the Total key must be held down through CC7.

The Probe leads can be used to monitor other signals in the 161. The probes may not be valid for (and probably should not be connected to) the output of OR gates due to the +10 bias on such outputs, as this may pull a CMOS input below Vss of the IC.