Canon 163 Calculator

Schematic

Contents

Appendix

Notes

♦ Gate symbols and signal names are presented in accordance with:
logic 0 = 0V, GND
logic 1 = +5V

♦ The symbol *bspp* denotes a physical connector pin where *b*=board (K,1–8), *s*=section (A,B,C,D), and *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.

♦ ——▶ ▶—— connection between different sections.
——▷ ▷—— connection limited to same section.
Arrows indicate direction of signal or energy flow.

♦ The symbol ▼ denotes V+5. The symbol ⏃ denotes V–5.

♦ These drawings based on unit with serial number 122900. These drawings should also apply to the Monroe 990.

Log

♦ 2005 Jan Initial drawing / bhilpert.
♦ 2014 Format updates, basic state sequence timing diagram/ bh.
♦ 2021 Mar Logic presentation improvements – negative logic gates, organisation refinement /bh.
♦ 2024 Jan Extensive improvements , appendix and Theory of Op documents.
To do: convert to ~ NOT notation, complete expander–diode inclusion in gate symbols.

Gate Identification

Gates are identified by symbols taking the following form:

bree

where

b = Board 1 to 8

r = Row 1 to 3

ee = Enumeration 1 to n

Signal Names

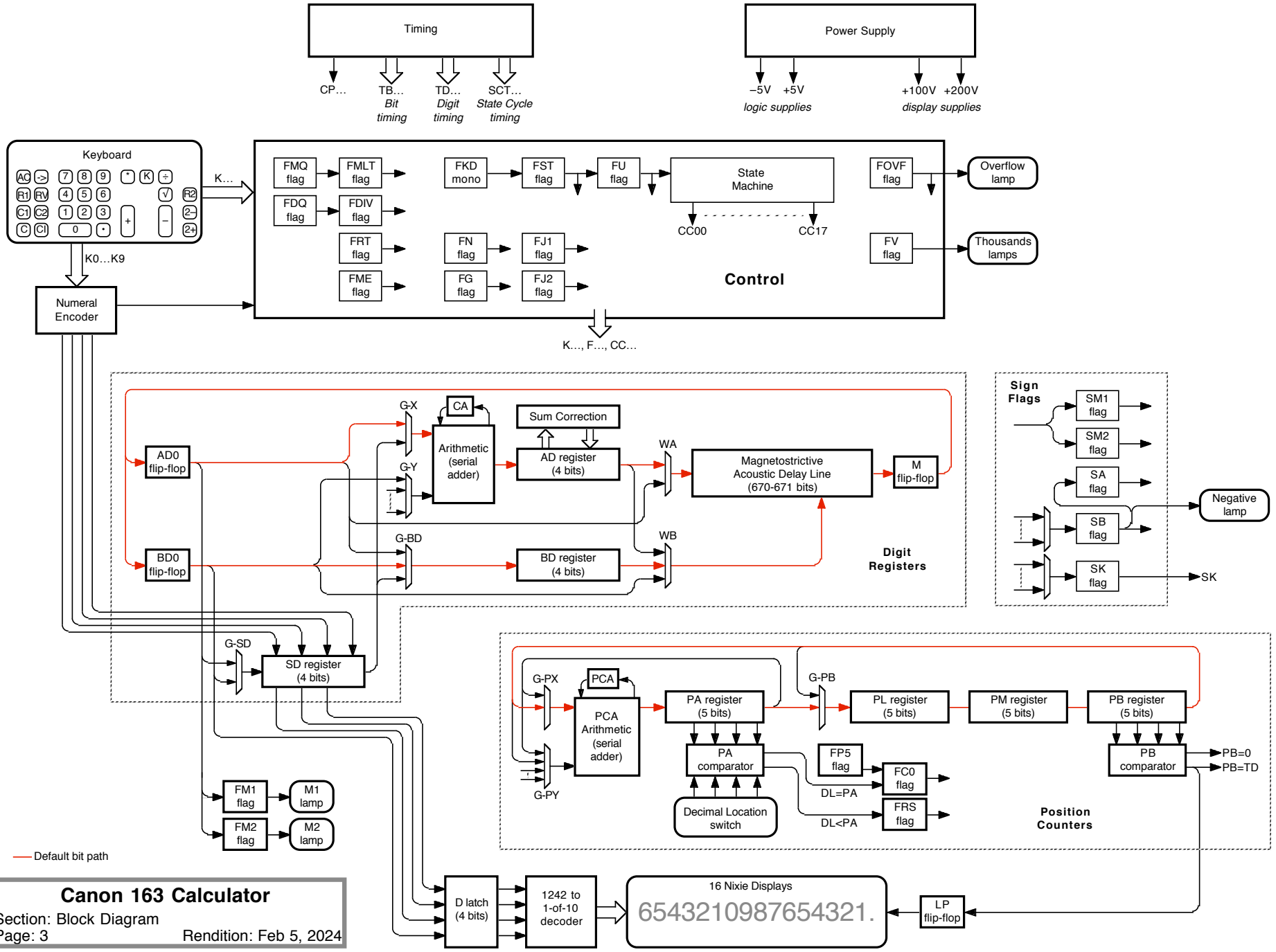
Many signal names were obtained from labels on the printed circuit boards. Not all signals have such labels however, so the following names have been created for this schematic:

CPR	K(M+D)	FST	LDNML	PASUM
CPW	KRM(1+2)	F(MQ+DQ)	nSUM<0	PA
TDBx	K(C+CI+CM)	F(M+D)	M	PB1
SCT01		F(M+D+R)	RSUM	PB2
SCT12		F(D+R)	CA	PB=TD
SCT34		n(KOP•FU)		
nTD0+TB3		nENDSP		
		nENDLP <== nEND		
		nENDP <== nEND2		
		en…		
		@…		

Sections and Signal Descriptions

A lowercase "n" at the beginning of a signal name indicates the logical NOT operation.

Section	Signal	Description
Timing	CPR	Read clock, rate at which bits are retrieved from the acoustic delay line (500KHz).
	CPA	The bit clock, rate at which bits are processed (250KHz).
	CPW	Write clock, a narrow pulse to form the bit pulses written to the acoustic delay line.
	CPC	Clock for Point Counters.
	TB0	Clock pulse to define bit 0 of digits.
	TB3	Clock pulse to define bit 3 (W) of digits.
	TD0	Clock pulse to define digit 0 (LSD) of numbers. There are 17 digit periods. Bits of the displayed digits are contained in periods 0 to 15 and displayed during periods 1 to 16.
	TD16	Digit 16 (MSD) clock period.
	SCT0–4	State Cycle phases. There are 5 phases to a state cycle, each being a number cycle of 17 digits.
	TP0	The first bit in a number cycle.
	TP67	The last bit in a number cycle (17•4–1).
Keyboard	K…	The keyboard and numeral encoder.
Control	CC00::CC17	The states of the procedure execution state machine.
	FST	Procedure start.
	FU	Procedure initiation pulse.
	FMLT	Multiply operation.
	FDIV	Divide operation.
	FRT	Square Root operation.
	FME	M2 Add/Subtract or M2–Sum operation.
	FN	New number in display.
	FG	For constant mode, indicates a constant operand is in RA.
	FJ1	– DP has been pressed during number entry. – Number went negative during subtract, held till EOS.
	FJ2	– Delayed action indicator for DP alignment. – 2–iteration loop counter for complementing negative results. – During SQRT, loop counter for double subtractions.
	FC0	Temporary used during DP alignment.
	FRS	Direction of shift during DP alignment. 1 is RIght–Shift (down).
	FOVF	Overflow flag.
	FM1,FM2	Flags to control the Memory 1 & 2 lamps
	FV	Flag to control the thousands–separator lamps.
	@…	Assorted control signals, otherwise unnamed, name derived from IC output pin.
Signs	SA	Sign of A register.
	SB	Sign of B register.
	SK	Sign flag that is actually used to determine add or subtract .
	SM1	Sign of Memory 1 register.
	SM2	Sign of Memory 2 register.
Memory	WA	Bit stream of A,C,D,M1,M2 registers to be injected into the acoustic delay line.
	WB	Bit stream of B register to be injected into the delay line.
	BD0	Bit stream of B register from the delay line.
	AD0	Bit stream of A,C,D,M1,M2 registers from the delay line.
	BD	A 4–bit register, part of the B register bit stream.
	SD	A 4–bit register used for keyboard input, display output and shifting.
Arithmetic	RSUM	Raw (uncorrected) binary sum from the adder.
	AD	A 4–bit register in which 1242 decimal sum correction is performed, and part of the A,C,D,M1,M2 bit stream.
	ACA	Carry output from the adder.
	CA…	Signals associated with the arithmetic carry flag.
PA Register	PA	Bit stream output from the PA register.
	DL=PA	
	DL<PA	Relationshsips between the PA register and the selected number of decimal points.
PB Register	PB…	Bit stream outputs from the PB register.
	PB=0	
	PB=TD	1 when the digit counter hits the decimal point digit.
	LP	A latched version of PB=TD to turn on the decimal point for the appropriate digit.



Canon 163 Calculator

Section: Block Diagram

Page: 3

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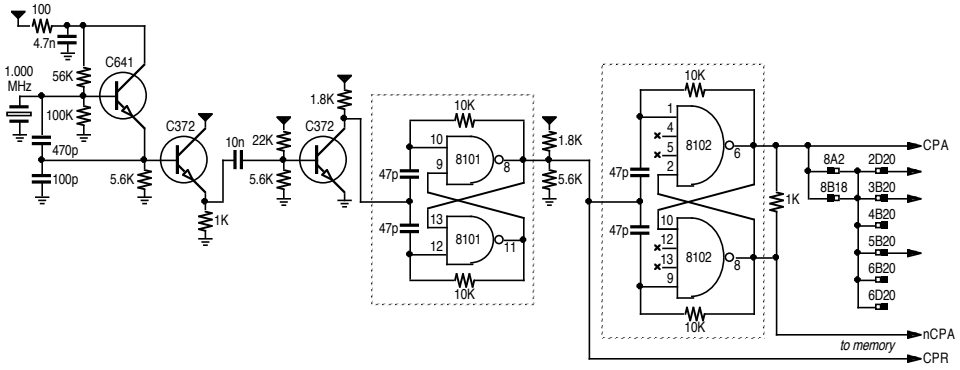

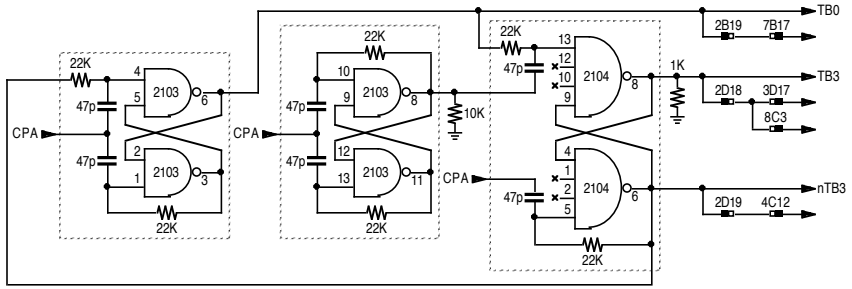

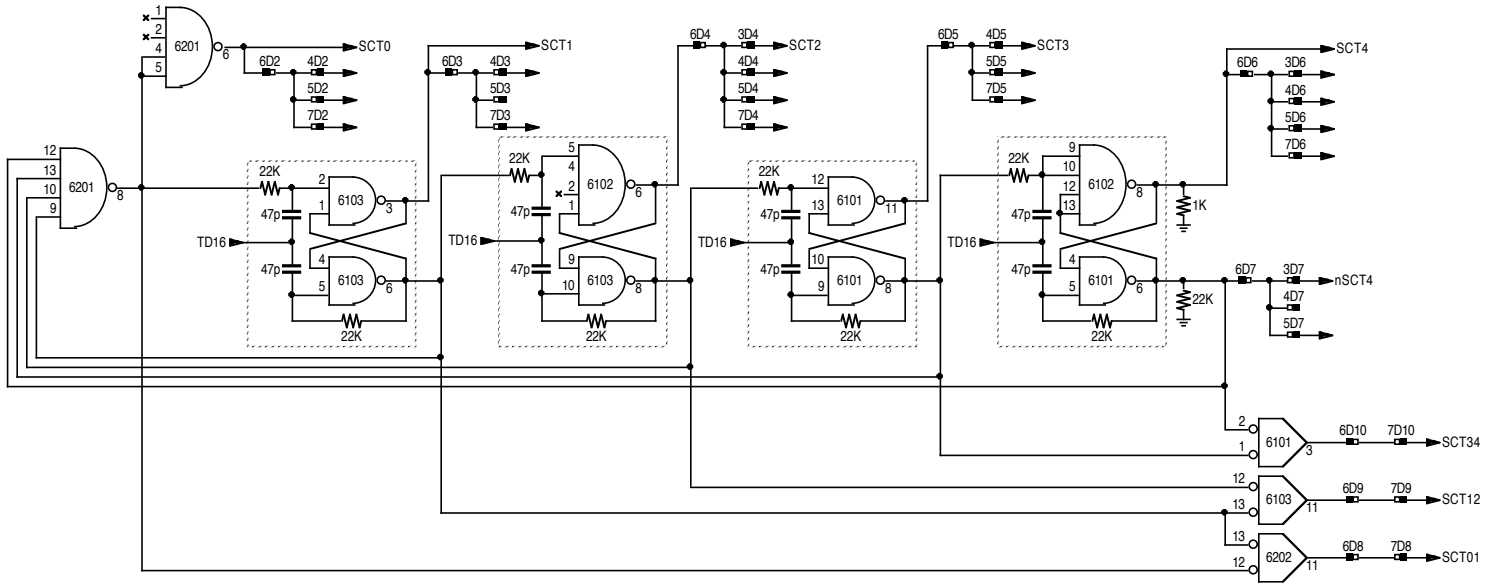

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Section: Timing - Bit & State

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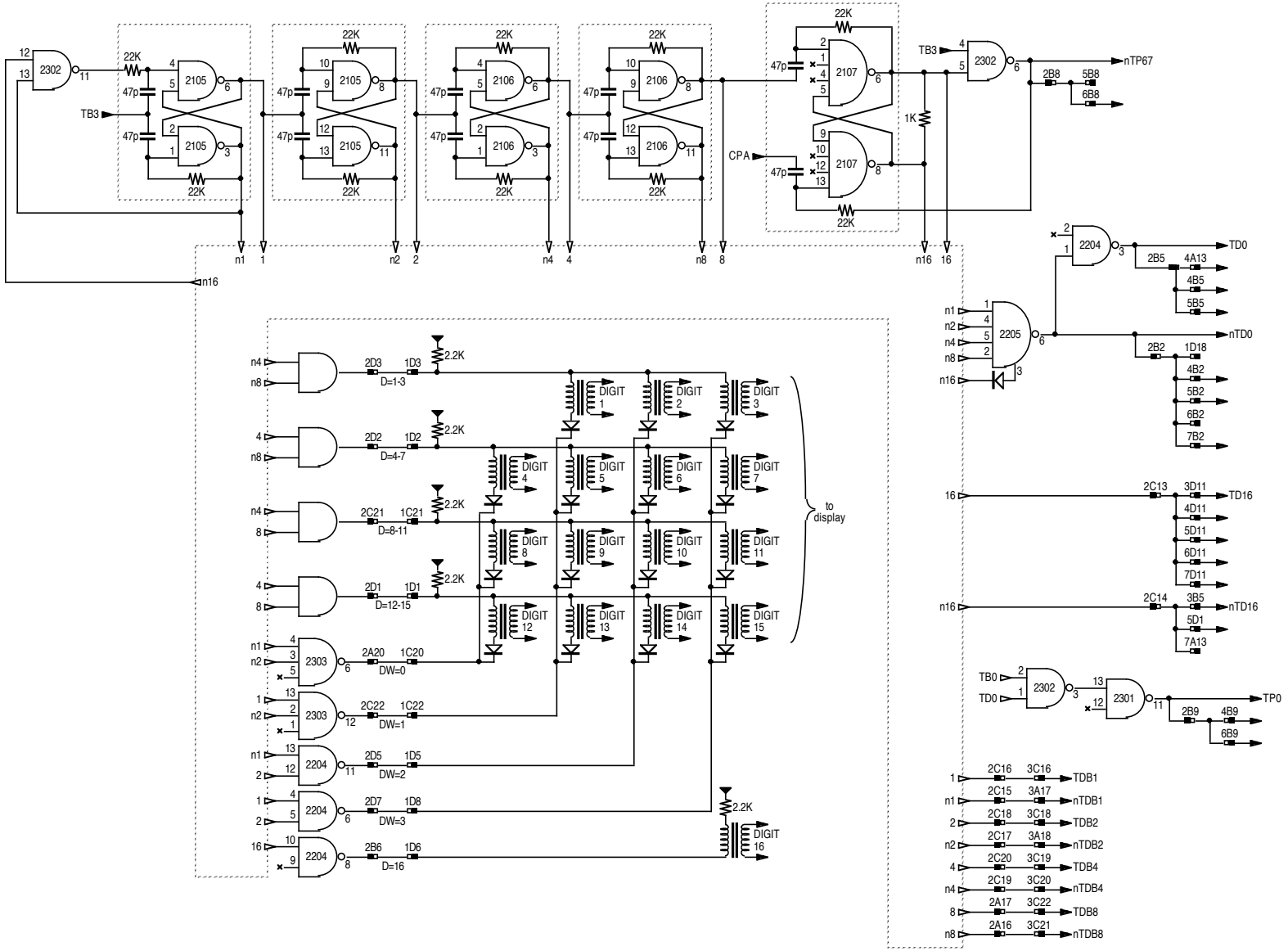

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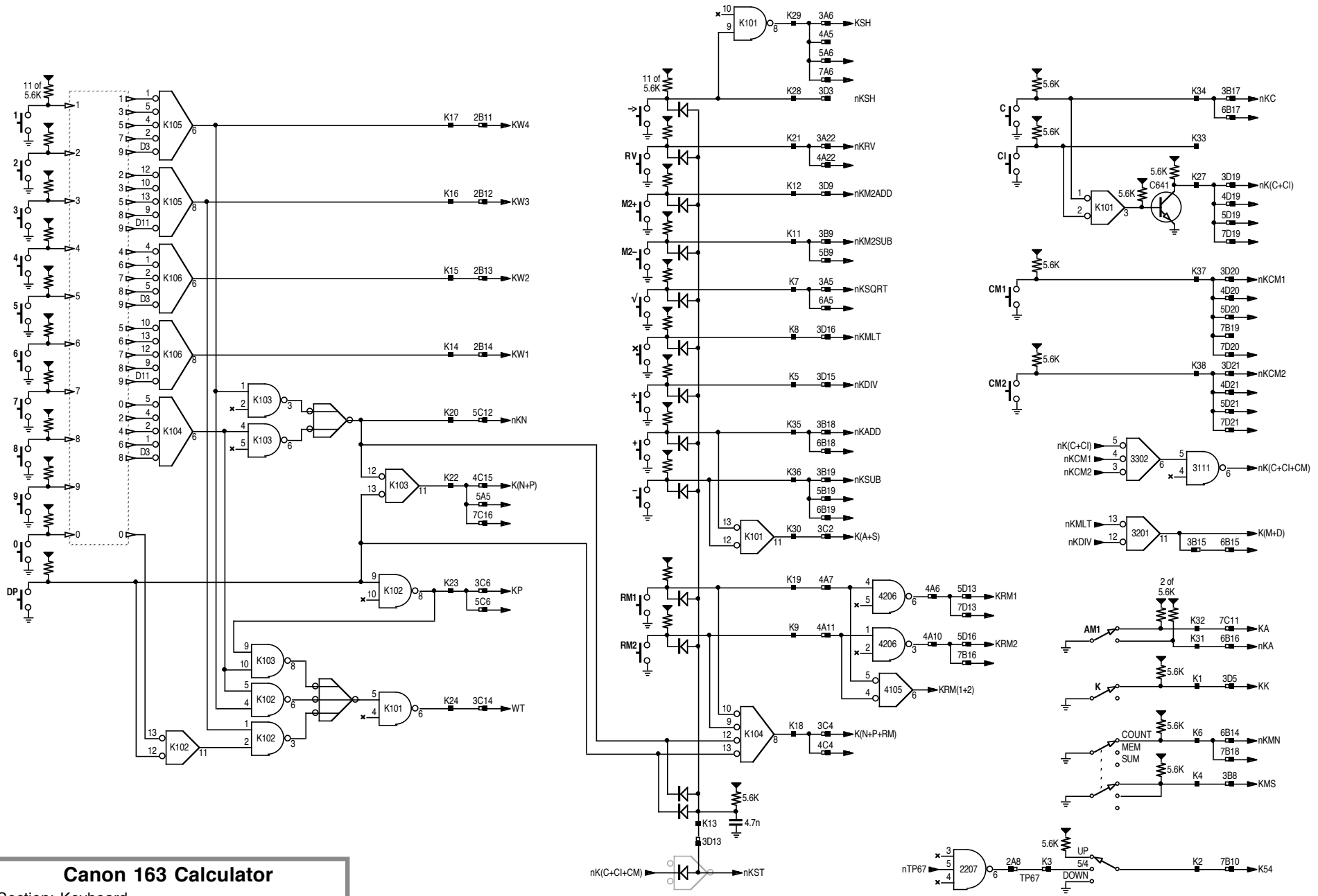
Section: Timing - Digit

Page: 5 Rendition: Feb 5, 2024



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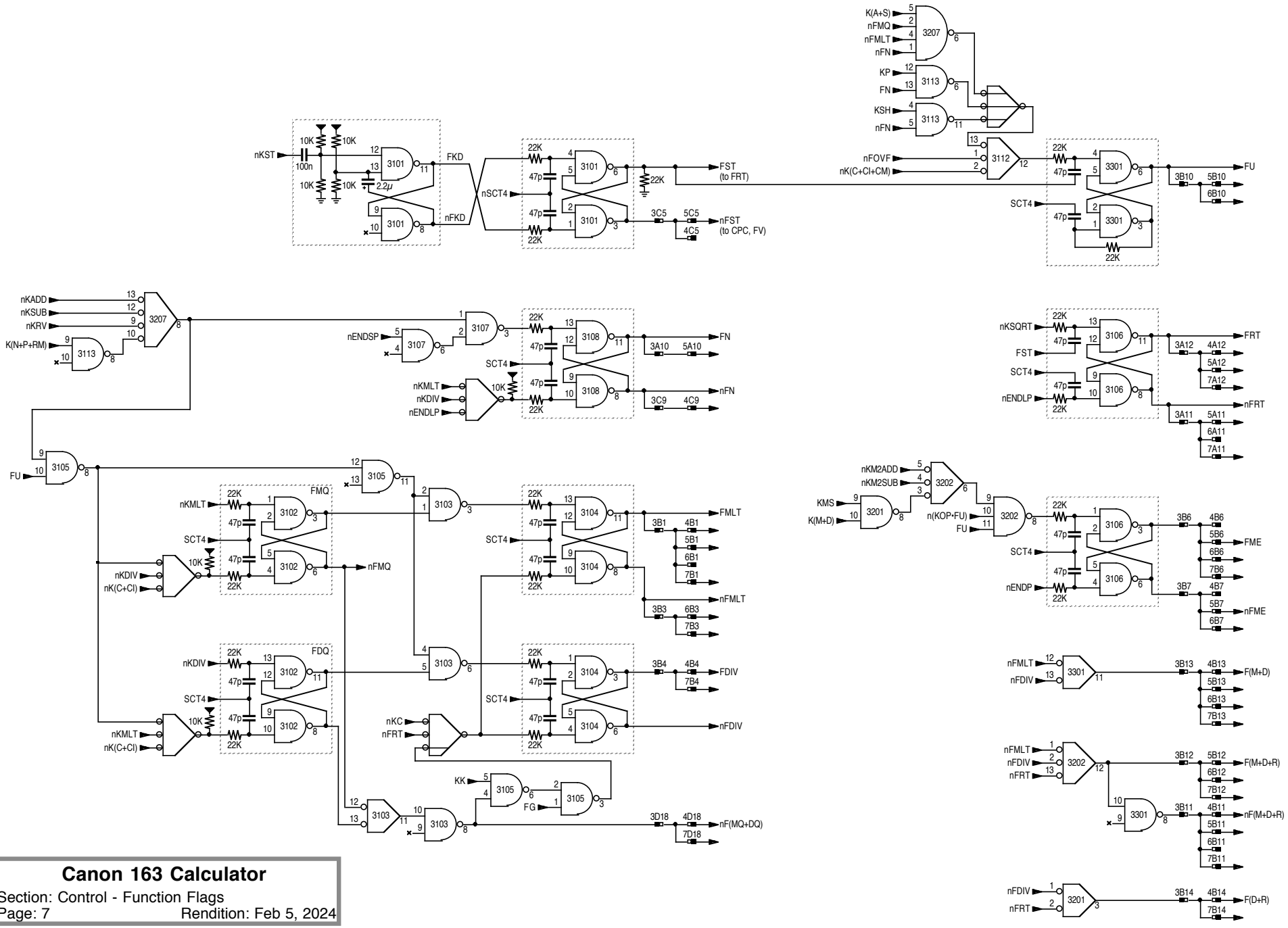
Section: Keyboard

Page: 6 Rendition: Feb 5, 2024



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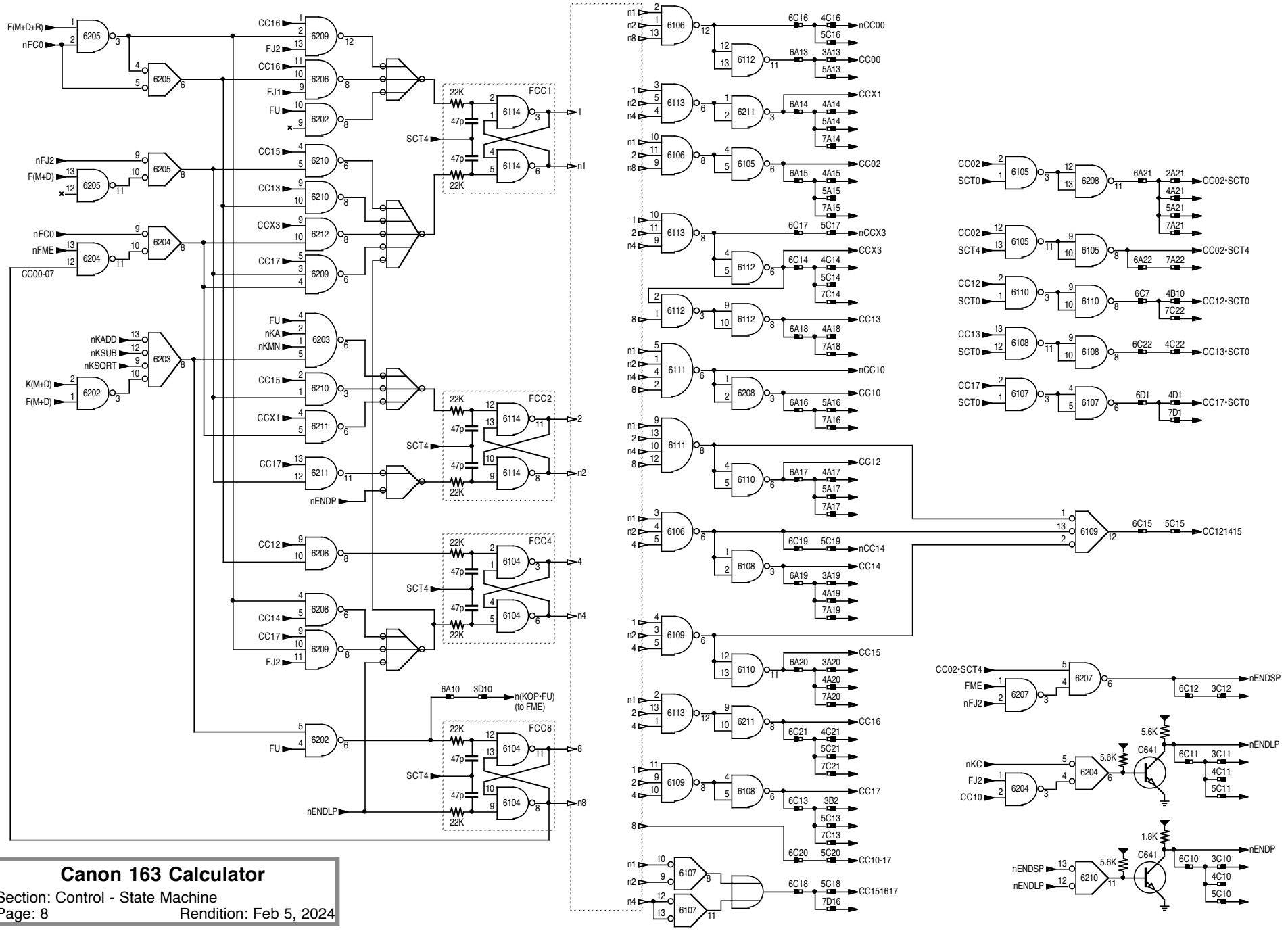
Section: Control - Function Flags

Page: 7 Rendition: Feb 5, 2024



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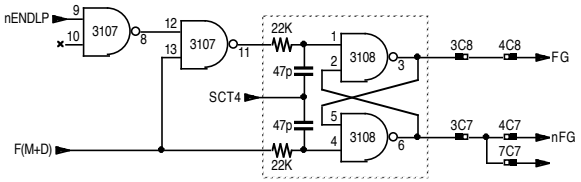
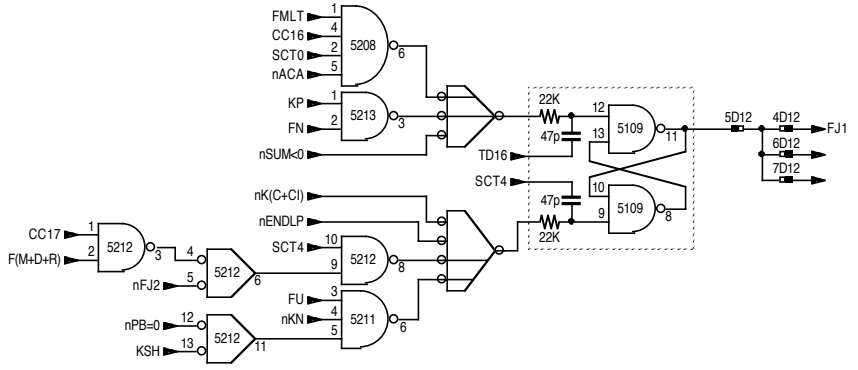
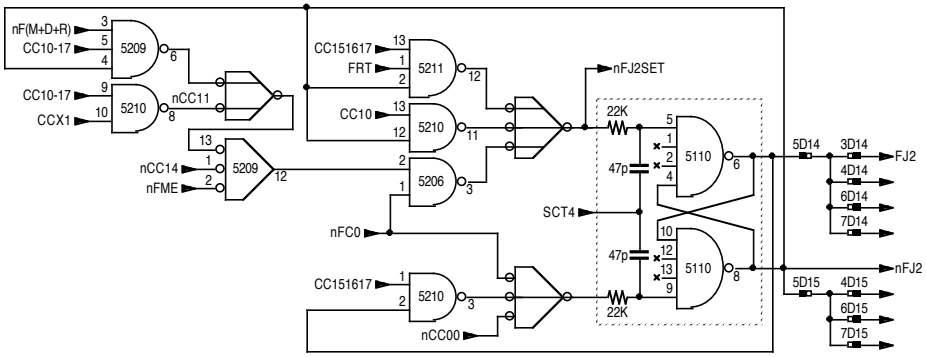
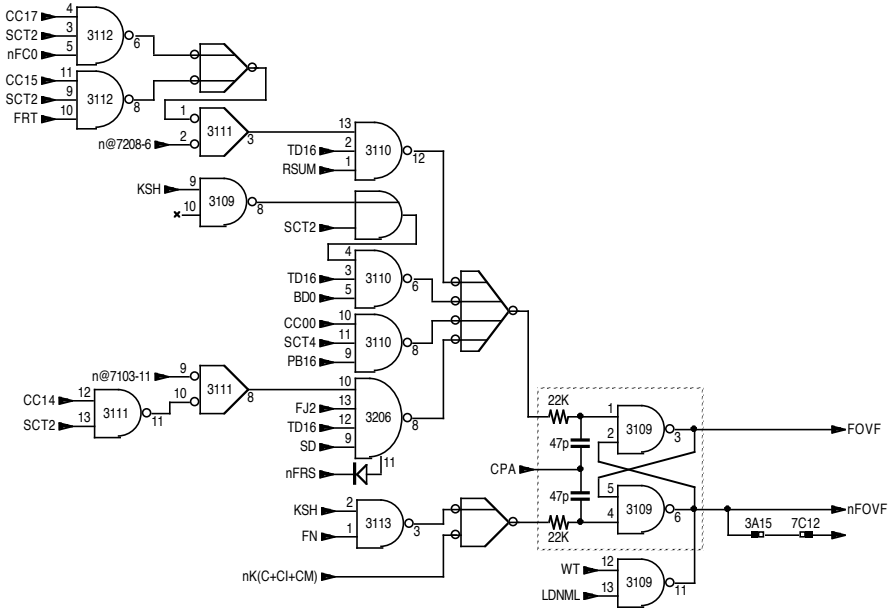
Section: Control - State Machine

Page: 8 Rendition: Feb 5, 2024









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Section: Control - Misc. Flags

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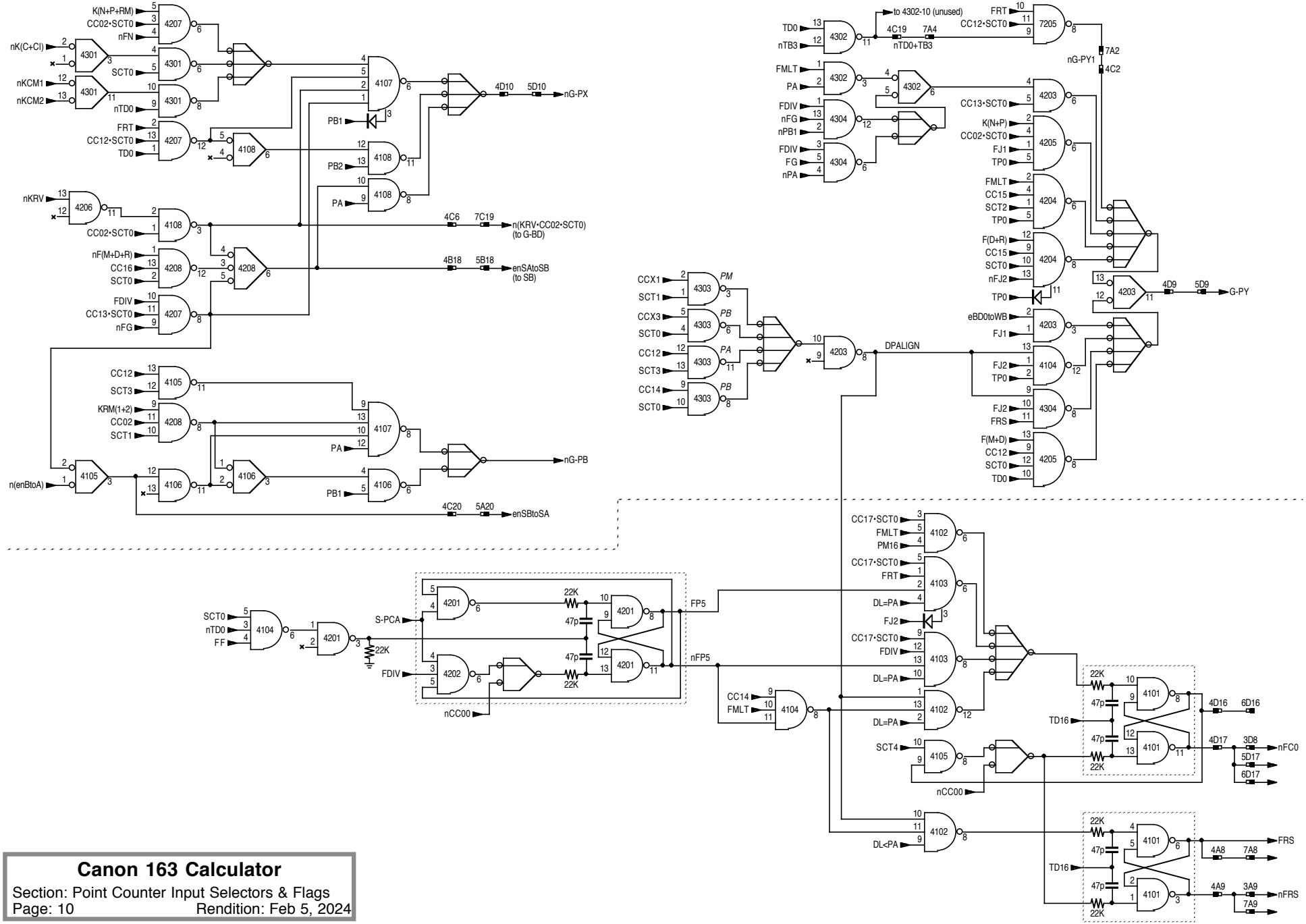

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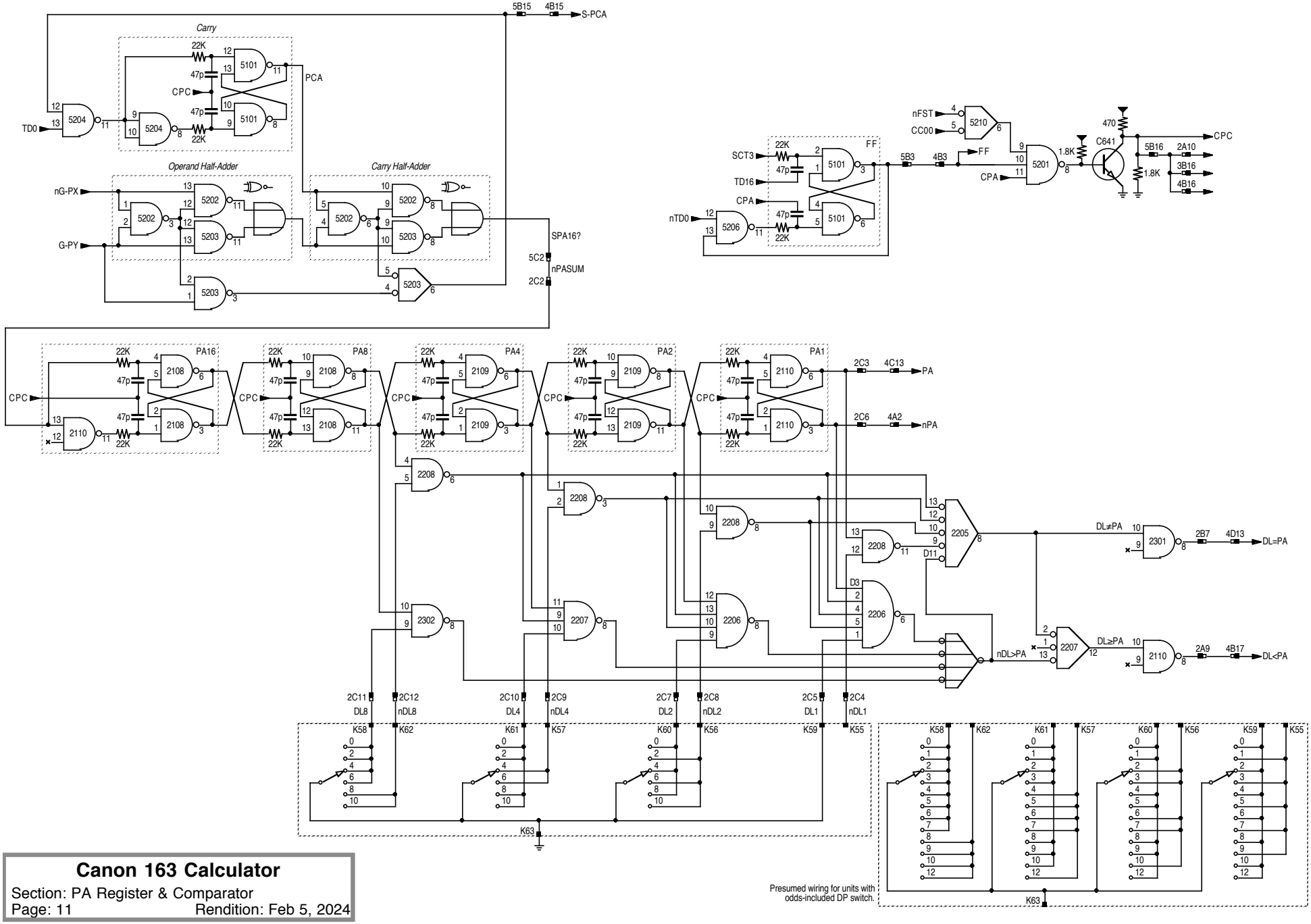
Section: Point Counter Input Selectors & Flags

Page: 10 Rendition: Feb 5, 2024



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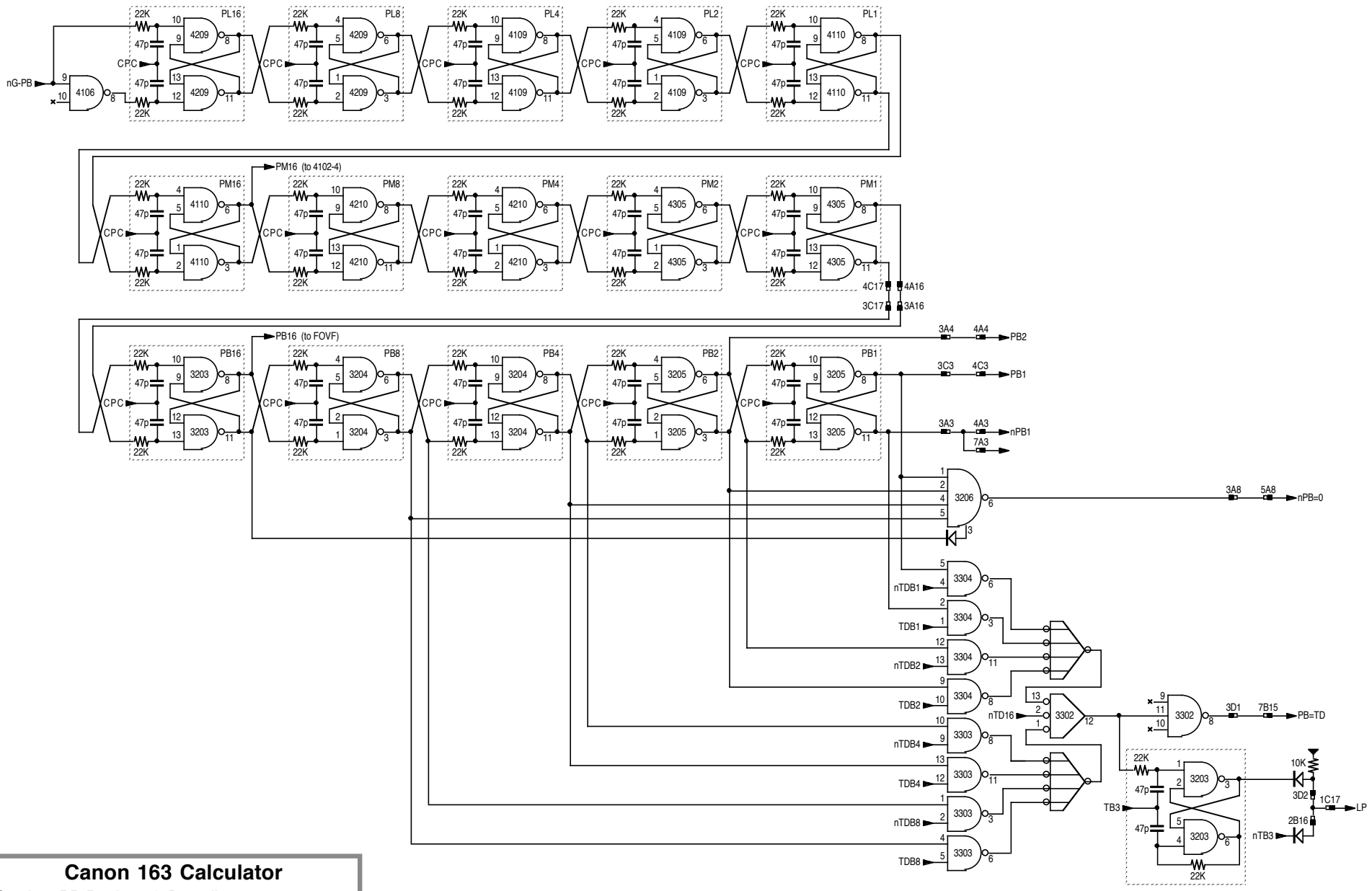
Section: PA Register & Comparator

Page: 11 Rendition: Feb 5, 2024



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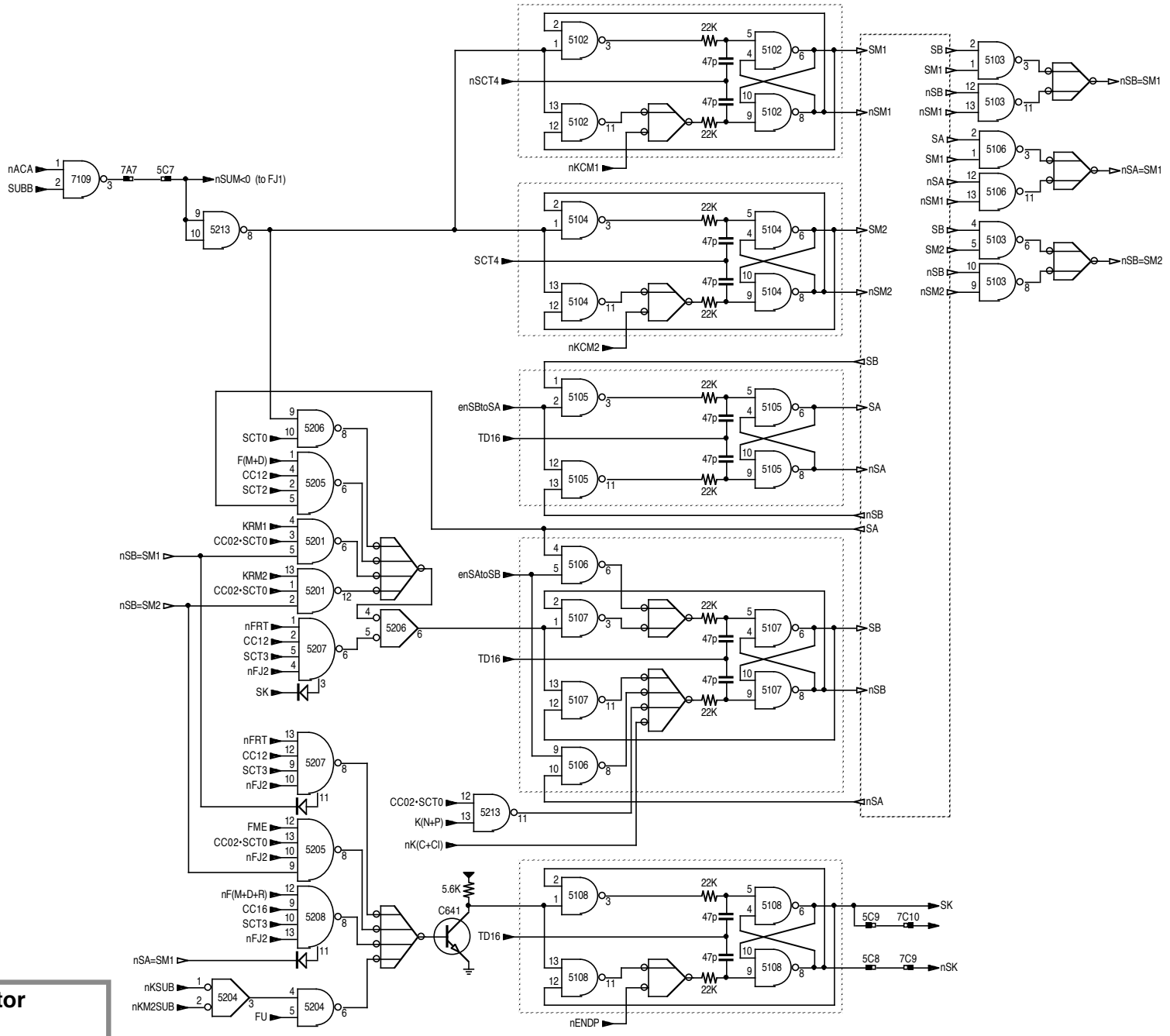
Section: PB Register & Decoding

Page: 12 Rendition: Feb 5, 2024



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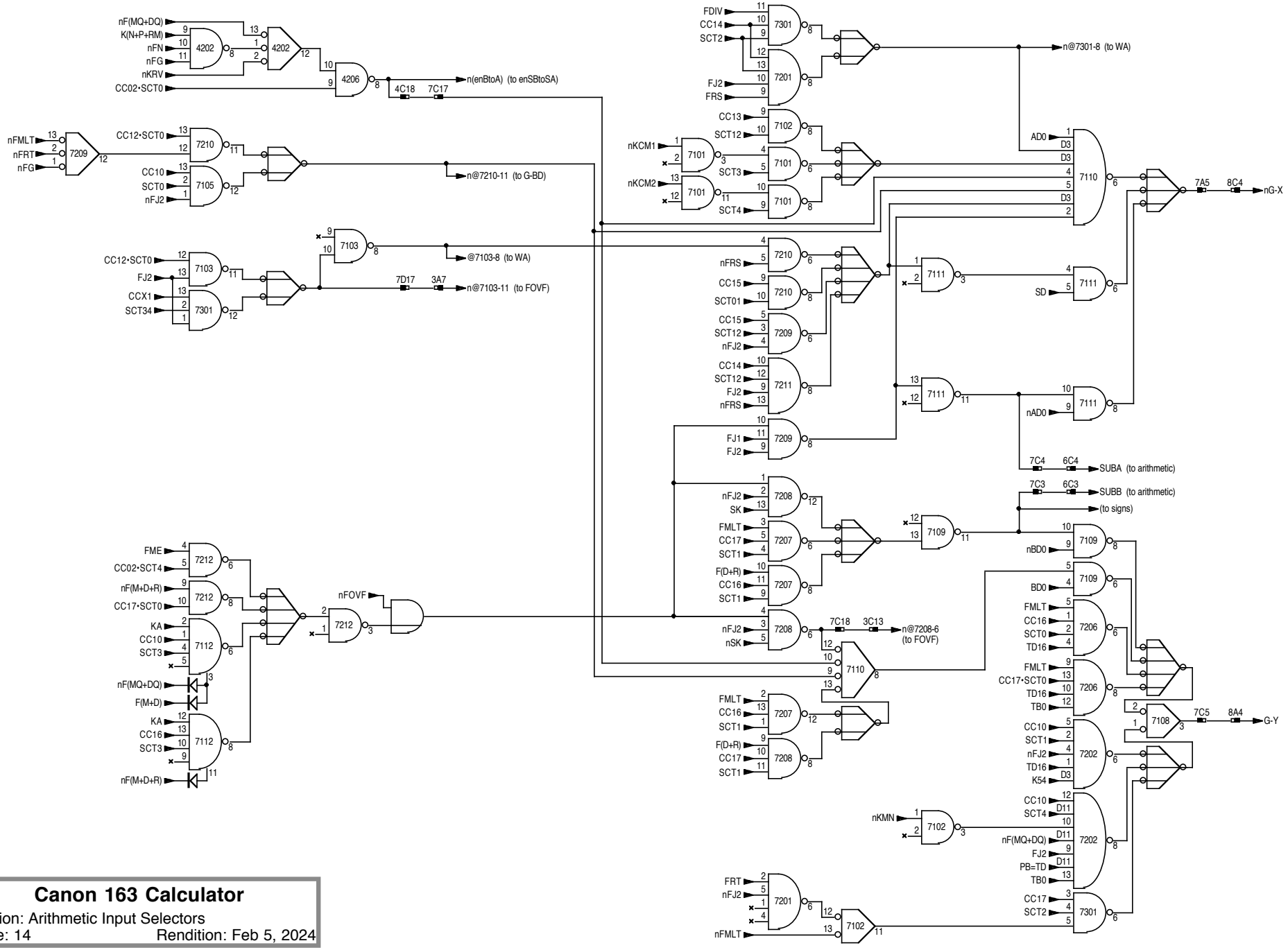
Section: Sign Flags

Page: 13 Rendition: Feb 5, 2024



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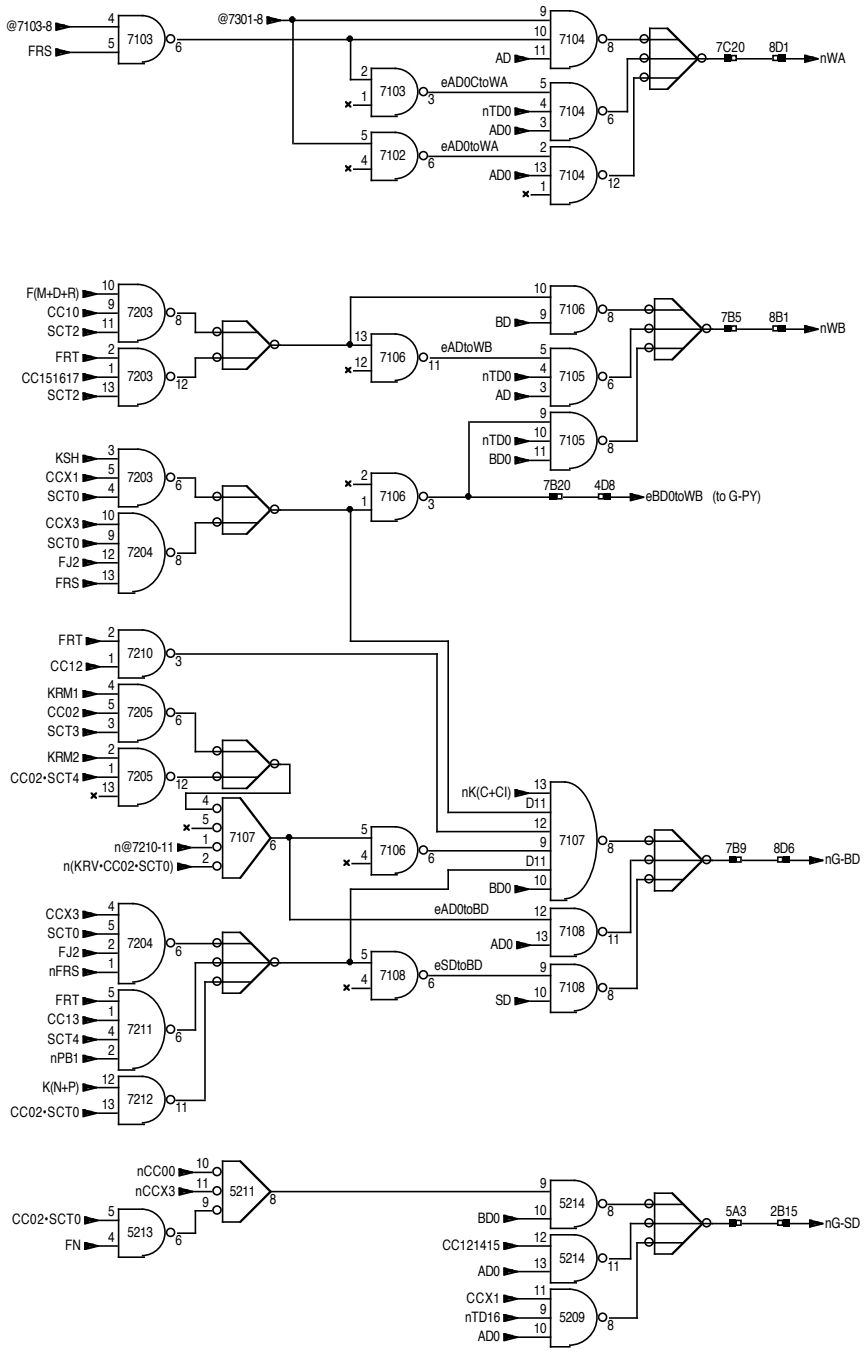
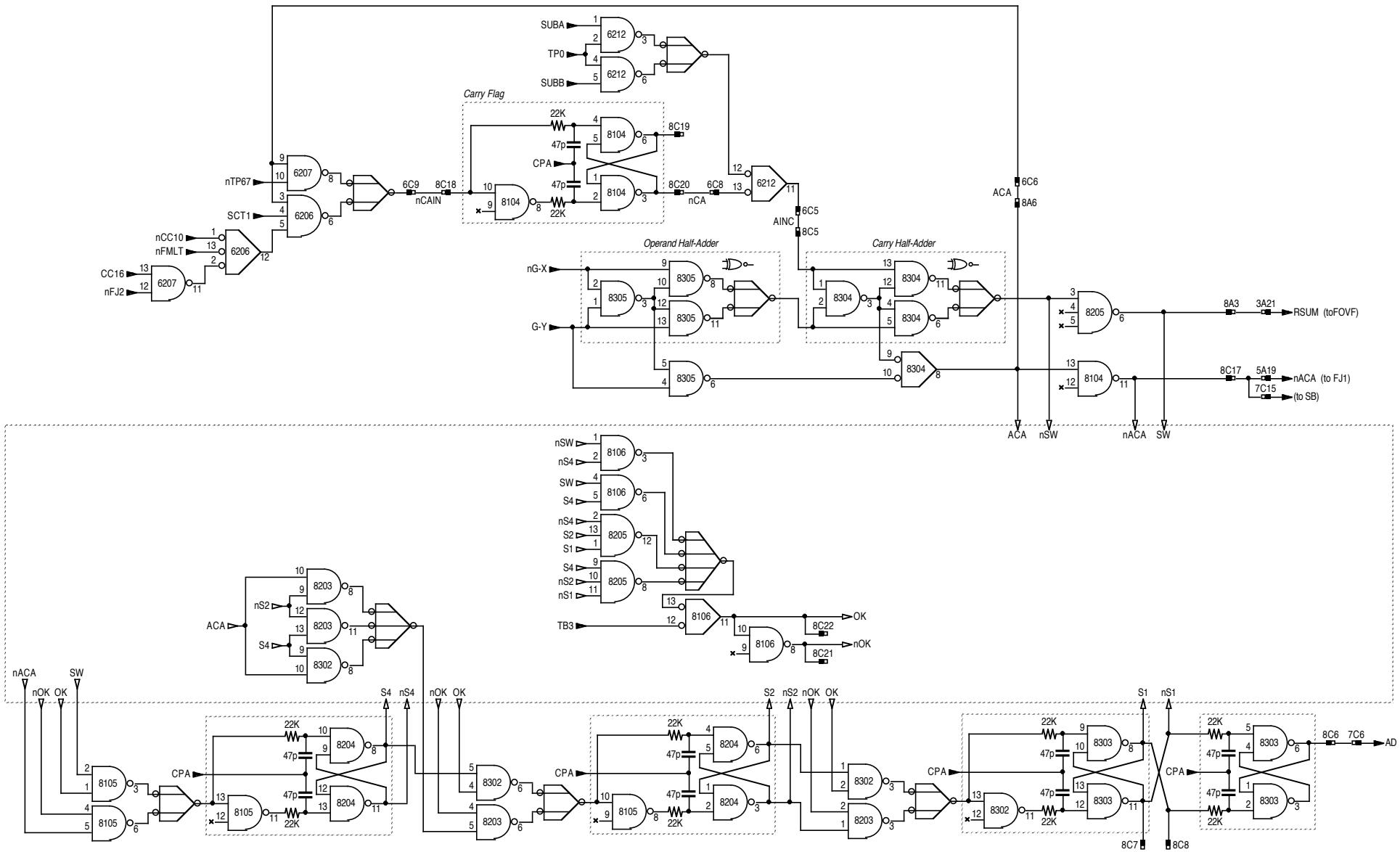
Section: Arithmetic Input Selectors

Page: 14 Rendition: Feb 5, 2024


@7103-8
FRS
7103
@7301-8
7103
eAD0CtoWA
7102
eAD0toWA
7104
AD
7104
nTD0
AD0
7104
AD0
7C20
8D1
nWA
F(M+D+R)
CC10
SCT2
FRT
CC151617
SCT2
7203
7203
7106
eADtoWB
7106
BD
7105
nTD0
AD
7105
nTD0
BD0
7B5
8B1
nWB
KSH
CCX1
SCT0
CCX3
SCT0
FJ2
FRS
7203
7204
7106
7B20
4D8
eBD0toWB (to G-PY)
FRT
CC12
KRM1
CC02
SCT3
KRM2
CC02•SCT4
7210
7205
7205
7107
n@7210-11
n(KRV•CC02•SCT0)
7106
nK(C+CI)
D11
D11
BD0
7107
7B9
8D6
nG-BD
CCX3
SCT0
FJ2
nFRS
FRT
CC13
SCT4
nPB1
K(N+P)
CC02•SCT0
7204
7211
7212
7108
eSDtoBD
eAD0toBD
AD0
SD
7108
7108
nCC00
nCCX3
CC02•SCT0
FN
5211
5213
5214
BD0
CC121415
AD0
CCX1
nTD16
AD0
5214
5209
5A3
2B15
nG-SD



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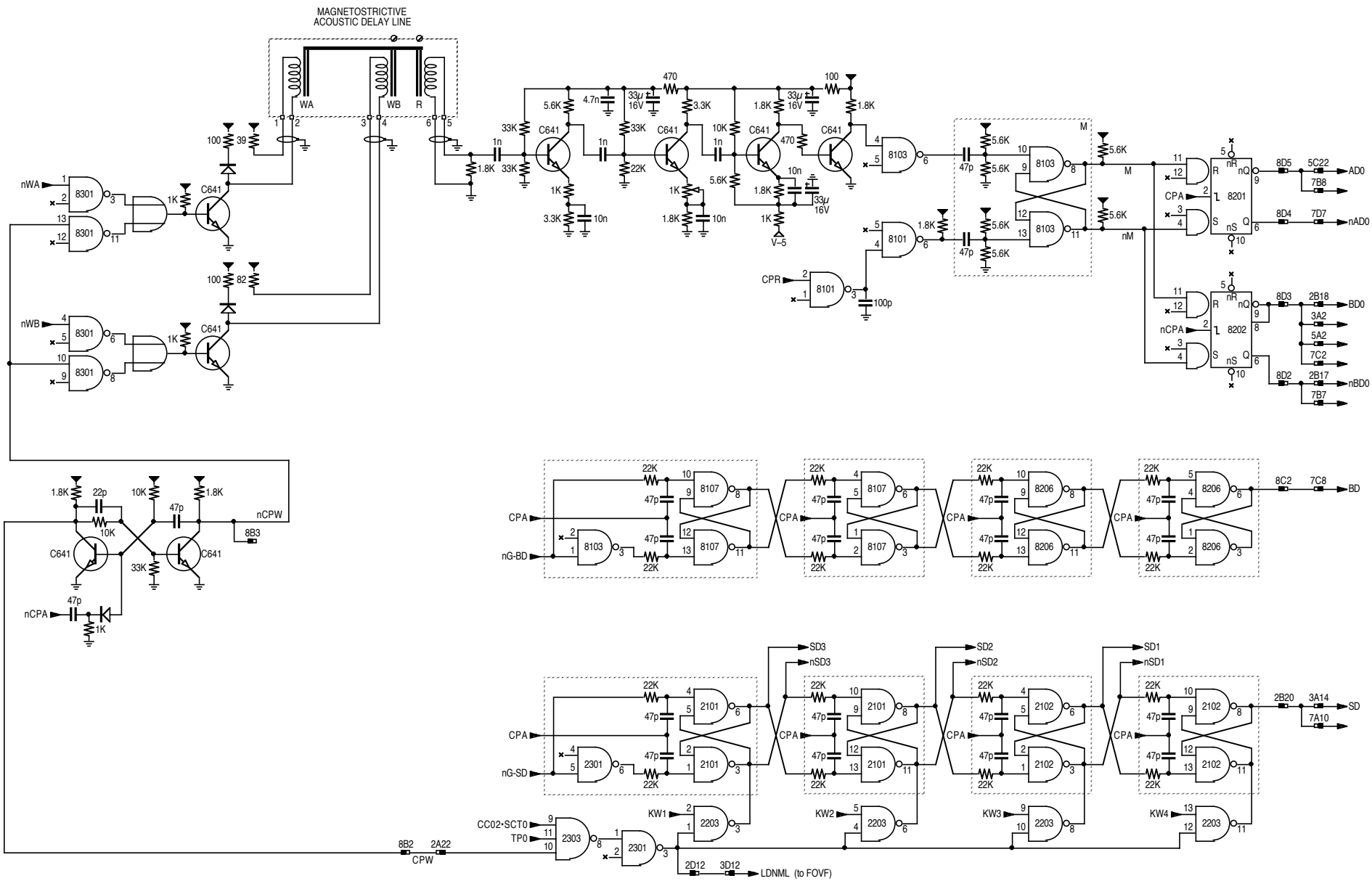
Section: Arithmetic

Page: 16 Rendition: Feb 5, 2024



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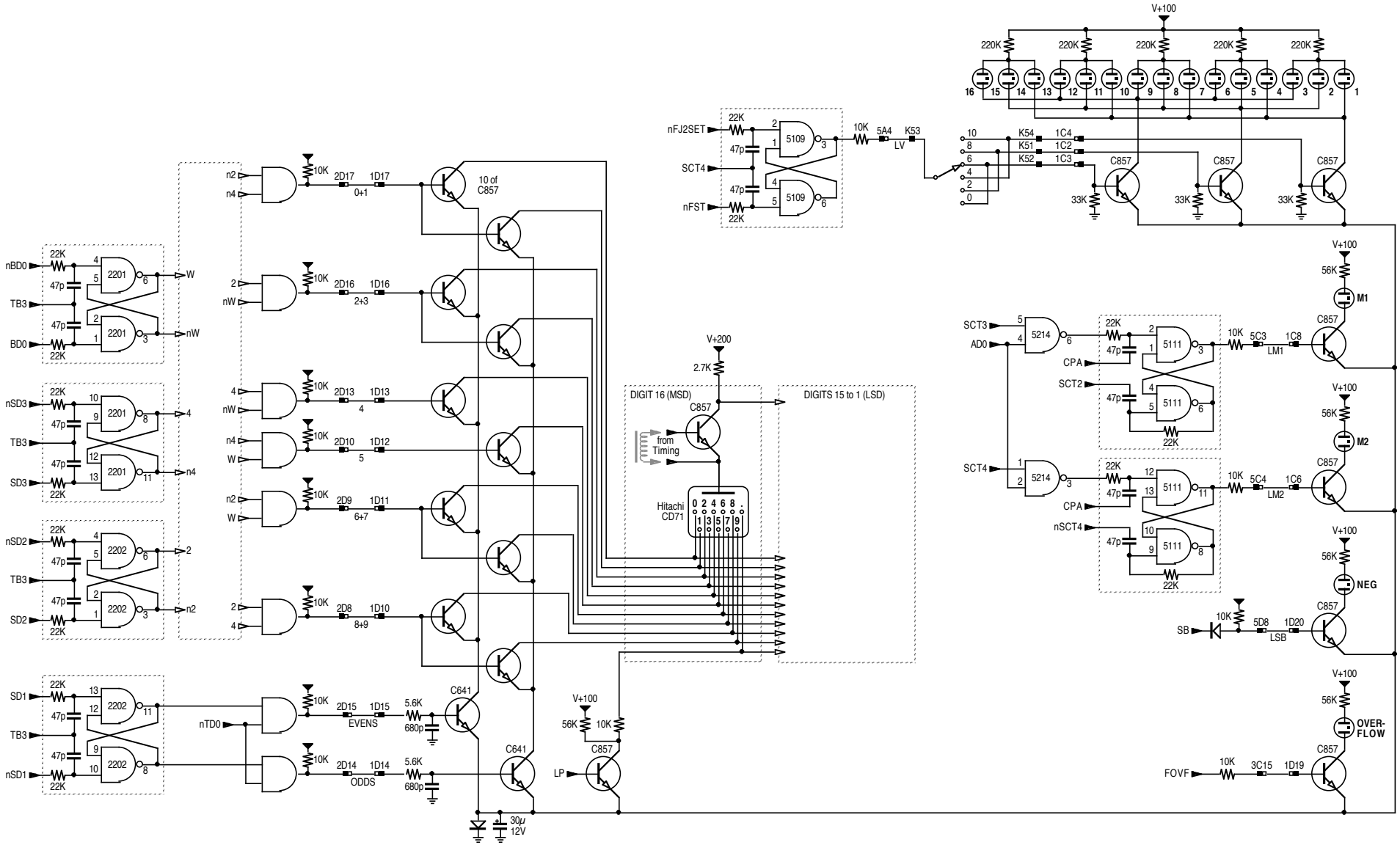
Section: Memory

Page: 17 Rendition: Feb 5, 2024



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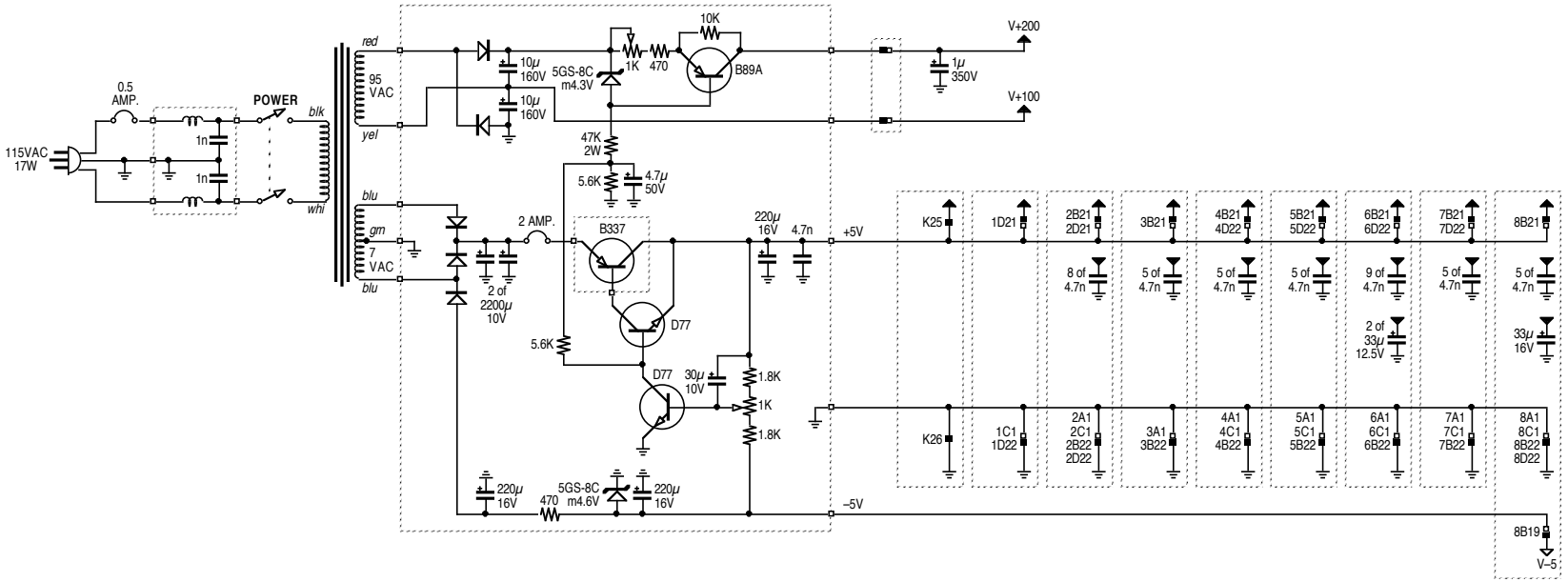
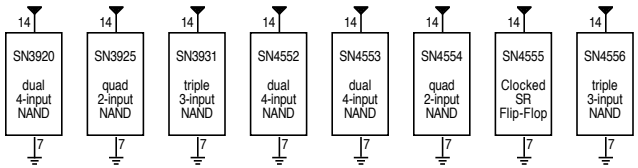
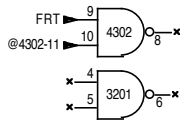
Section: Display

Page: 18 Rendition: Feb 5, 2024





Unused Gates

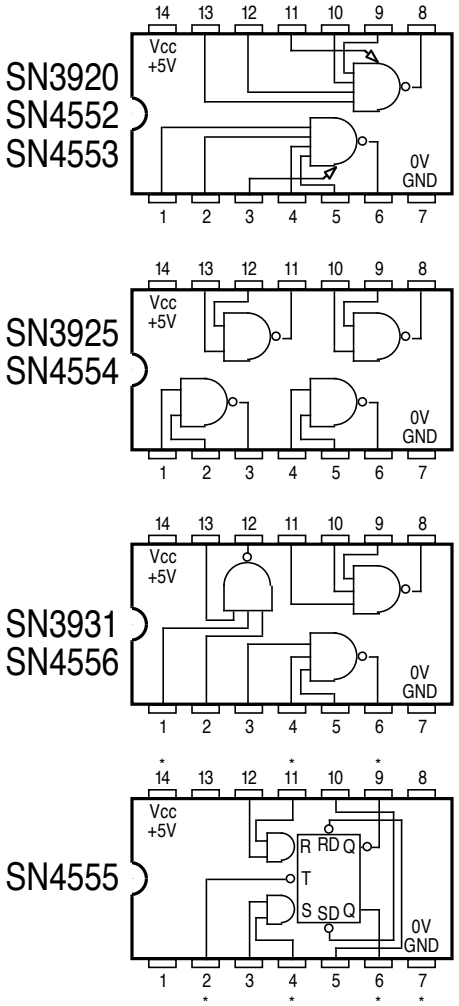


Canon 163 Calculator

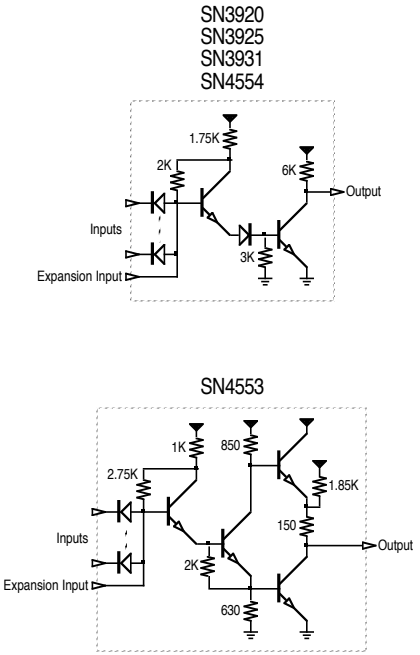
Section: Power Supply

Rendition: Feb 5, 2024

SN3900 / 4500 Series DTL IC Pinouts



SN3900 / 4500 Series DTL Gate Construction



800/900-Series DTL Equivalents

SN3920	930	Fair69.3-116
SN3925	946	Fair69.3-116
SN3931	962	Fair69.3-116
SN4552		
SN4553	932	Fair69.3-118
SN4554	946	Fair69.3-116
SN4555	*see comment	
SN4556		

The pinout for SN4555 has been inferred through reverse engineering and by matching the pins utilised in the 163 to the pinout of the following ICs: 831/931, 845/945 & 848/948 DTL clocked flip-flop.
The pins marked with '*' are those utilised in the 163.

Refs:
- Motorola Semiconductor Data Book, 4th Edition, 1969, pg. IC-49
- Fairchild 1969, pg 3-5, 3-116::119).

Board Contents

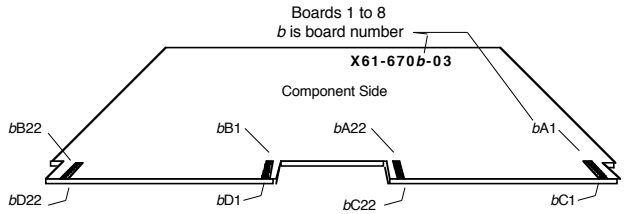
Board Contents

1	• display & drivers • numeral decoder
2	• TB & TD counters • display latch • SD register • PA register & comparator
3	• FST, FN, FU, FG, FMLT, FDIV, FRT, FME function flags • FOVF flag & overflow detection • portion of PB register & PB decoding
4	• FC0 & FRS flags • PA & PB input gates • portion of PB register • portion of arithmetic input gating
5	• FF flag & CPC gating • SA, SB, SK, SM1, SM2 sign flags • FJ1, FJ2, FV, FM1, FM2 flags • SD input gate • PA adder & PCA flag
6	• SCT counter • CC state machine (latches, decoding & sequencing)
7	• input gates for arithmetic, memory & BD
8	• clock • memory interface • adder with CA flag & AD sum correction • BD register

Odd/Incorrect Labels

pin	label	actually
5B1	FD16	FMLT
5C20	01	CC10-17
5B18	12	
5A17	SCT2	CC12
7C22	SK	CC12•SCT0
7D17	OC13	
4110-6	nPC1	PM16

Board Orientation



IC	3920	3925	3931	4552	4553	4554	4556
K101		•					
K102		•					
K103						•	
K104	•						
K105	•						
K106	•						
	3	2	0	0	0	1	0
2101		•					
2102		•					
2103						•	
2104					•		
2105						•	
2106						•	
2107					•		
2108		•					
2109		•					
2110		•					
2201						•	
2202						•	
2203		•					
2204		•					
2205				•			
2206	•						
2207			•				
2208						•	
2301						•	
2302		•					
2303			•				
	1	8	2	1	2	7	0
3101		•					
3102		•					
3103		•					
3104						•	
3105		•					
3106						•	
3107		•					
3108						•	
3109		•					
3110							•
3111		•					
3112							•
3113		•					
3201		•					
3202							•
3203		•					
3204		•					
3205						•	
3206				•			
3207	•						
3301						•	
3302			•				
3303		•					
3304		•					
	1	13	1	1	0	5	3

IC	3920	3925	3931	4552	4553	4554	4556
4101						•	
4102							•
4103				•			
4104							•
4105		•					
4106		•					
4107				•			
4108		•					
4109		•					
4110		•					
4201		•					
4202							•
4203		•					
4204	•						
4205	•						
4206		•					
4207			•				
4208			•				
4209		•					
4210		•					
4301		•					
4302		•					
4303		•					
4304			•				
4305		•					
	2	14	3	2	0	1	3
5101		•					
5102		•					
5103		•					
5104		•					
5105		•					
5106		•					
5107		•					
5108		•					
5109		•					
5110					•		
5111		•					
5201			•				
5202		•					
5203		•					
5204		•					
5205	•						
5206		•					
5207	•						
5208				•			
5209			•				
5210		•					
5211			•				
5212		•					
5213		•					
5214		•					
	2	18	3	1	1	0	0

IC	3920	3925	3931	4552	4553	4554
6101						•
6102					•	
6103						•
6104						•
6105						•
6106			•			
6107		•				
6108						•
6109			•			
6110						•
6111	•					
6112						•
6113			•			
6114						•
6201					•	
6202		•				
6203				•		
6204		•				
6205		•				
6206			•			
6207		•				
6208						•
6209			•			
6210		•				
6211						•
6212		•				
	1	7	5	1	2	10
7101		•				
7102		•				
7103		•				
7104			•			
7105			•			
7106		•				
7107	•					
7108		•				
7109		•				
7110	•					
7111		•				
7112	•					
7201	•					
7202	•					
7203			•			
7204	•					
7205			•			
7206	•					
7207			•			
7208			•			
7209			•			
7210		•				
7211	•					
7212		•				
7301			•			
	8	9	8	0	0	0

IC	3920	3925	3931	4552	4553	4554	4555	4556
8101		•						
8102					•			
8103		•						
8104		•						
8105		•						
8106		•						
8107		•						
8201							•	
8202							•	
8203		•						
8204						•		
8205			•					
8206		•						
8301						•		
8302		•						
8303						•		
8304		•						
8305		•						
	0	11	1	0	1	3	2	

Board	3920	3925	3931	4552	4553	4554	4555	4556
K	3	2	0	0	0	1		0
2	1	8	2	1	2	7		0
3	1	13	1	1	0	5		3
4	2	14	3	2	0	1		3
5	2	18	3	1	1	0		0
6	1	7	5	1	2	10		
7	8	9	8	0	0	0		
8	0	11	1	0	1	3	2	
Total	18	82	23	6	6	27	2	6
ICs	170							

Board	Transistors	Diodes
K	1	18
1	36	16
2		28
3		17
4		5
5	2	13
6	2	2
7		13
8	11	3
PS	4	7
Total	56	122

N1

C	
1	GND
2	A3
3	A2
4	A1
5	-
6	LM2
7	[ ]
8	LM1
9	-
10	-
11	-
12	-
13	-
14	-
15	-
16	-
17	LP
18	- [->]
19	- [->]
20	DW=0
21	D=8-11
22	DW=1

D	
1	D=12-15
2	D=4-7
3	D=1-3
4	-
5	DW=2
6	D=16
7	-
8	DW=3
9	-
10	8+9
11	6+7
12	5
13	4
14	ODD
15	EVEN
16	2+3
17	0+1
18	[nTD0]
19	LOF
20	LSB
21	V+5
22	GND

N2

A		C	
GND	1	1	GND
-	2	2	nPASUM
-	3	3	**PA**
-	4	4	nDL1
-	5	5	DL1
[->]	6	6	**nPA**
-	7	7	DL2
TP67	8	8	nDL2
DL<PA	9	9	nDL4
CPC	10	10	DL4
[ ]	11	11	DL8
-	12	12	nDL8
-	13	13	**TD16**
-	14	14	**nTD16**
-	15	15	**nTDB1**
nTDB8	16	16	**TDB1**
TDB8	17	17	**nTDB2**
[<-] -	18	18	**TDB2**
[<-] -	19	19	**nTDB4**
DW=0	20	20	**TDB4**
C02•S0	21	21	**D=8-11**
nCPW	22	22	**DW=1**

B		D	
-	1	1	**D=12-15**
nTD0	2	2	**D=4-7**
-	3	3	**D=1-3**
-	4	4	-
TD0	5	5	**DW=2**
D=16	6	6	-
DL=PA	7	7	**DW=3**
nTP67	8	8	**8+9**
TP0	9	9	**6+7**
-	10	10	**5**
KW4	11	11	-
KW3	12	12	**LDNML**
KW2	13	13	**4**
KW1	14	14	**ODD**
nG-SD	15	15	**EVEN**
LP	16	16	**2+3**
nBD0	17	17	**0+1**
BD0	18	18	**TB3**
TB0	19	19	**nTB3**
SD	20	20	CPA
V+5	21	21	V+5
GND	22	22	GND

N3

A		C	
GND	1	1	[GND]
BD0	2	2	nK(A+S)
nPB1	3	3	**PB1**
PB2	4	4	K(N+P+RM)
nKSQRT	5	5	**nFST**
KSH	6	6	KP
n@7103-11	7	7	**nFG**
nPB=0	8	8	**FG**
nFRS	9	9	**nFN**
FN	10	10	nENDP
nFRT	11	11	nENDLP
FRT	12	12	nENDSP
CC00	13	13	n@7208-6
SD	14	14	WT
nFOVF	15	15	**LOF**
PM1	16	16	TDB1
nTDB1	17	17	nPM1
nTDB2	18	18	TDB2
CC14	19	19	TDB4
CC15	20	20	nTDB4
RSUM	21	21	nTDB8
nKRV	22	22	TDB8

B		D	
FMLT	1	1	**PB=TD**
CC17	2	2	**LP**
nFMLT	3	3	[nKSH]
FDIV	4	4	SCT2
nTD16	5	5	KK
FME	6	6	SCT4
nFME	7	7	nSCT4
KMS	8	8	nFC0
nKM2SUB	9	9	nKM2ADD
FU	10	10	n(KOP•FU)
nF(M+D+R)	11	11	TD16
F(M+D+R)	12	12	LDNML
F(M+D)	13	13	nKST
F(D+R)	14	14	FJ2
K(M+D)	15	15	nKDIV
CPC	16	16	nKMLT
nKC	17	17	TB3
nKADD	18	18	**nF(MQ+DQ)**
nKSUB	19	19	nK(C+CI)
CPA	20	20	nKCM1
V+5	21	21	nKCM2
GND	22	22	[V+5]

N4

A		C	
GND	1	1	GND
nPA	2	2	**nG-PY1**
nPB1	3	3	PB1
PB2	4	4	K(N+P+RM)
[KSH]	5	5	[nFST]
KRM1	6	6	**nKRVC2S0**
nKRM1	7	7	nFG
FRS	8	8	FG
nFRS	9	9	nFN
KRM2	10	10	[nENDP]
nKRM2	11	11	[nENDLP]
FRT	12	12	nTB3
TD0	13	13	PA
CCX1	14	14	CCX3
CC02	15	15	K(N+P)
PM1	16	16	nCC00
CC12	17	17	**nPM1**
[CC13]	18	18	**n(enBtoA)**
CC14	19	19	**nTD0+TB3**
CC15	20	20	**enSBtoSA**
C02•S0	21	21	CC16
nKRV	22	22	C13•S0

B		D	
FMLT	1	1	C17•S0
nTD0	2	2	SCT0
FF	3	3	SCT1
FDIV	4	4	SCT2
TD0	5	5	SCT3
[FME]	6	6	SCT4
[nFME]	7	7	[nSCT4]
-	8	8	eBD0toWB
TP0	9	9	**G-PY**
C12•S0	10	10	**nG-PX**
nF(M+D+R)	11	11	TD16
-	12	12	FJ1
F(M+D)	13	13	DL=PA
F(D+R)	14	14	FJ2
S-PCA	15	15	nFJ2
CPC	16	16	**FC0**
DL<PA	17	17	**nFC0**
enSAtoSB	18	18	nF(MQ+DQ)
-	19	19	nK(C+CI)
[CPA]	20	20	nKCM1
V+5	21	21	nKCM2
GND	22	22	V+5

N5

A		C	
GND	1	1	GND
BD0	2	2	**nPASUM**
nG-SD	3	3	**LM1**
LV	4	4	**LM2**
K(N+P)	5	5	nFST
KSH	6	6	KP
-	7	7	nSUM<0
nPB=0	8	8	**nSK**
-	9	9	**SK**
FN	10	10	nENDP
nFRT	11	11	nENDLP
FRT	12	12	nKN
CC00	13	13	CC17
CCX1	14	14	[CCX3]
[CC02]	15	15	CC121415
CC10	16	16	nCC00
CC12	17	17	nCCX3
-	18	18	CC151617
nACA	19	19	nCC14
enSBtoSA	20	20	CC10-17
C02•S0	21	21	CC16
-	22	22	AD0

B		D	
FMLT	1	1	nTD16
nTD0	2	2	SCT0
FF	3	3	[SCT1]
-	4	4	SCT2
TD0	5	5	SCT3
FME	6	6	SCT4
nFME	7	7	nSCT4
[nTP67]	8	8	**LSB**
nKM2SUB	9	9	G-PY
FU	10	10	nG-PX
nF(M+D+R)	11	11	TD16
F(M+D+R)	12	12	**FJ1**
F(M+D)	13	13	KRM1
-	14	14	**FJ2**
S-PCA	15	15	**nFJ2**
CPC	16	16	KRM2
[->]	17	17	nFC0
enSAtoSB	18	18	-
nKSUB	19	19	nK(C+CI)
CPA	20	20	nKCM1
V+5	21	21	nKCM2
GND	22	22	V+5

N6

A		C	
GND	1	1	GND
-	2	2	-
-	3	3	SUBB
-	4	4	SUBA
nKSQRT	5	5	**AINC**
-	6	6	ACA
-	7	7	**C12•S0**
-	8	8	nCA
-	9	9	**nCAIN**
n(KOP•FU)	10	10	**nENDP**
[nFRT]	11	11	**nENDLP**
-	12	12	**nENDSP**
CC00	13	13	**CC17**
CCX1	14	14	**CCX3**
CC02	15	15	**CC121415**
CC10	16	16	**nCC00**
CC12	17	17	**nCCX3**
CC13	18	18	**CC151617**
CC14	19	19	**nCC14**
CC15	20	20	**CC10-17**
C02•S0	21	21	**CC16**
C02•S4	22	22	**C13•S0**

B		D	
[FMLT]	1	1	**C17•S0**
[nTD0]	2	2	**SCT0**
nFMLT	3	3	**SCT1**
-	4	4	**SCT2**
-	5	5	**SCT3**
FME	6	6	**SCT4**
nFME	7	7	**nSCT4**
nTP67	8	8	**SCT01**
TP0	9	9	**SCT12**
FU	10	10	**SCT34**
[nF(M+D+R)]	11	11	TD16
F(M+D+R)	12	12	FJ1
F(M+D)	13	13	-
nKMN	14	14	FJ2
K(M+D)	15	15	nFJ2
nKA	16	16	[FC0]
nKC	17	17	nFC0
nKADD	18	18	-
nKSUB	19	19	-
[CPA]	20	20	[CPA]
V+5	21	21	-
GND	22	22	V+5

N7

A		C	
GND	1	1	GND
nG-PY1	2	2	BD0
nPB1	3	3	**SUBB**
nTD0+TB3	4	4	**SUBA**
nG-X	5	5	**G-Y**
KSH	6	6	AD
nSUM<0	7	7	nFG
FRS	8	8	BD
nFRS	9	9	nSK
SD	10	10	SK
nFRT	11	11	KA
FRT	12	12	nFOVF
[nTD16]	13	13	CC17
CCX1	14	14	CCX3
CC02	15	15	nACA
CC10	16	16	K(N+P)
CC12	17	17	n(enBtoA)
CC13	18	18	**n@7208-6**
CC14	19	19	nKRVC2S0
CC15	20	20	**nWA**
C02•S0	21	21	CC16
C02•S4	22	22	C12•S0

B		D	
FMLT	1	1	C17•S0
nTD0	2	2	SCT0
nFMLT	3	3	SCT1
FDIV	4	4	SCT2
nWB	5	5	SCT3
FME	6	6	SCT4
nBD0	7	7	nAD0
AD0	8	8	SCT01
nG-BD	9	9	SCT12
K54	10	10	SCT34
nF(M+D+R)	11	11	TD16
F(M+D+R)	12	12	FJ1
F(M+D)	13	13	KRM1
F(D+R)	14	14	FJ2
PB=TD	15	15	nFJ2
KRM2	16	16	CC151617
TB0	17	17	**n@7103-1**
nKMN	18	18	nF(MQ+DQ)
[nKCM1]	19	19	nK(C+CI)
eBD0toWB	20	20	nKCM1
V+5	21	21	nKCM2
GND	22	22	V+5

N8

A		C	
GND	1	1	GND
CPA	2	2	**BD**
RSUM	3	3	TB3
G-Y	4	4	nG-X
[<-]	5	5	AINC
ACA	6	6	**AD**
-	7	7	**{nAD1}**
-	8	8	**{AD1}**
-	9	9	-
-	10	10	-
-	11	11	-
-	12	12	-
-	13	13	-
-	14	14	-
-	15	15	-
-	16	16	-
-	17	17	**nACA**
-	18	18	nCAIN
-	19	19	**{CA}**
-	20	20	**nCA**
-	21	21	**{nAOK}**
-	22	22	**{AOK}**

B		D	
nWB	1	1	nWA
nCPW	2	2	**nBD0**
{CPW}	3	3	**BD0**
-	4	4	**nAD0**
-	5	5	**AD0**
-	6	6	nG-BD
-	7	7	-
-	8	8	-
-	9	9	-
-	10	10	-
-	11	11	-
-	12	12	-
-	13	13	-
-	14	14	-
-	15	15	-
-	16	16	-
-	17	17	-
-	18	18	-
V–5	19	19	-
-	20	20	-
V+5	21	21	[V+5]
GND	22	22	GND

Canon 163 Calculator

Section: Connectors
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- As viewed from bottom of backplane.
- Bold-faced expressions are signal sources.
- {signal} : connected on the PCB but not connected on the backplane.
- [signal] : connected on the backplane but not connected on the PCB.