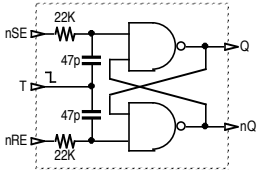
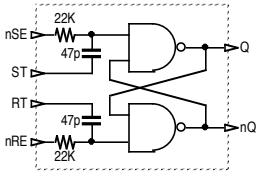
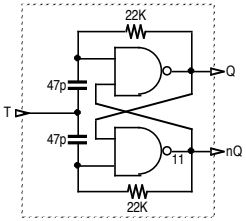
Flip-Flops & Variations



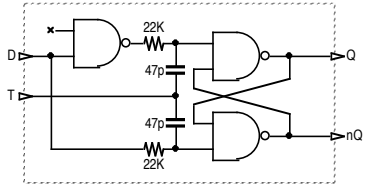
Basic Flip-Flop
- Q goes 1 if nSE=0 at –edge of T
- Q goes 0 if nRE=0 at –edge of T
- No change if nSE=1 & nRE=1 at trigger
- Undefined if nSE=0 & nRE=0 at trigger



Separated Triggers
- Q goes 1 if nSE=0 at –edge of ST
- Q goes 0 if nRE=0 at –edge of RT

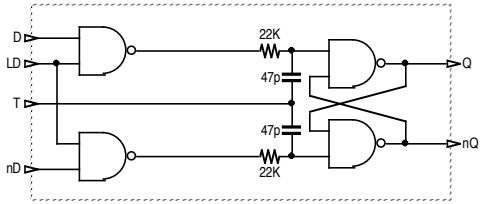


Toggle Flip-flop
- Q inverts on –edge of T



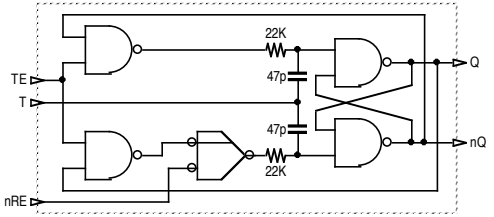
D Flip-Flop

- Q follows D at –edge of T



Gated Load

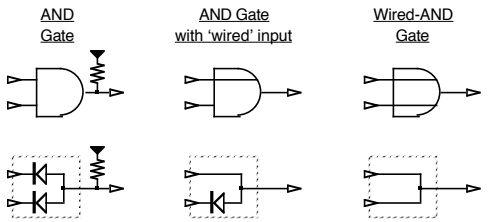
- Q follows D if LD=1 at –edge of T
- No change at trigger if LD=0



Gated Toggle

And with Synchronous Reset.
Variation on Gated-Load:
Q follows nQ if TE=1 at –edge of T

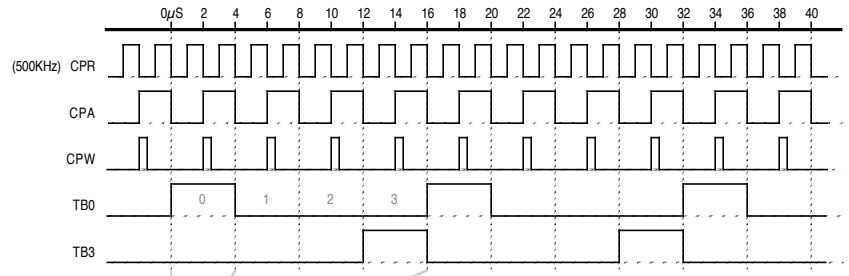
- Q toggles if TE=1 at –edge of T
- Q goes 0 if nRE=0 at –edge of T



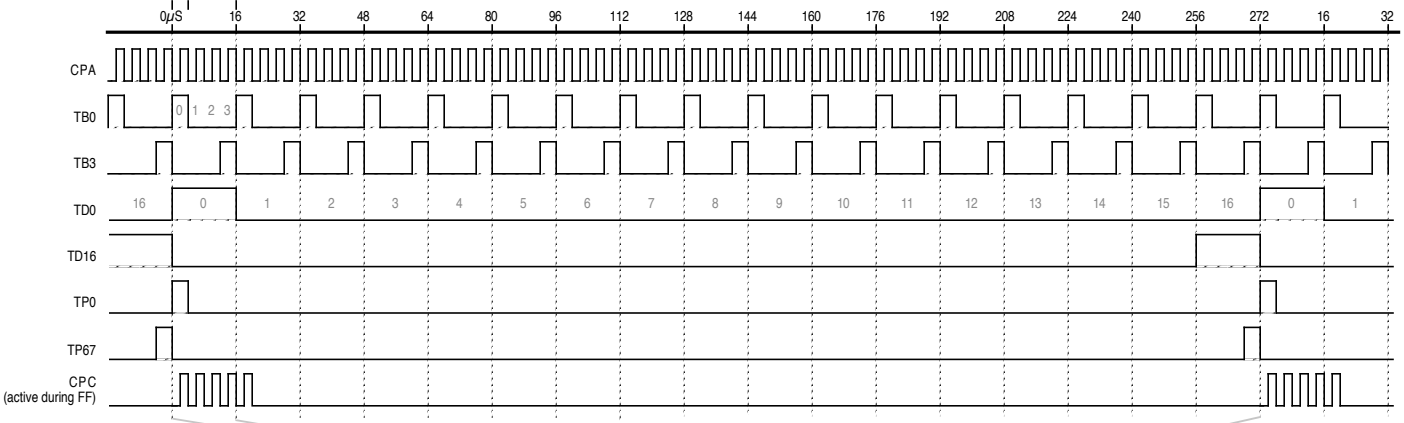
Discrete Gate Construction

A few gates are constructed from discrete diodes and resistors. A wire–AND construction is indicated by the input line traversing the width of the gate.

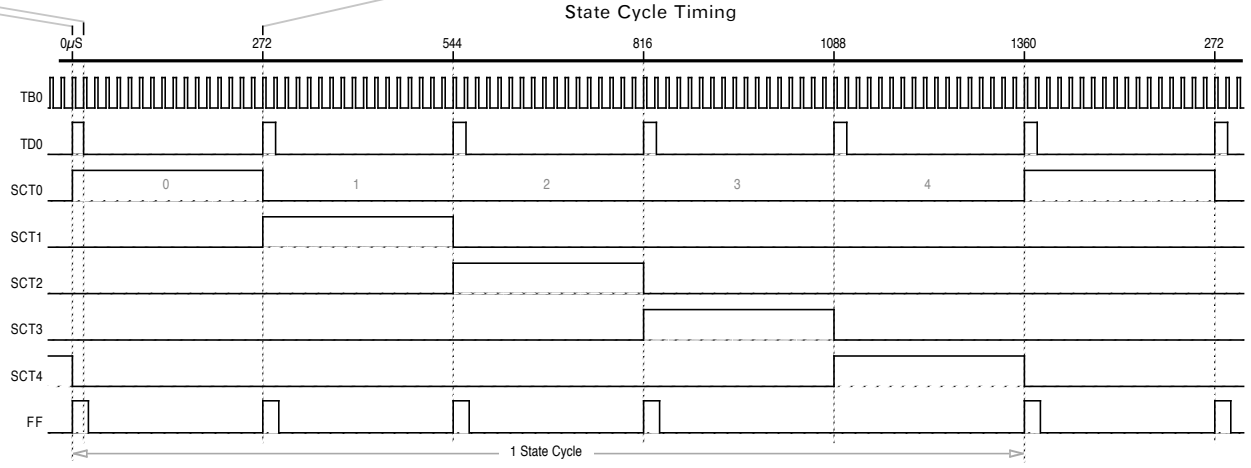
Bit & Digit Timing



Digit & Number Timing



State Cycle Timing



• CPW measured as 0.5 μS.

Figure M1
Register-Level Functional Model

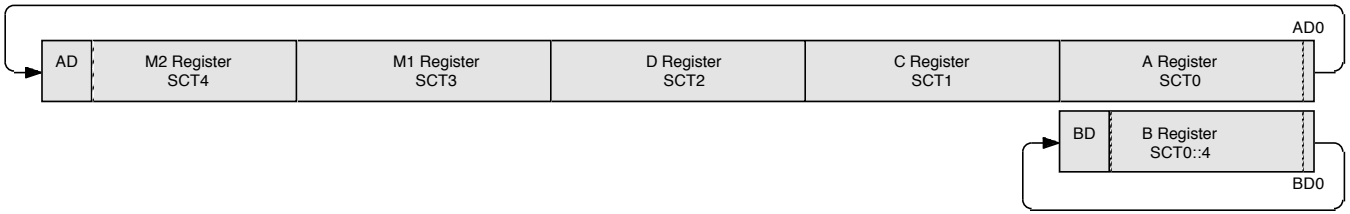


Figure M2
Delay-Line Storage Organisation
with Idle-State Bit Paths at Time TB0 of TD0 of SCT0

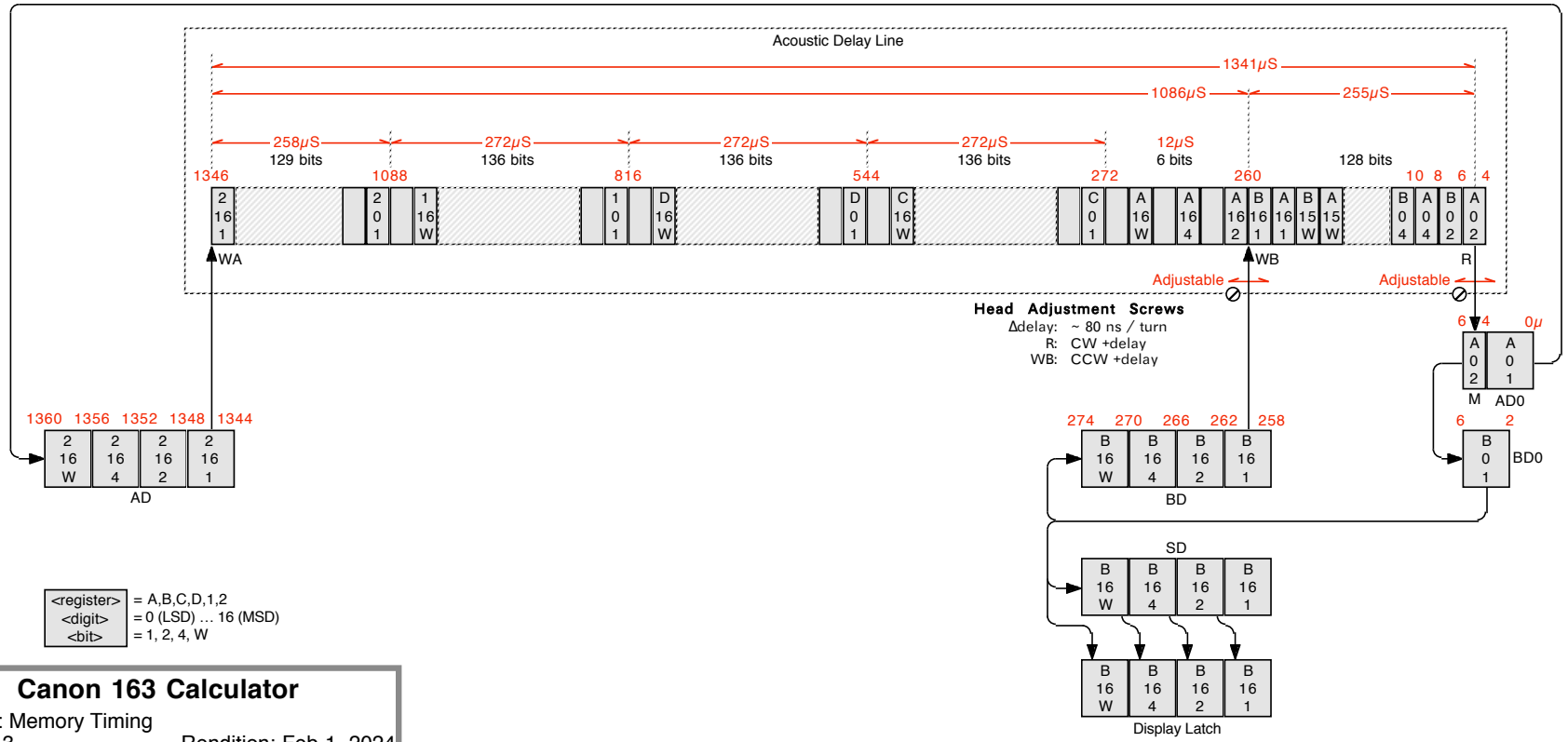


Figure M3
Acoustic Delay Line Timing

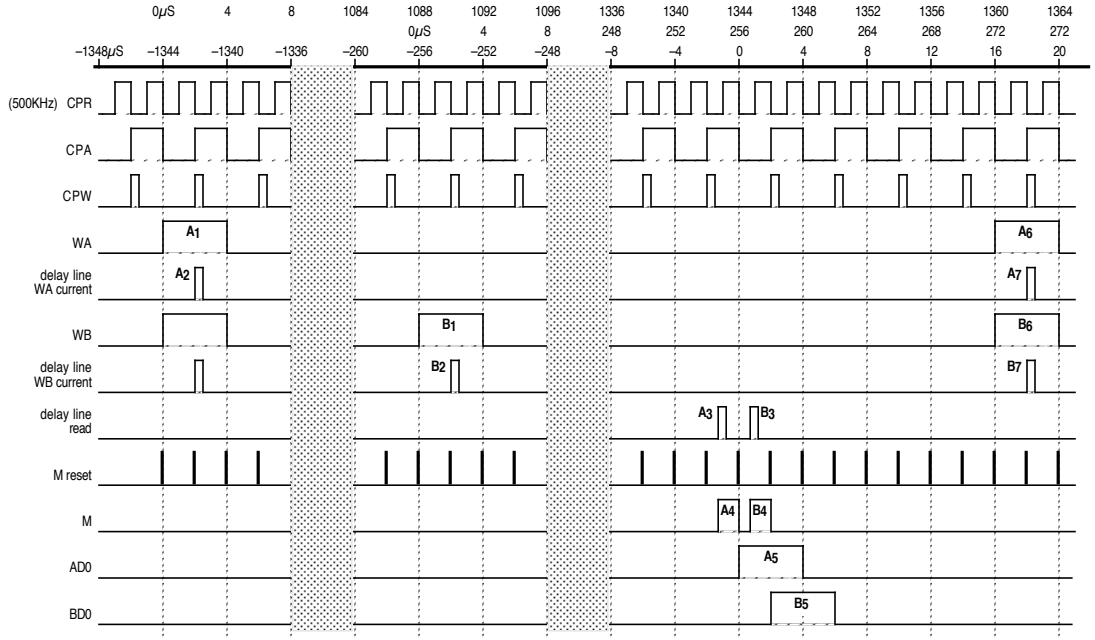


Figure M4
Delay Line Read Timing

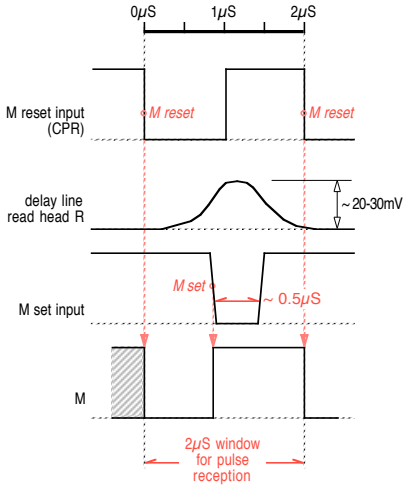
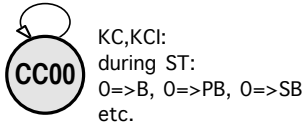


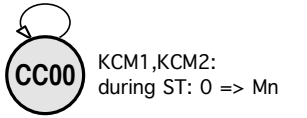
Figure M5
Decimal Encoding

Value	W421
0	0000
1	0001
2	0010
3	0011
4	0100
-	0101
-	0110
-	0111
-	1000
-	1001
-	1010
5	1011
6	1100
7	1101
8	1110
9	1111

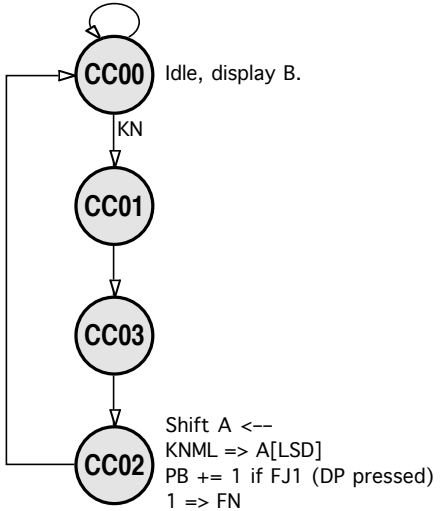
Clear



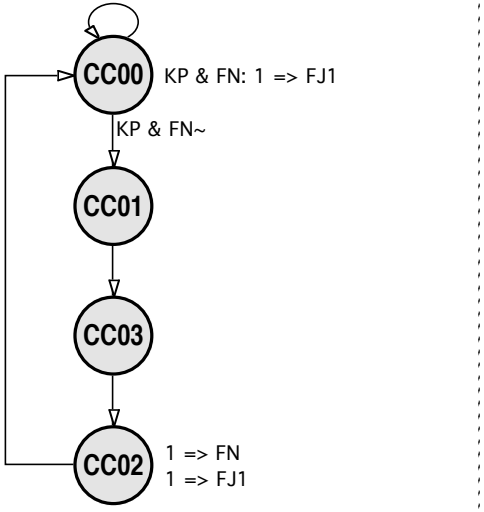
Clear Memory



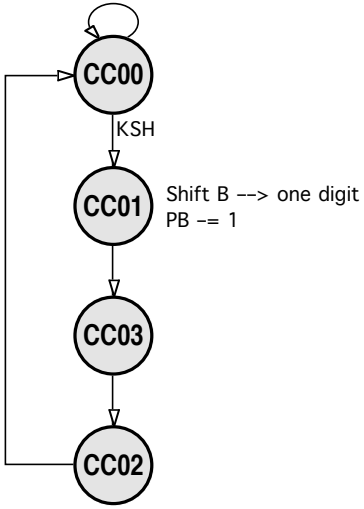
Numeral Entry



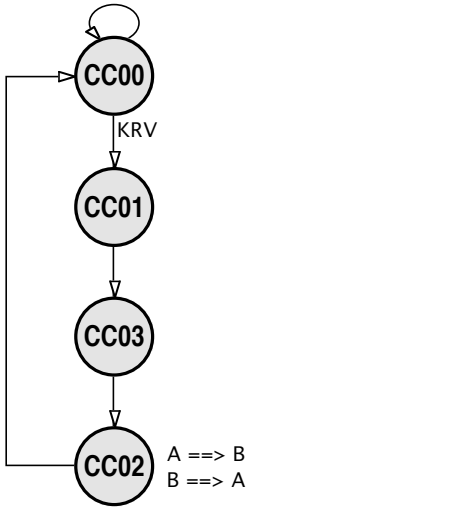
DP Entry



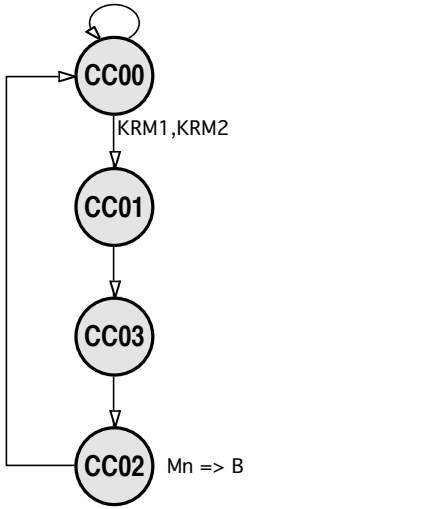
Undo Entry



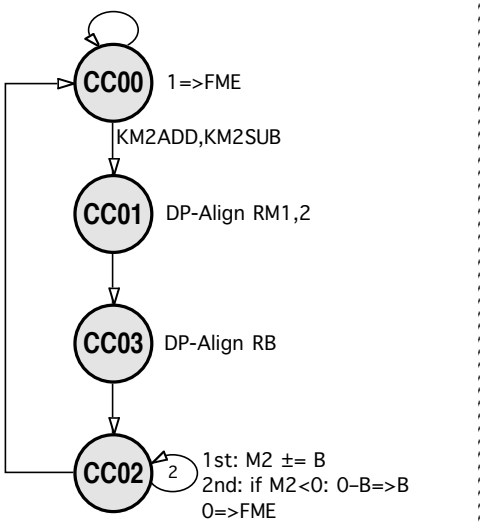
Reverse



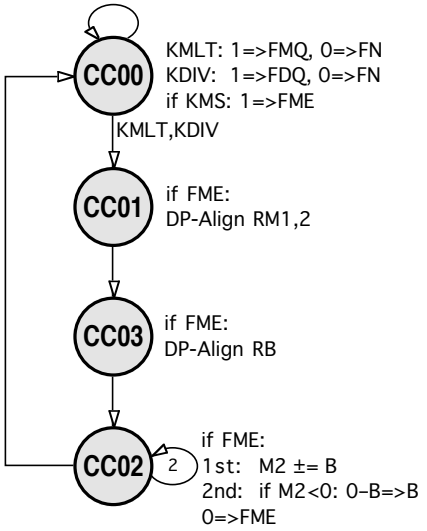
Recall Memory



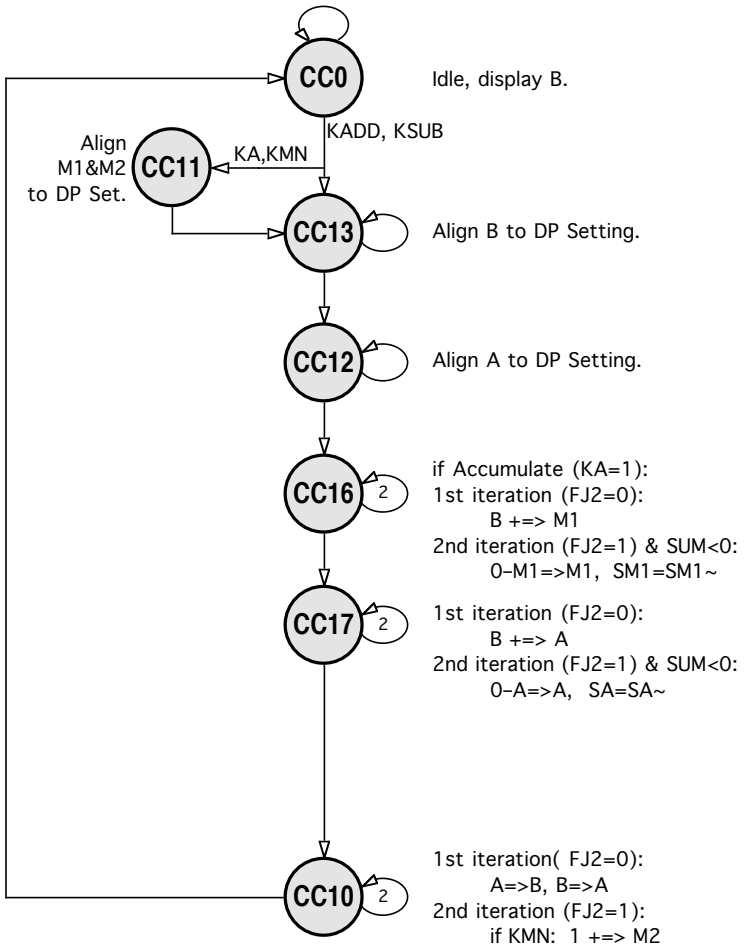
M2 Add/Subtract



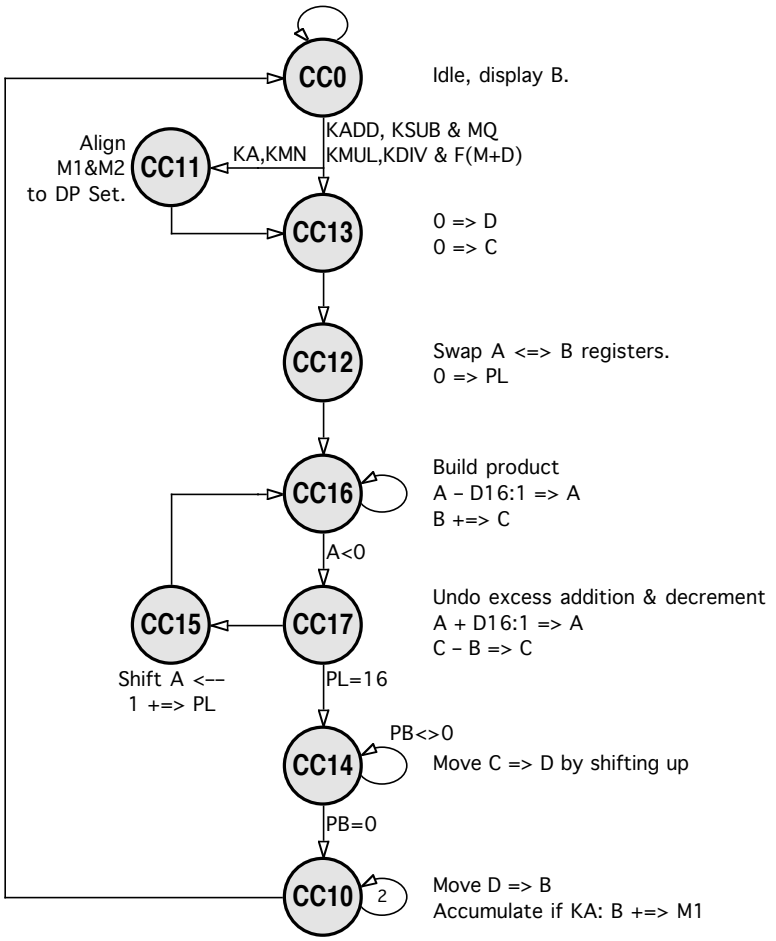
Queue Multiply / Divide



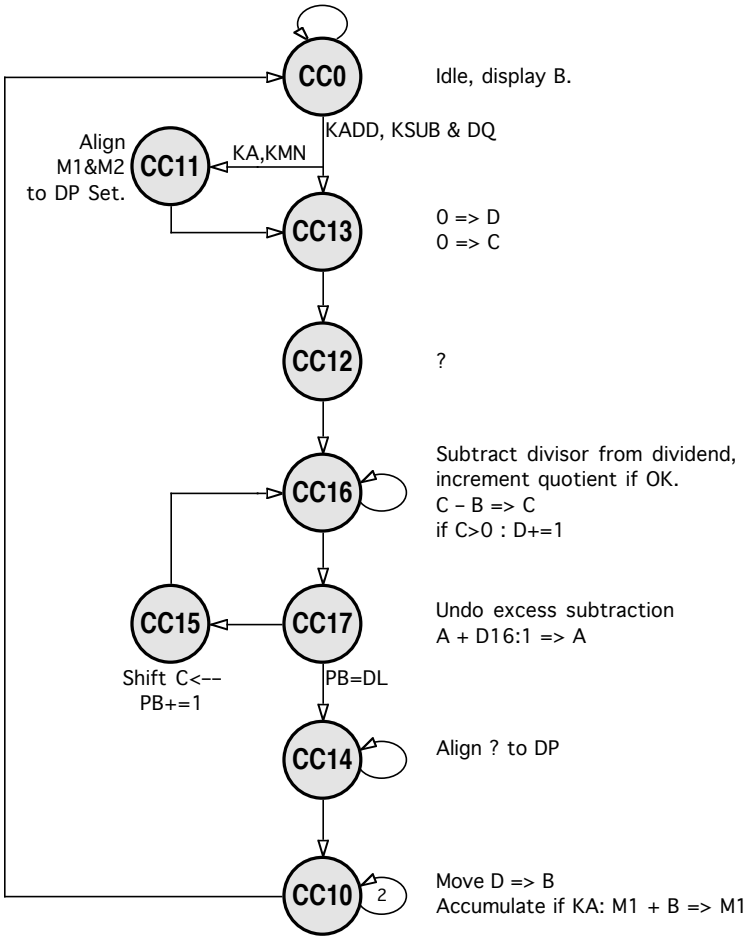
Add / Subtract



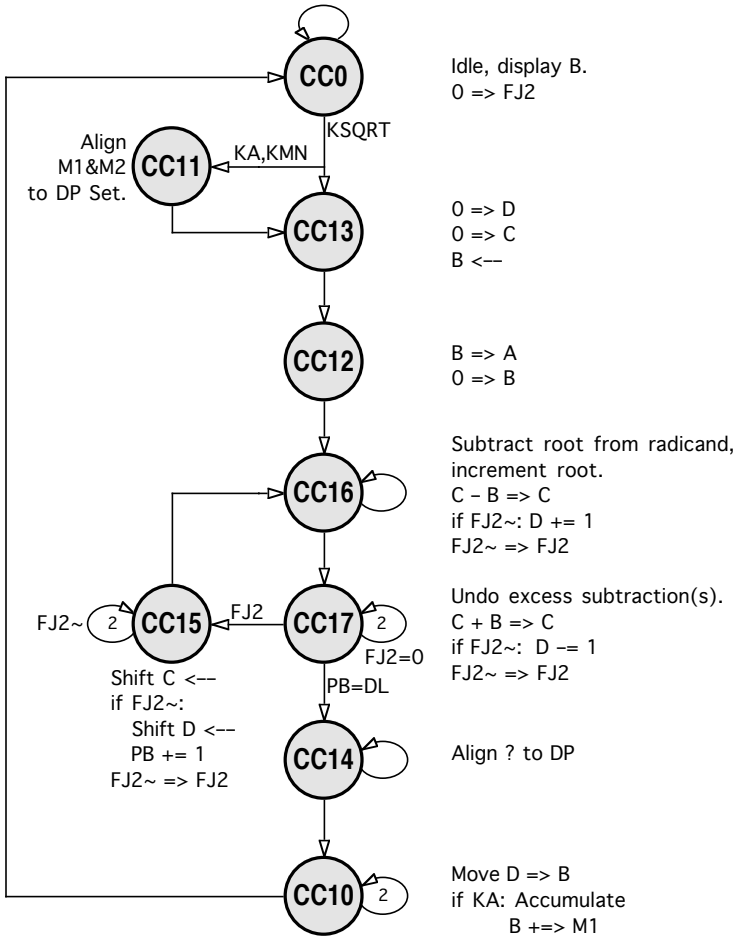
Multiply



Divide

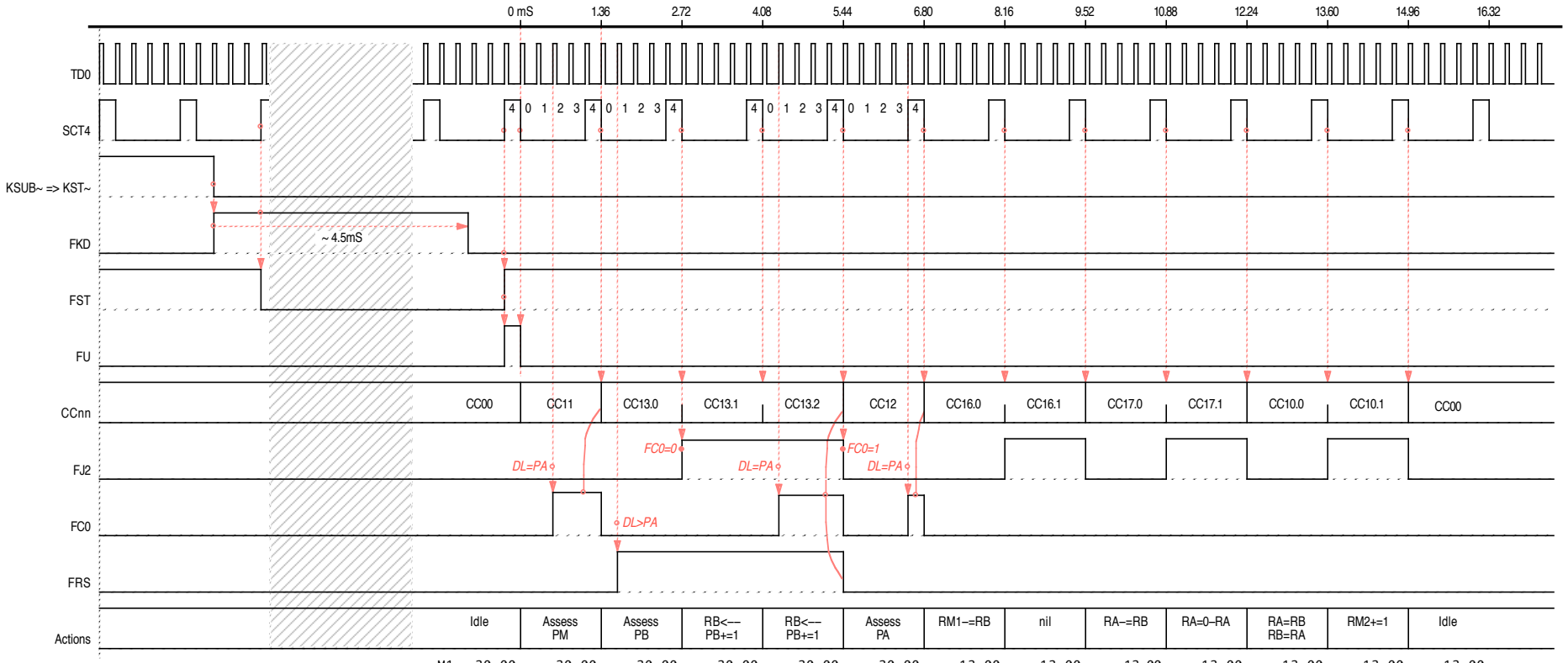


Square Root



Example Procedure Execution – Subtraction

- DP switch = 2
- M2 mode switch = Count
- Accumulate to M1 = ON
- Current Total (RM1) = 20.00
- Last Result (RA) = 5.00
- New number entered (RB) = 8
- Press –= KEY (subtract)



Register contents after end of state cycle:

M1=	20.00	20.00	20.00	20.00	20.00	20.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
A=	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	99997.00	3.00	8.00	8.00	8.00
B=	8	8	8	8.0	8.00	8.00	8.00	8.00	–8.00	–8.00	–3.00	–3.00	–3.00

Square Root Procedure Sample
√2

Radicand		Root	State	FJ2
2	-	0	16	0
2	-	1	16	1
1	-	1	16	0
0	-	2	16	1
-2	+	2	17	0
0	+	1	17	1
1		1	15	0
10		10	15	1
100	-	10	16	0
90	-	11	16	1
79	-	11	16	0
68	-	12	16	1
56	-	12	16	0
44	-	13	16	1
31	-	13	16	0
18	-	14	16	1
4	-	14	16	0
-10	+	14	17	1
4		14	15	0
40		140	15	1
400	-	140	16	0
260	-	141	16	1
119	-	141	16	0
-22	+	141	17	1
119		141	15	0
1190		1410	15	1
11900	-	1410	16	0
10490	-	1411	16	1
9079	-	1411	16	0
7668	-	1412	16	1
6256	-	1412	16	0
4844	-	1413	16	1
3431	-	1413	16	0
2018	-	1414	16	1
604	-	1414	16	0
-810	+	1414	17	1
604				0