Canon EP151 Calculator

Contents

Notes

- A lowercase “n” in a symbol name indicates the logical NOT operation.
- The symol N*bcpp* denotes a physical connector pin, where *b*=board (1 to 7), *c*=connector, (A or B), and *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector. Board 8 is the backplane. See “Connectors” page.
- Connection points labeled “NM*pps*” refer to the row of points on the main/backplane board between the PCB connectors and the ICs. *s*=stagger (C,K or M) depending on whether the pin is staggered towards the connectors, the keyboard, or in the middle.
- The symbol ▼ without an explicit voltage specification denotes V+5.
- Capacitance in microfarads unless otherwise indicated.
- These drawings based on unit with Serial No.: 200464

Log

- 2002 Apr-May: Initial drawing / bhilpert.
- 2021 Feb: TMS3314 shift register pinout obtained, register organisation resolved.
  Conversion to single pdf, format upates.
  Connector pin labeling redone from alpha to ABCD.
  Block, Timing, State diagrams added.
  Some gates changed to negative-logic presentation.

Signal Names

Most signal names are obtained from labels on the printed circuit boards. Some labels used here were created during the reverse engineering process.

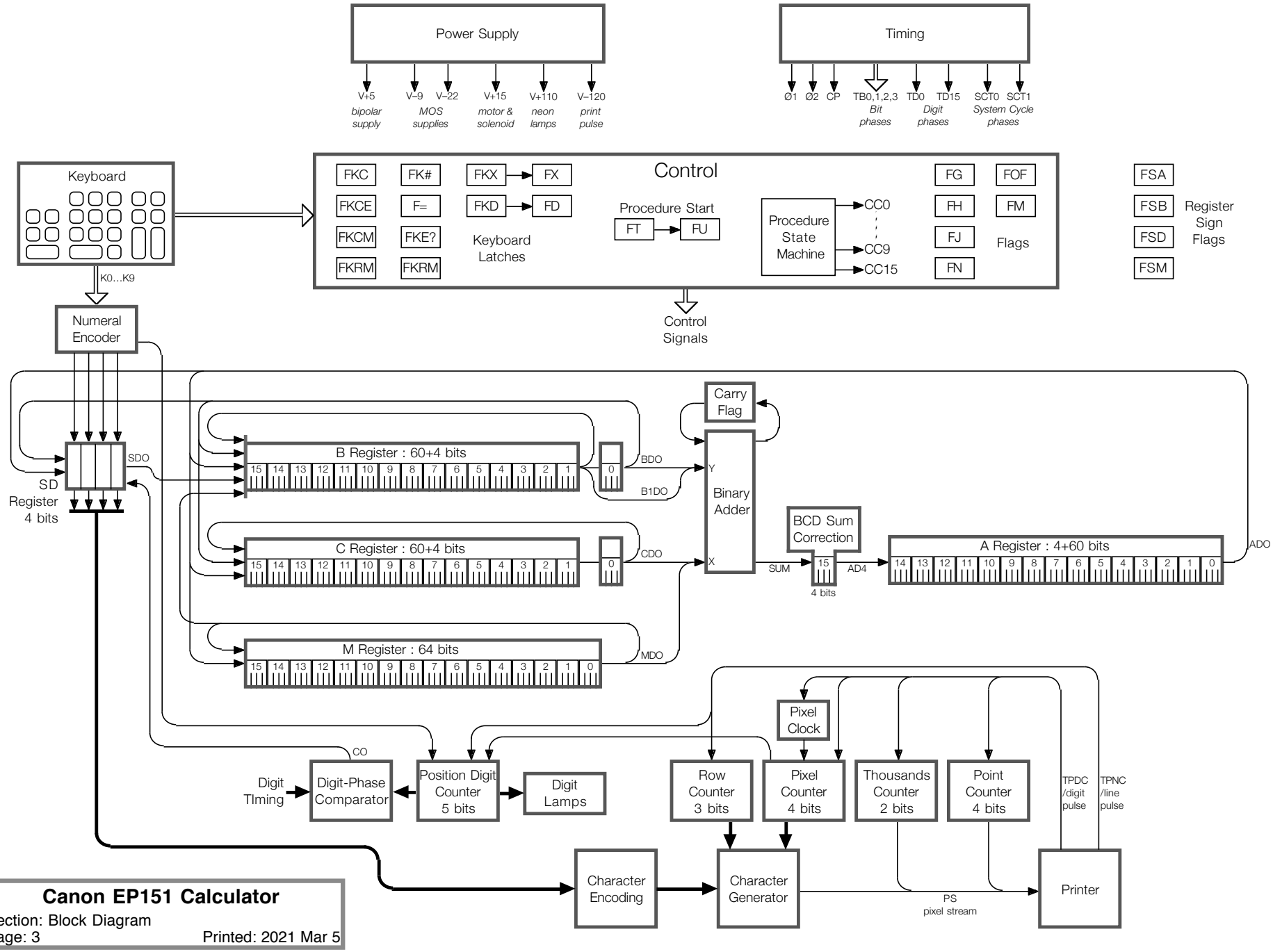
Section	Signal	Description
Timing	Ø1	Clock for MOS memory.
	Ø2	Clock for MOS memory.
	CP	Clock Pulse. +5V version of Ø?. This is the basic bit clock.
	TB0…TB3	Time Bit. Pulses for specified bit.
	TD0…TD15	Time Digit. Pulses for specified digit.
	SCT0,SCT1	State Cycle Time. Two phases of a state cycle.
Keyboard	K…	The keyboard and numeral encoder.
	FK…	Latched versions of the keyboard signals.
	FU	Function keypress sychronized to the state cycle.
Control	CC0…CC15	The 11 states of the state machine.
	F…	Assorted 1-bit Flag registers.
	FOF	Overflow latch.
Memory	ADO	A Register Data Output (bit stream).
	BDO	B Register Data Output.
	CDO	C Register Data Output.
	MDO	M Register Data Output.
Arithmetic	AD4	Bit stream from arithmetic to the memory.
	CA	Carry.
PC Counter	PC=0	1 when the decimal Point Counter is 0.
	PC=DL	1 when the decimal Point Counter coincides with the Decimal Limit (switch setting).
PD Counter	PD…	Position Digit Counter. Used for two purposes: - To count digits during number entry, indicated via neon lamps. - During the print cycle to track and time the loading of the SD register with the appropriate digit data to print.
	CO	Comparator Output, indicates match of PD Counter with digit phase.
Character Encoding		
	CHRx	Six bit Character code to address character ROM.
Character Generator		
	PS	Pixel Stream to printer.

• The label for Fmlt+Fdiv by U4202 is actually the inversion.
• The label for Fmlt+Fdiv by U4207 is incorrect, this is nFOF.

• Renamed symbols:

nK÷	nKD
FK÷	FKD
FX+F÷	FK(X+D)
Fmlt	FX
Fdiv	FD
Fmlt+Fdiv	F(X+D)

• Created symbols, not found on PCBs:
CPp
KN1, KN2, KN4, KN8, KNUM, KNP, KCEM#, KASXD
FKENT, FKC, FKCE, FKCM, FKRM, FK#, FOF, FKaa, n(FM+FD•nKK), nFXDR, nBADENT
F=RE
FCC1SE, FCC2SE, nCSaa, CLRB, nCScc
B1DO, MDO, SDIN, SD=0, DR**, X–Y, SUM, CA10
PC3ENB, PCENB
Maa, Mbb, CHR*, ØP, PXENB, PXC=6, PXTa, PXTb



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Section: Block Diagram

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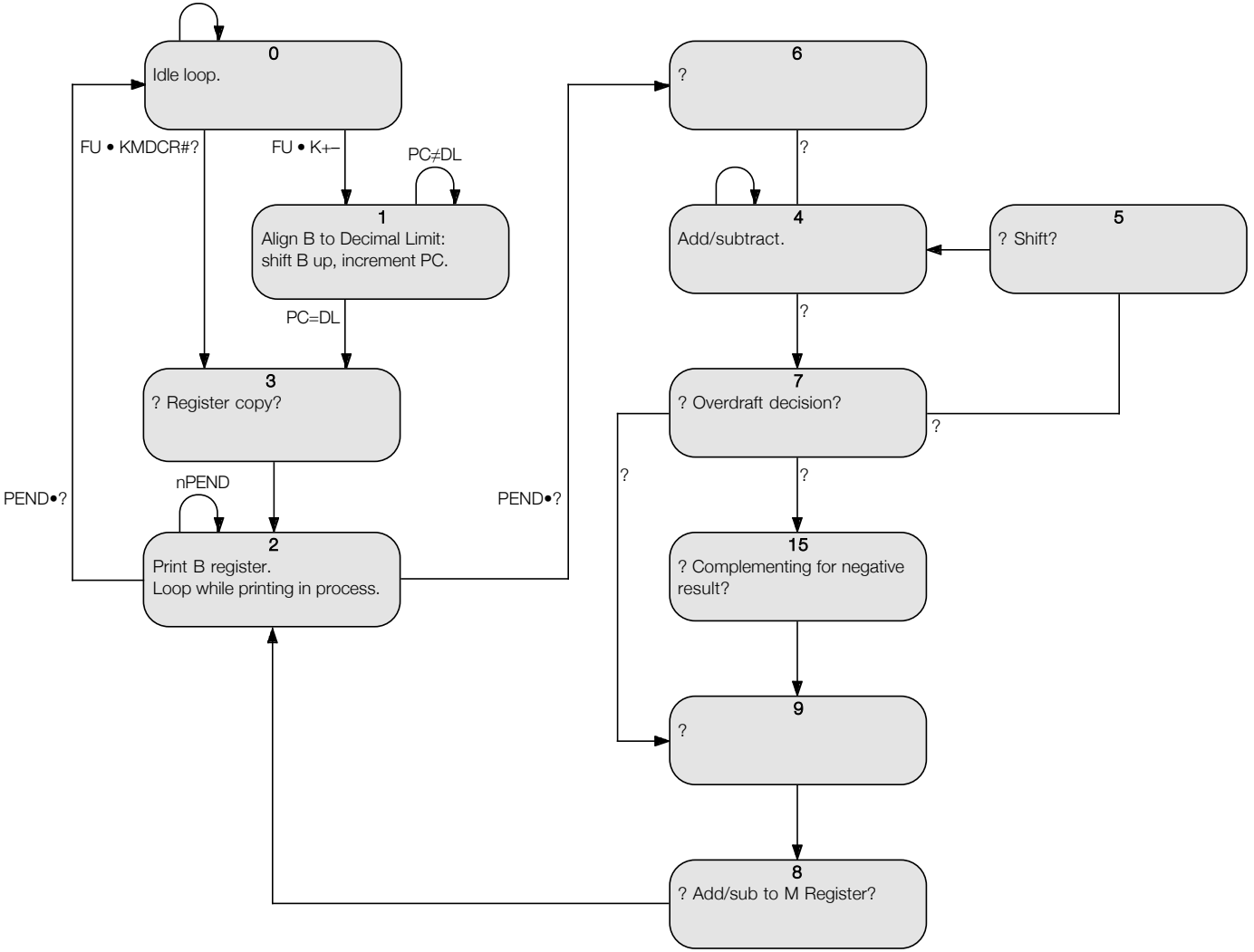
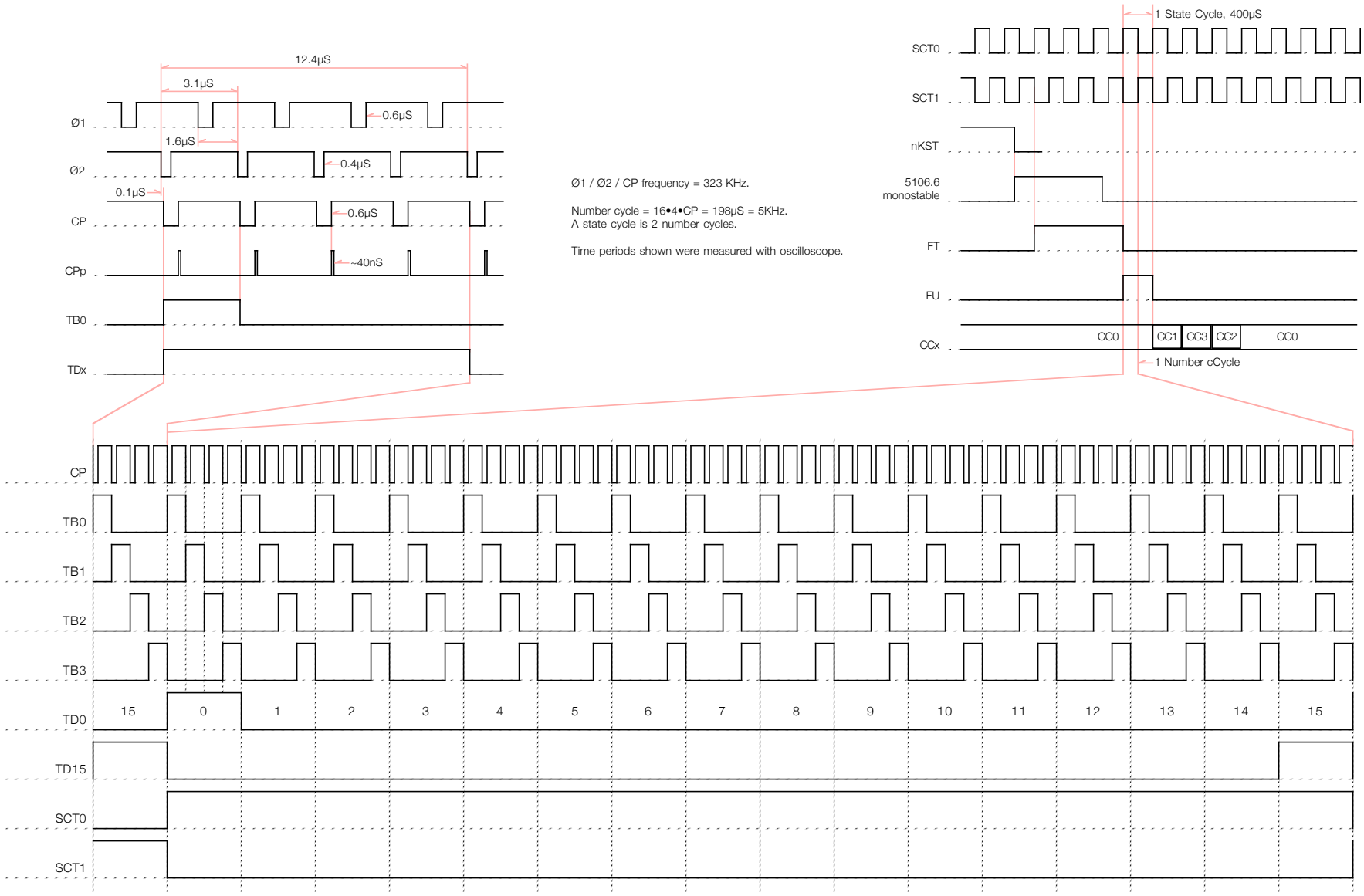
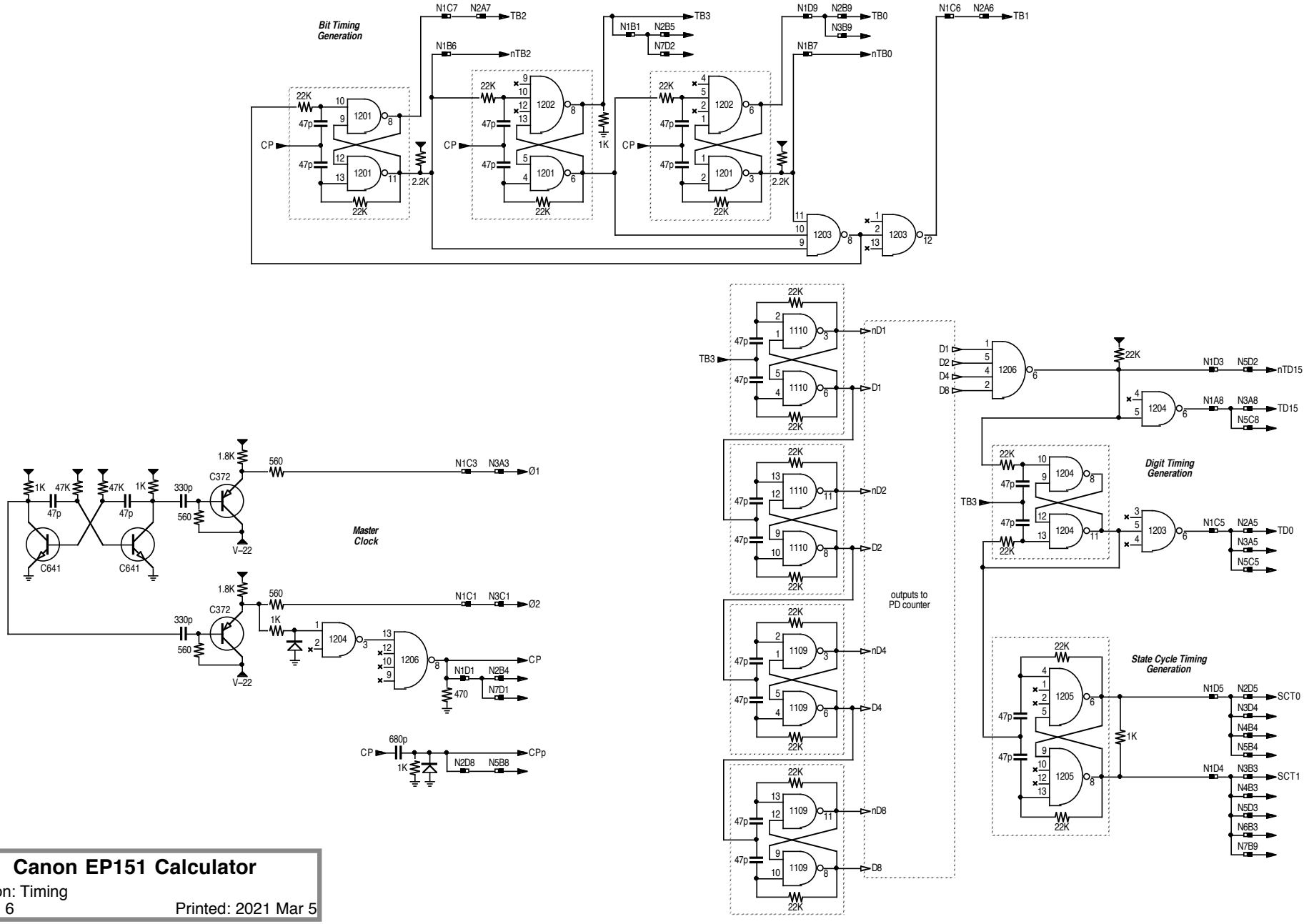


3.0 default
3.1 if RM, M –> B


12.4µS
3.1µS
Ø1
0.6µS
1.6µS
Ø2
0.4µS
0.1µS
CP
0.6µS
CPp
~40nS
TB0
TDx
Ø1 / Ø2 / CP frequency = 323 KHz.
Number cycle = 16•4•CP = 198µS = 5KHz.
A state cycle is 2 number cycles.
Time periods shown were measured with oscilloscope.
1 State Cycle, 400µS
SCT0
SCT1
nKST
5106.6
monostable
FT
FU
CCx
CC0
CC1
CC3
CC2
CC0
1 Number cCycle
CP
TB0
TB1
TB2
TB3
TD0
15
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
TD15
SCT0
SCT1



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Section: Timing

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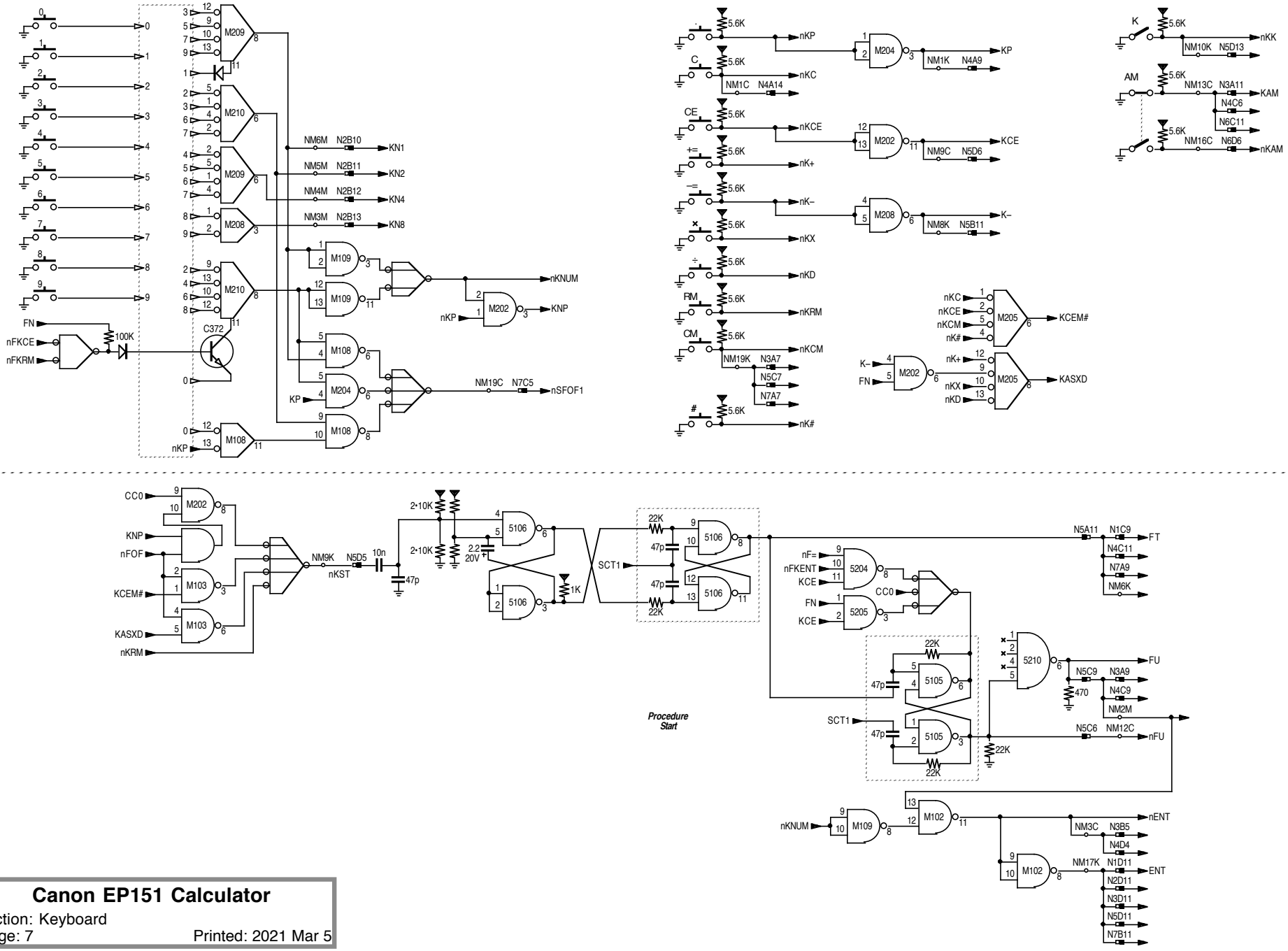

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Section: Keyboard

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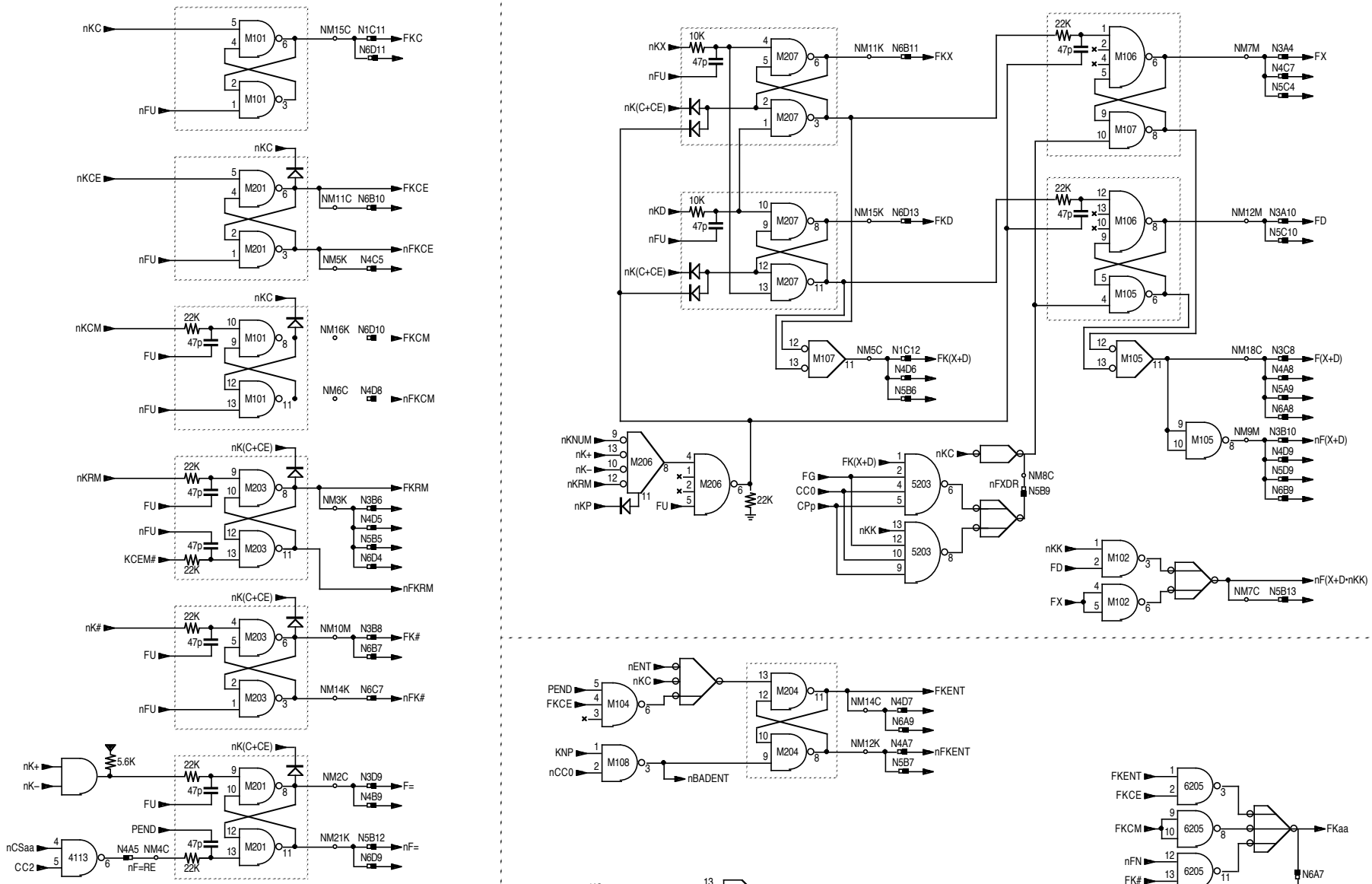

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Section: Keyboard Latches

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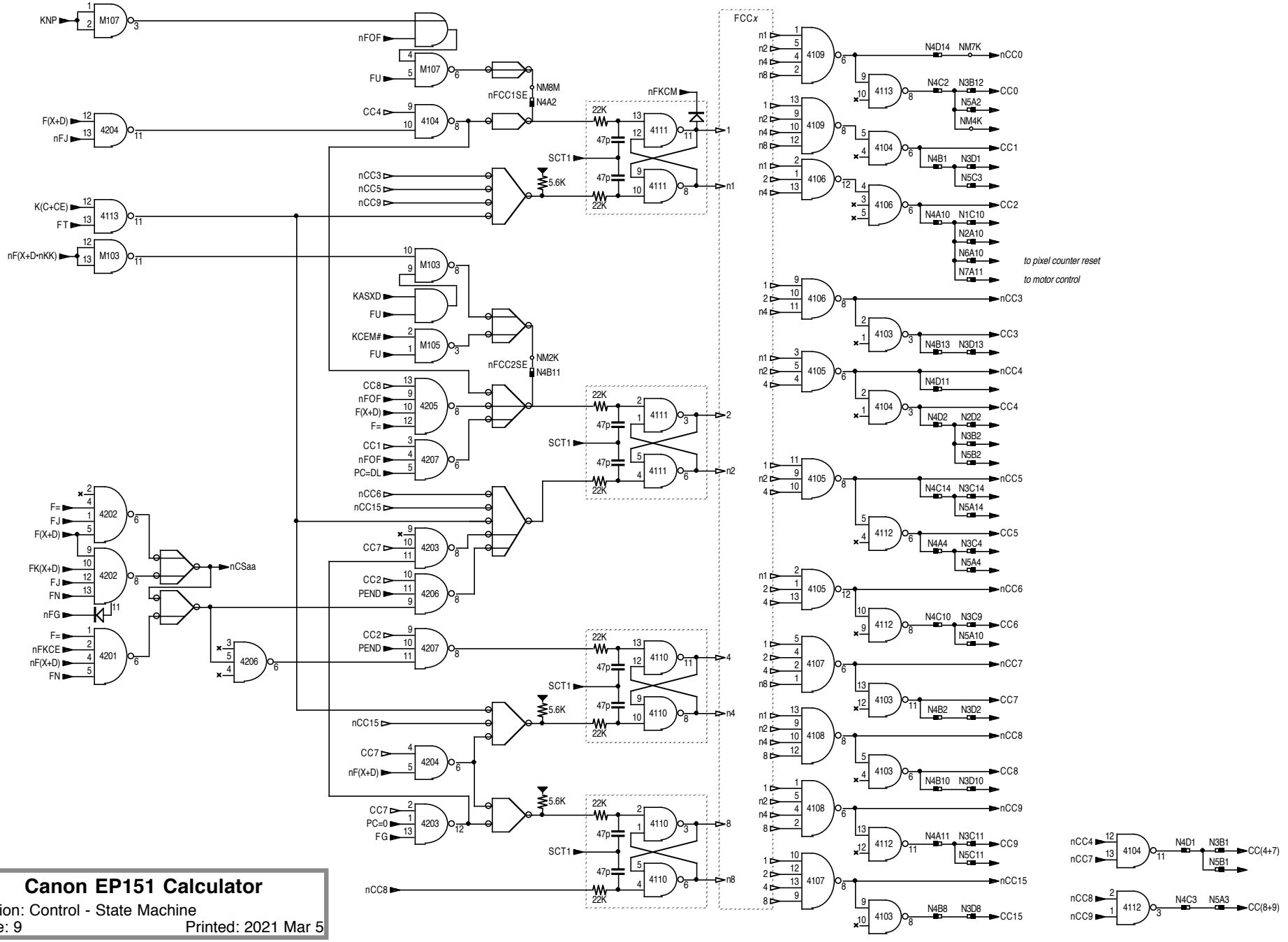

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Section: Control - State Machine

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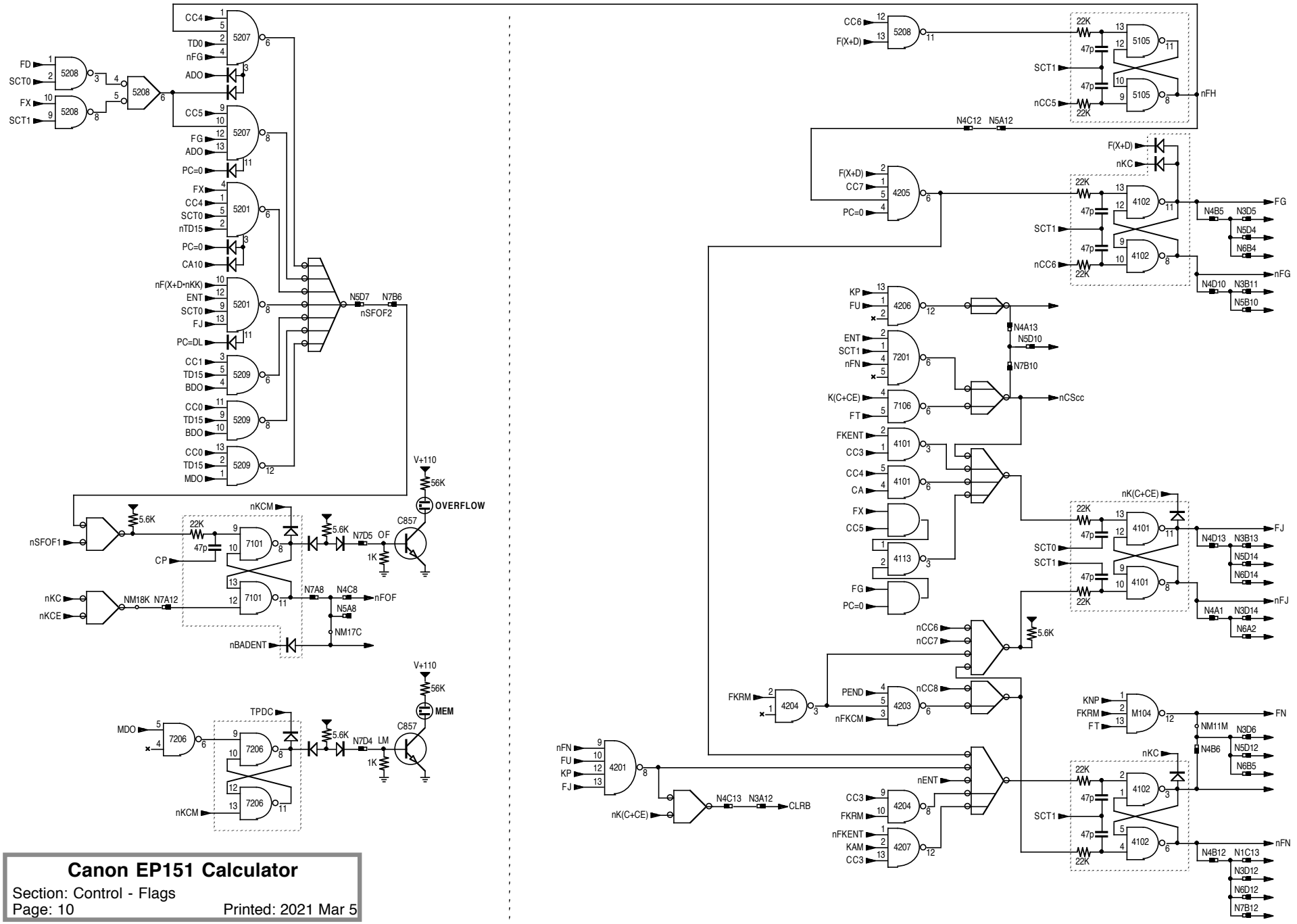

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Section: Control - Flags

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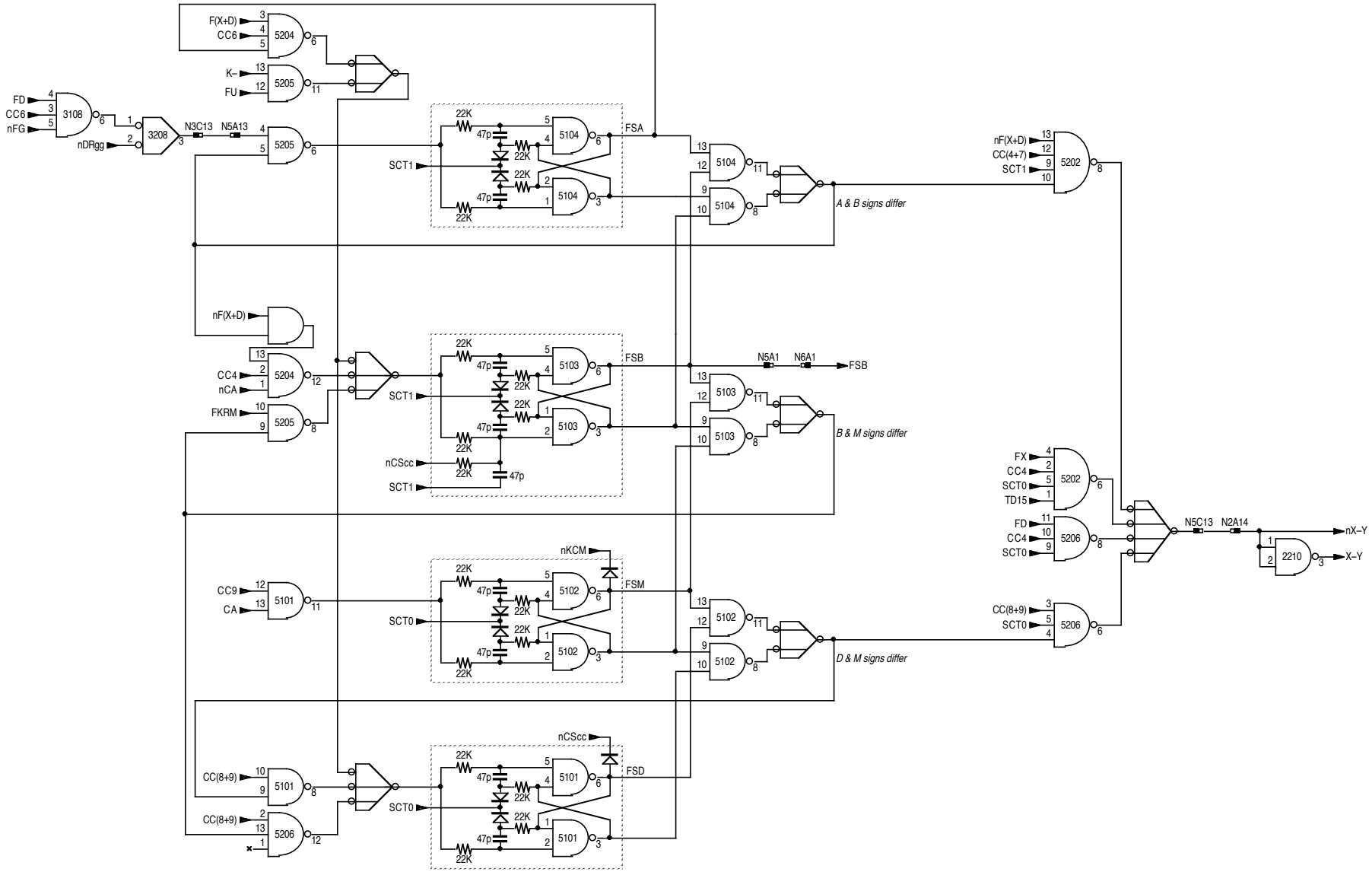

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Section: Sign Flags & Subtraction

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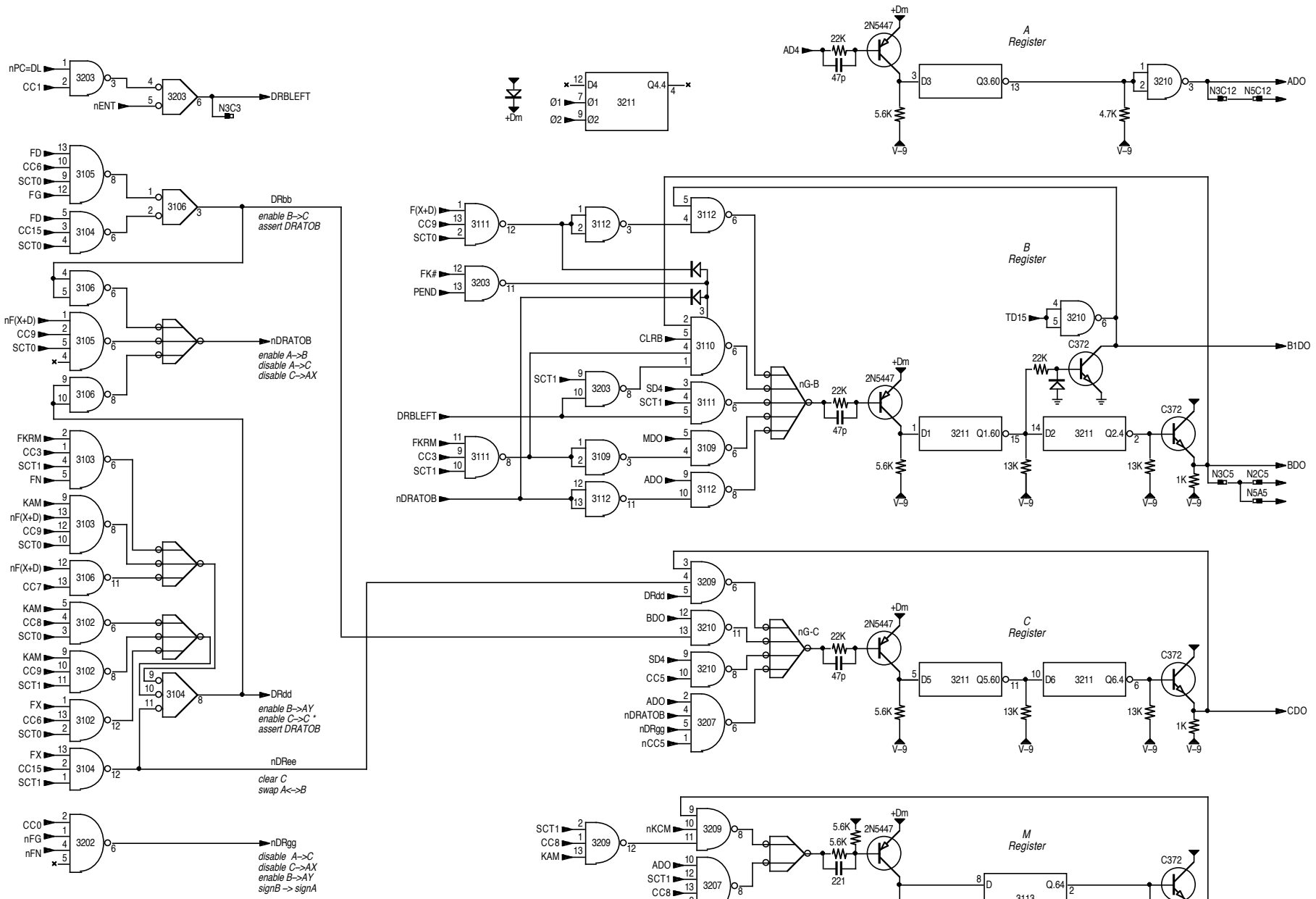

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Section: Data Routing & Memory

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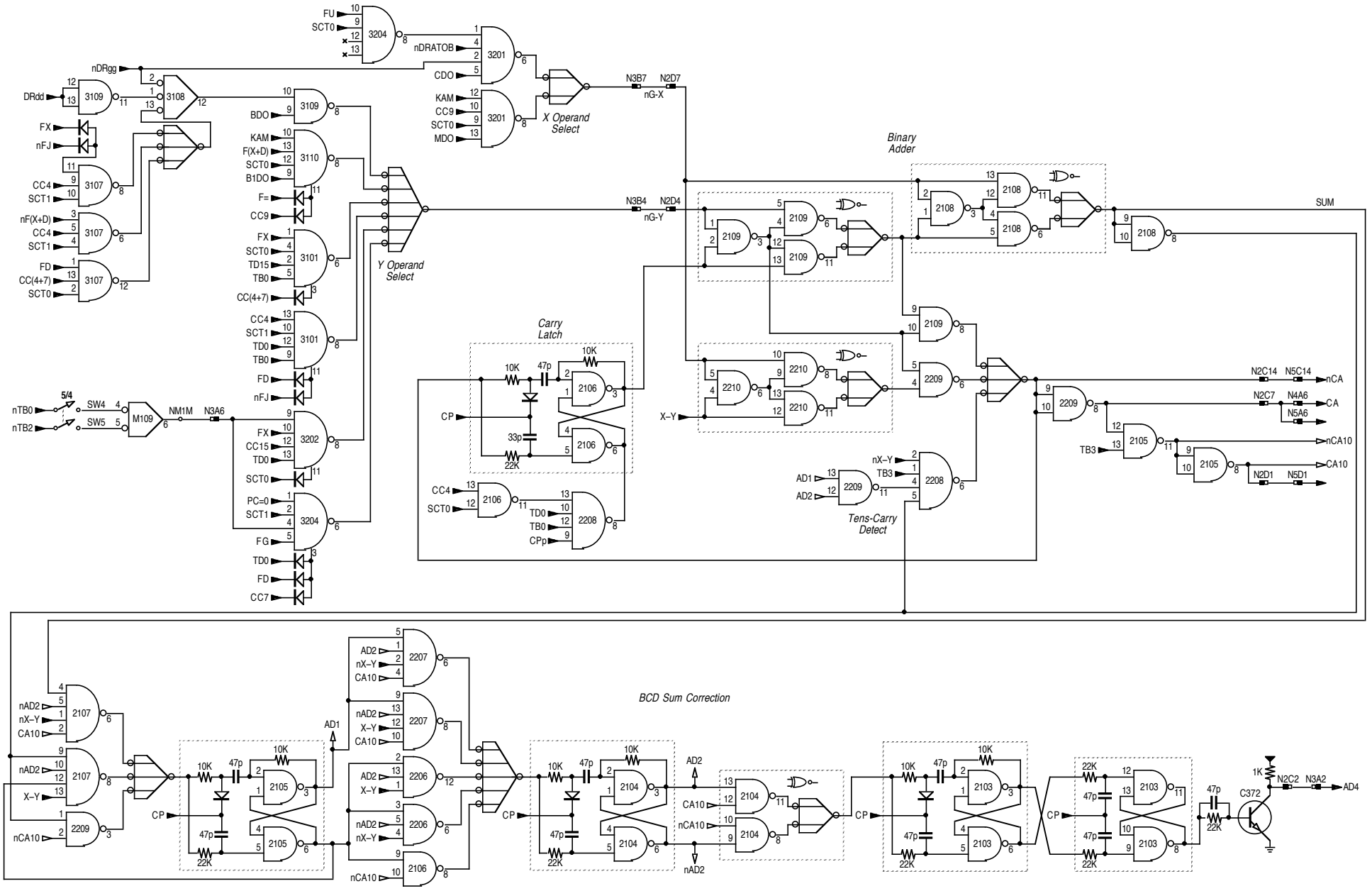

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Section: Arithmetic

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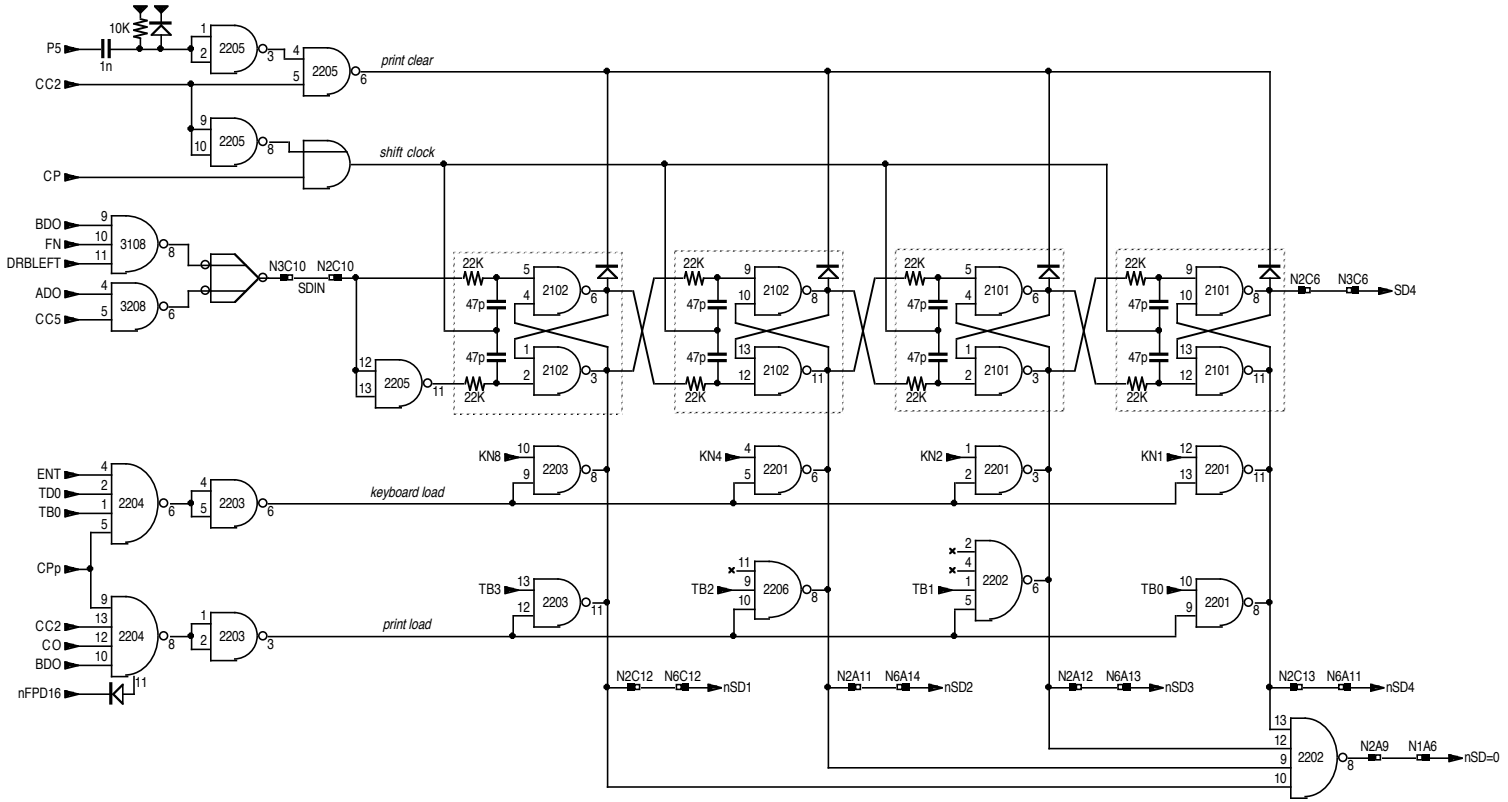

Canon EP151 Calculator

Section: SD Register

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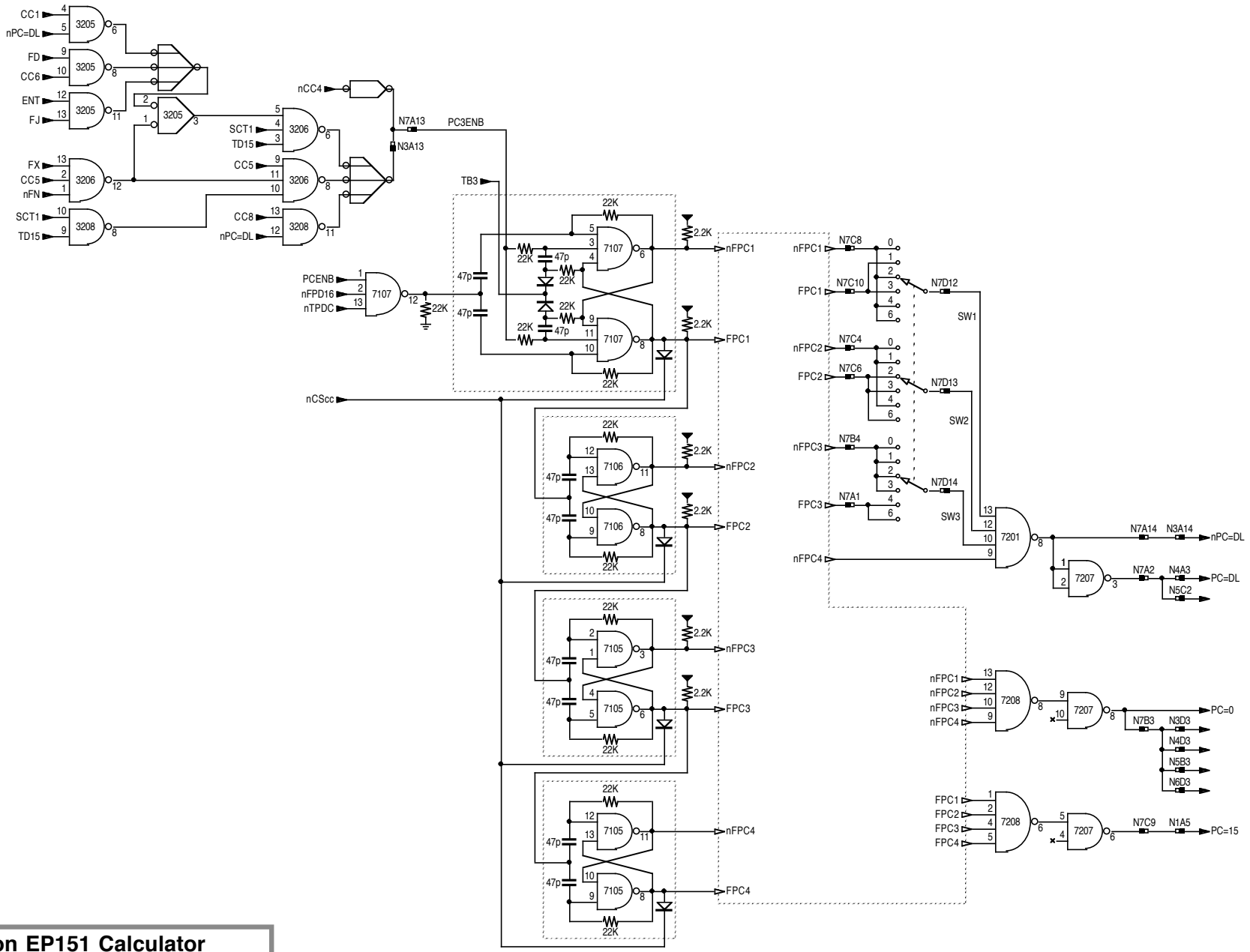

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Section: Point Counter

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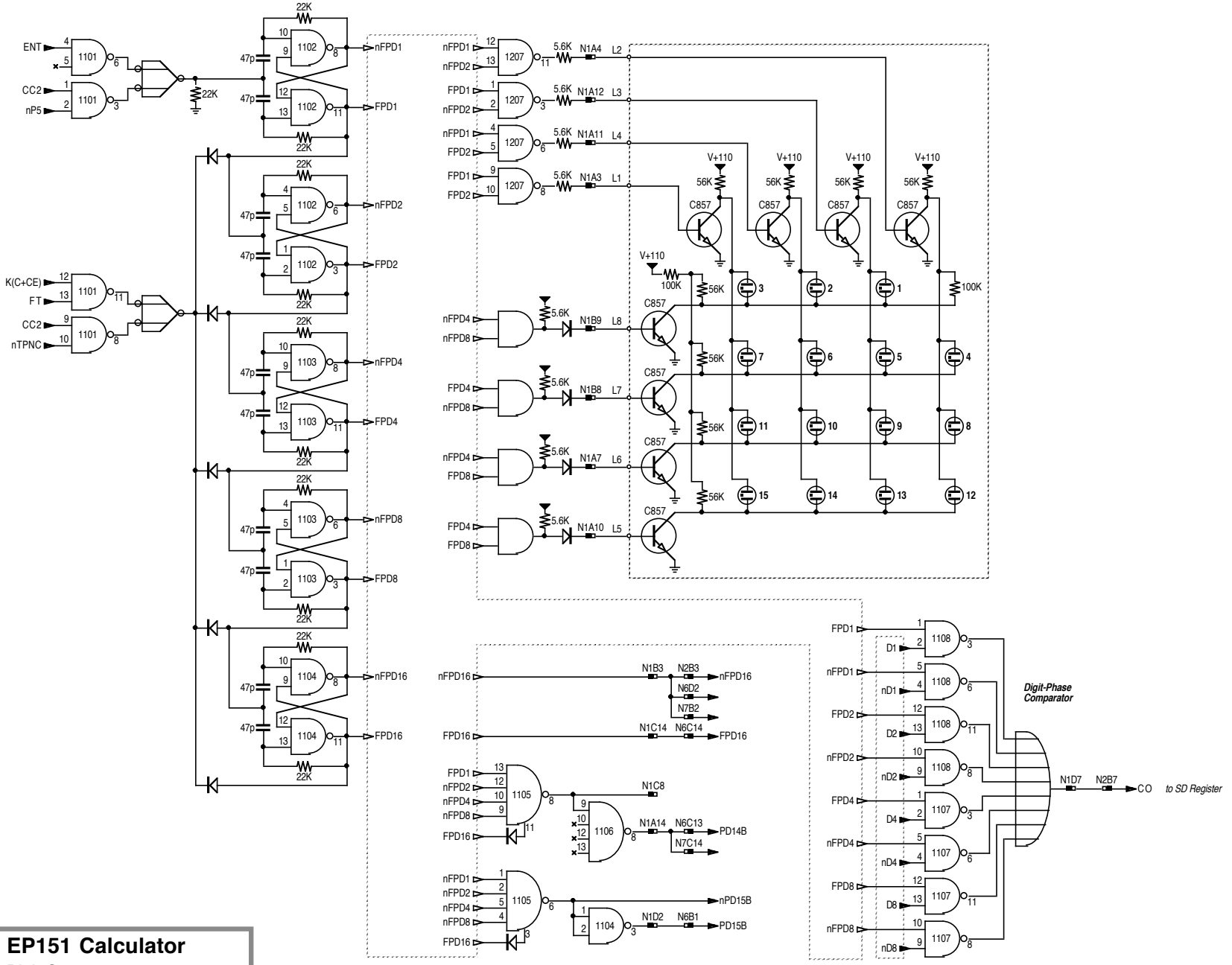

Canon EP151 Calculator

Section: Position Digit Counter

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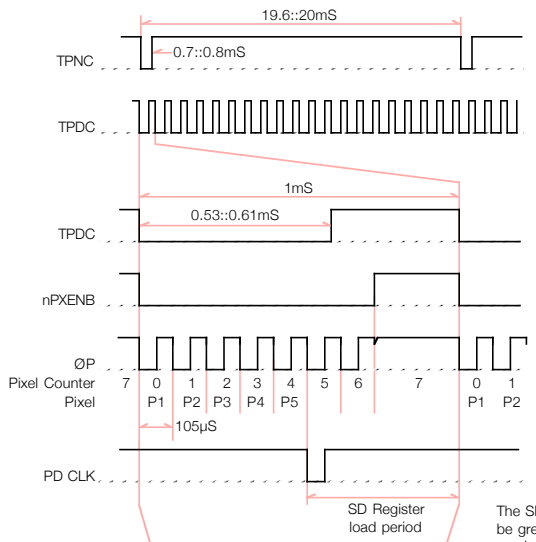
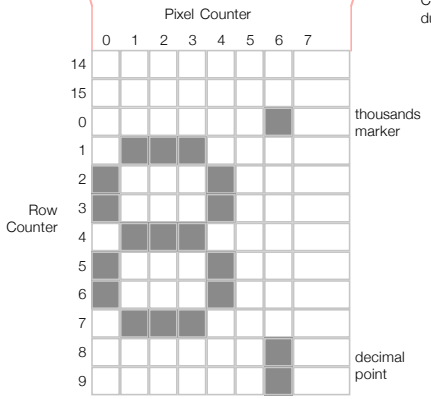
Printer Timing



The SD Register load period must be greater than the period of a number cycle (~200µS) to ensure that the SDR has an opportunity to obtain new digit data after the PD Counter has been incremented during a print scan line.

Character Cell Layout



Print Line Format

```
PD Counter:      0 1 2 3 4 5 6 7 8 9 A B C D E F1011
Digit Phase:     F E D C B A 9 8 7 6 5 4 3 2 1 0
Print Line:        n n n n n n n n n n n n n n m f

n = numeral
m = modifier character
f = function character
```

mf
C
M
CM
R
=
-=
x
÷
◊
#
%

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Section: Print Timing & Character Encoder
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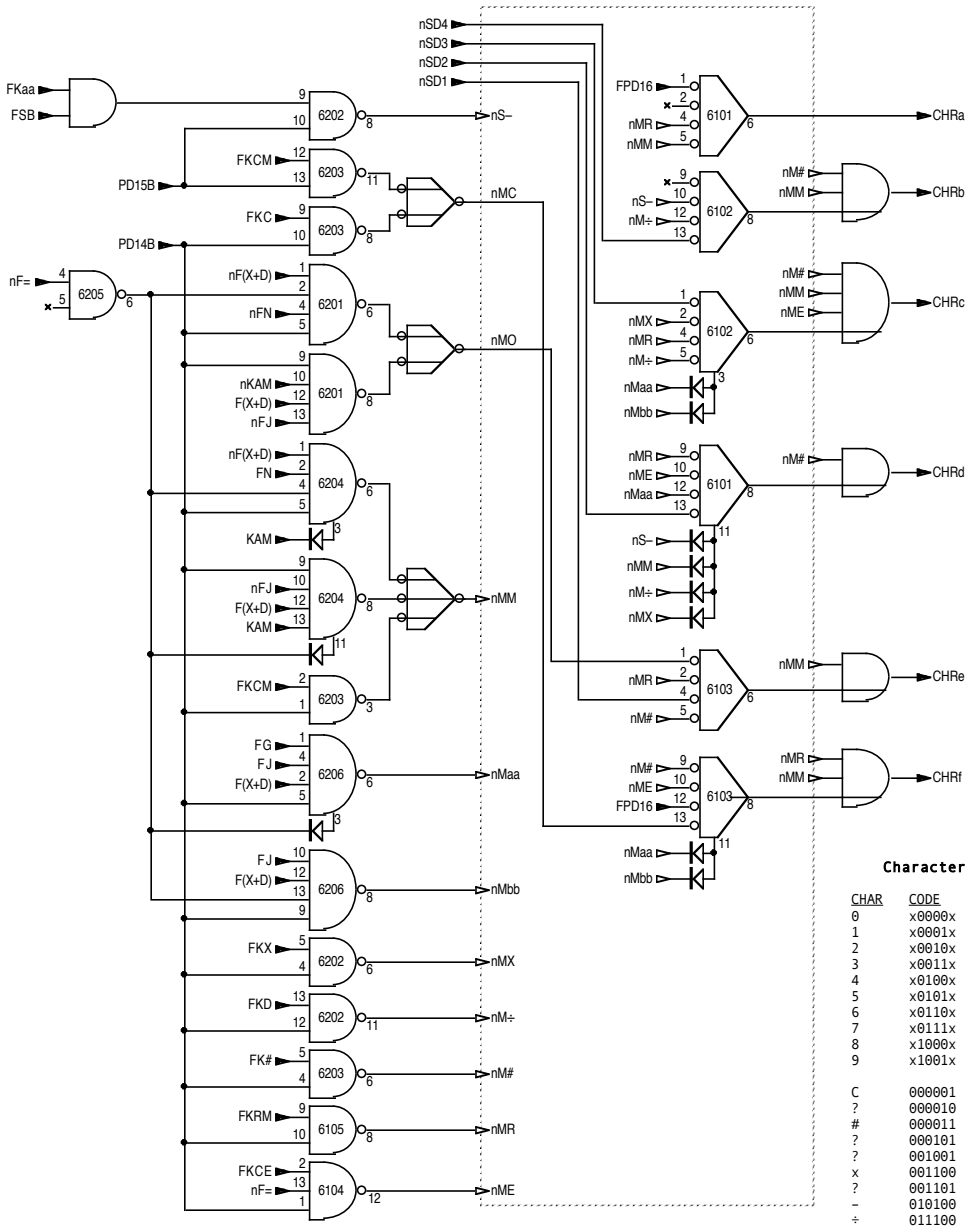
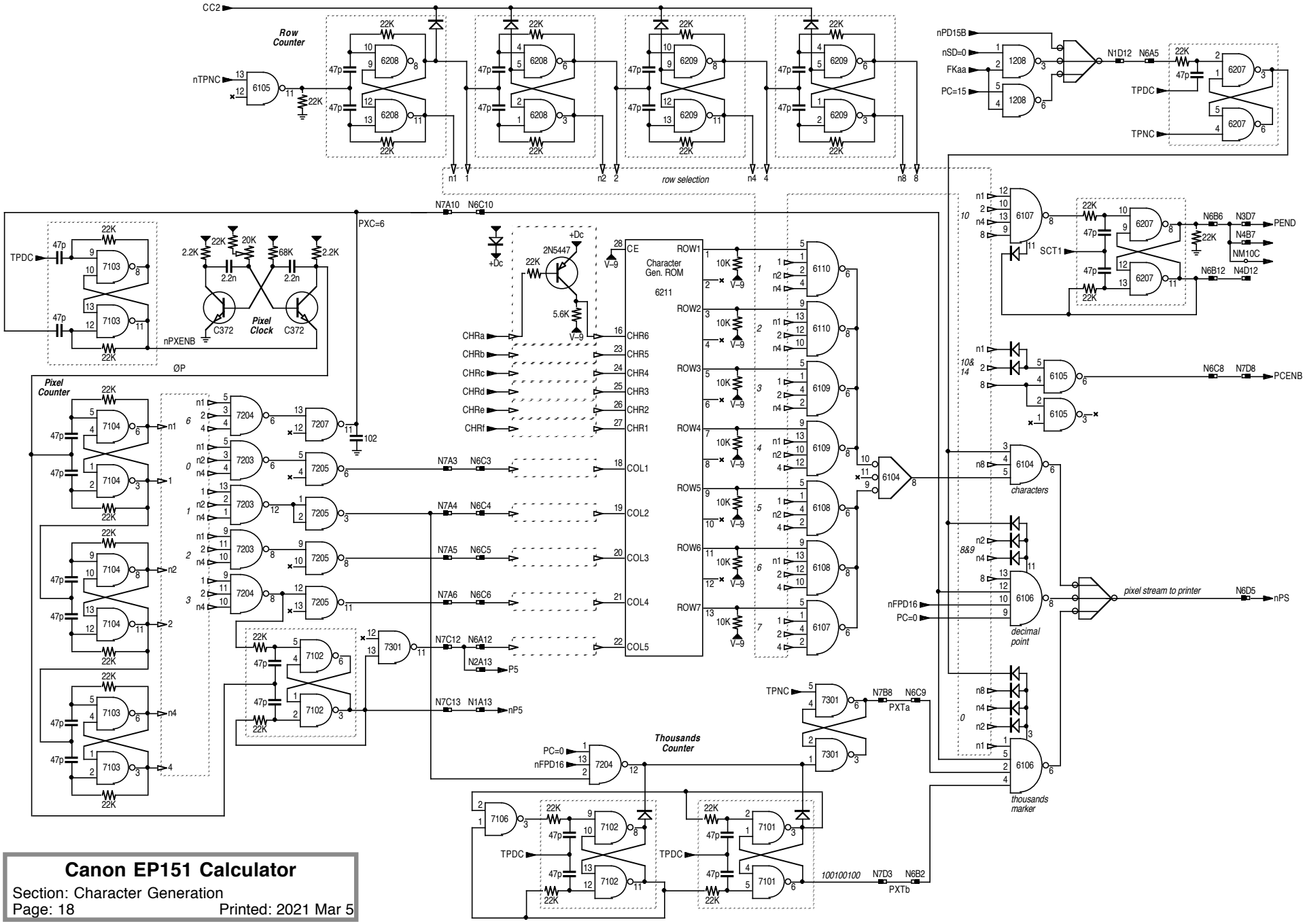


Character Codes

CHAR	CODE	SIG
0	x0000x	
1	x0001x	
2	x0010x	
3	x0011x	
4	x0100x	
5	x0101x	
6	x0110x	
7	x0111x	
8	x1000x	
9	x1001x	
C	000001	MC
?	000010	MO
#	000011	M#
?	000101	ME
?	001001	Mbb
x	001100	MX
?	001101	Maa
–	010100	S–
÷	011100	M÷
M	100100	MM
R	101110	MR
=	?	
◊	?	
%	?	



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Section: Character Generation

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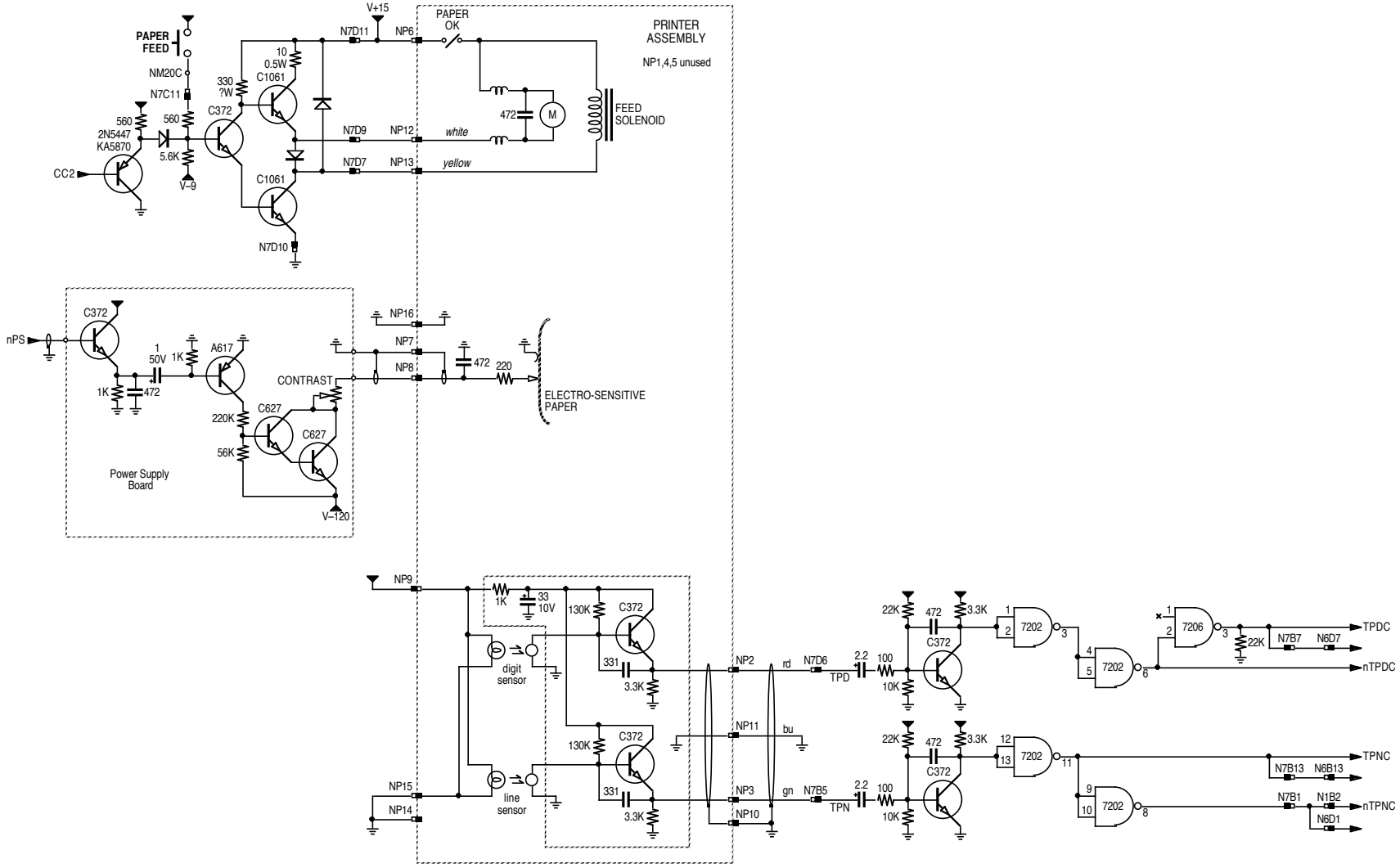
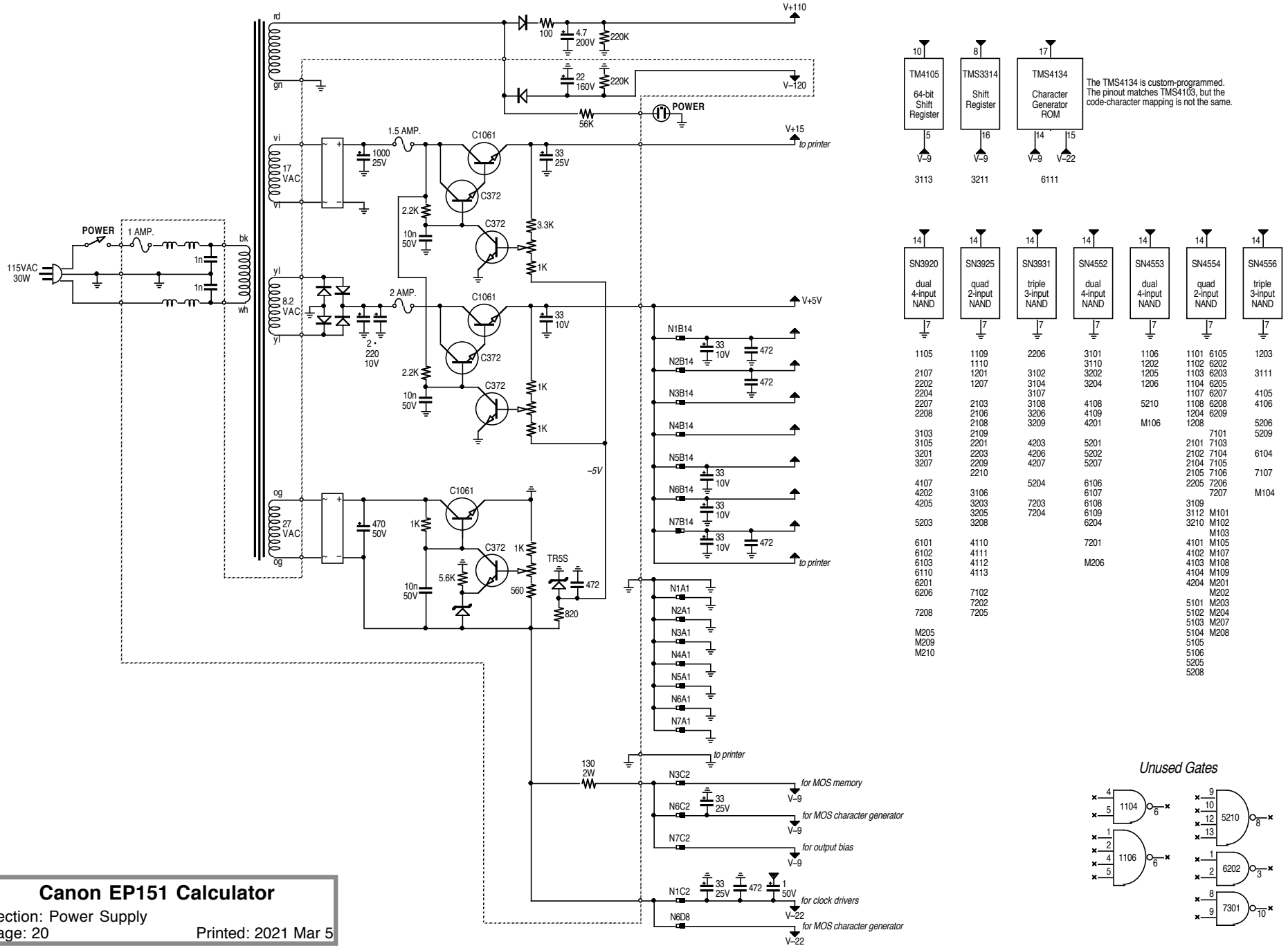

PAPER FEED
NM20C
N7C11
560
2N5447
KA5870
560
5.6K
V–9
CC2
C372
330 ?W
10 0.5W
C1061
C1061
N7D10
V+15
N7D11
NP6
PAPER OK
PRINTER ASSEMBLY
NP1,4,5 unused
472
M
FEED SOLENOID
N7D9
NP12
white
N7D7
NP13
yellow
nPS
C372
1K
1 50V
472
1K
A617
220K
56K
C627
C627
CONTRAST
V–120
Power Supply Board
NP16
NP7
NP8
472
220
ELECTRO-SENSITIVE PAPER
NP9
1K
33 10V
digit sensor
line sensor
130K
C372
331
3.3K
130K
C372
331
3.3K
NP15
NP14
NP2
rd
N7D6
TPD
NP11
bu
NP3
gn
N7B5
TPN
NP10
2.2
100
10K
22K
472
C372
3.3K
7202
7206
22K
N7B7
N6D7
TPDC
nTPDC
22K
472
C372
3.3K
7202
N7B13
N6B13
TPNC
N7B1
N1B2
N6D1
nTPNC



The TMS4134 is custom-programmed. The pinout matches TMS4103, but the code-character mapping is not the same.

SN3920 dual 4-input NAND	SN3925 quad 2-input NAND	SN3931 triple 3-input NAND	SN4552 dual 4-input NAND	SN4553 dual 4-input NAND	SN4554 quad 2-input NAND	SN4556 triple 3-input NAND
14	14	14	14	14	14	14
7	7	7	7	7	7	7
1105	1109	2206	3101	1106	1101 6105	1203
	1110		3110	1202	1102 6202	
2107	1201	3102	3202	1205	1103 6203	3111
2202	1207	3104	3204	1206	1104 6205	
2204		3107			1107 6207	4105
2207	2103	3108	4108	5210	1108 6208	4106
2208	2106	3206	4109		1204 6209	
	2108	3209	4201	M106	1208	5206
3103	2109				7101	5209
3105	2201	4203	5201		2101 7103	
3201	2203	4206	5202		2102 7104	6104
3207	2209	4207	5207		2104 7105	
	2210				2105 7106	7107
4107		5204	6106		2205 7206	
4202	3106		6107		7207	M104
4205	3203	7203	6108		3109	
	3205	7204	6109		3112 M101	
5203	3208		6204		3210 M102	
					M103	
6101	4110		7201		4101 M105	
6102	4111				4102 M107	
6103	4112		M206		4103 M108	
6110	4113				4104 M109	
6201					4204 M201	
6206	7102				M202	
	7202				5101 M203	
7208	7205				5102 M204	
					5103 M207	
M205					5104 M208	
M209					5105	
M210					5106	
					5205	
					5208	

Unused Gates

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Section: Power Supply

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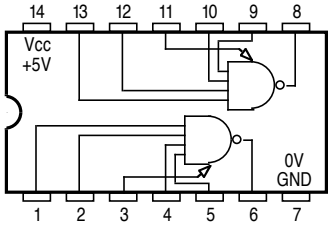
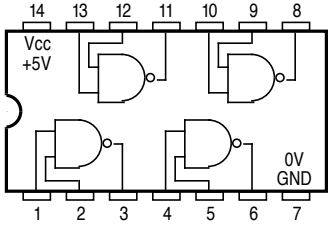
SN3900 / 4500 Series DTL Integrated Circuits

* SN4552 information derived through reverse engineering, others from manufacturer data sheet.

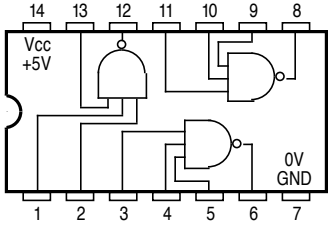
SN3920
SN4552*
SN4553



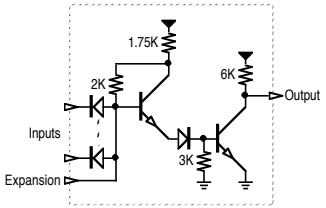
SN3925
SN4554



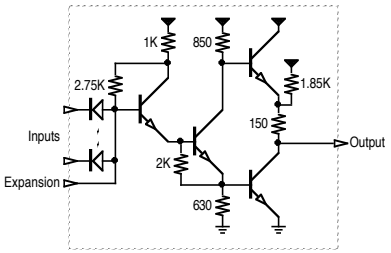
SN3931
SN4556



SN3920
SN3925
SN3931
SN4552*
SN4554



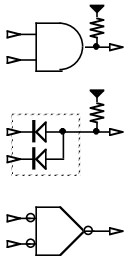
SN4553



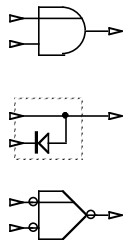
Discrete Gate Construction

A few gates are constructed from discrete diodes and resistors. The internal construction of these gates is shown in the following diagrams. A wire–AND construction is indicated by the input line traversing the width of the gate.

AND Gate



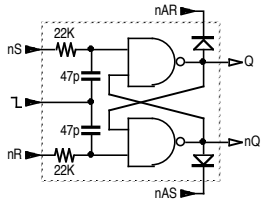
AND Gate with 'wired' input



Flip-Flops

Flip-flops are constructed from NAND gates with capacitor triggerring and resistors biasing inputs for control. Transitions occur on the negative edge of clock inputs.

The basic structure is that of a clocked SR flip-flop in which the SR inputs are assert-Low. Asynchronous Set and Reset inputs may be provided via output triggering.



Clocked-SR Flip-Flop with Asynchronous Set & Reset

nS	nR	CLK	Q	nQ
1	1	1–>0	–	–
0	1	1–>0	1	0
1	0	1–>0	0	1
0	0	1–>0	*	*

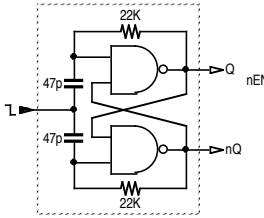
– no change
* undefined

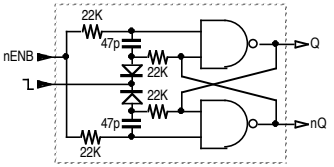
In a variation, the clock input to the capacitors may be separated to provide separate clocks for the S & R inputs.

Toggle Flip-Flops

A simple toggle flip-flop is formed by wrapping the SR inputs back from the outputs.

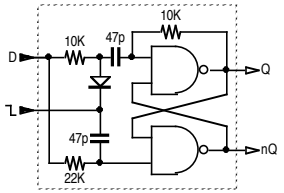
Another variation provides an assert-Low control input to enable toggling.





D Flip-Flop

A D flip-flop is formed with an asymmetric adaptation on the capacitor triggering.



N1

GND	1	1	**Ø2**
FKaa	2	2	V–22
L1	3	3	**Ø1**
L2	4	4	K(C+CE)
PC=15	5	5	**TD0**
nSD=0	6	6	**TB1**
L6	7	7	**TB2**
TD15	8	8	**~~nPD14B~~**
-	9	9	FT
L5	10	10	CC2
L4	11	11	FKC
L3	12	12	FK(X+D)
nP5	13	13	nFN
PD14B	14	14	**FPD16**

A	C		
B	D		
TB3	1	1	**CP**
nTPNC	2	2	**PD15B**
nFPD16	3	3	**nTD15**
-	4	4	**SCT1**
-	5	5	**SCT0**
nTB2	6	6	-
nTB0	7	7	**CO**
L7	8	8	-
L8	9	9	**TB0**
-	10	10	-
-	11	11	ENT
-	12	12	***1208.3,6..***
-	13	13	-
V+5	14	14	-

N2

GND	1	1	-
-	2	2	**AD4**
-	3	3	-
-	4	4	-
TD0	5	5	BDO
TB1	6	6	**SD4**
TB2	7	7	**CA**
-	8	8	-
nSD=0	9	9	-
CC2	10	10	SDIN
nSD2	11	11	-
nSD3	12	12	**nSD1**
P5	13	13	**nSD4**
nX–Y	14	14	**nCA**

A	C		
B	D		
-	1	1	**CA10**
-	2	2	CC4
nFPD16	3	3	-
CP	4	4	nG-Y
TB3	5	5	SCT0
-	6	6	-
CO	7	7	nG-X
-	8	8	**CPp**
TB0	9	9	-
KN1	10	10	-
KN2	11	11	ENT
KN4	12	12	-
KN8	13	13	-
V+5	14	14	-

N3

GND	1	1	Ø2
AD4	2	2	V–9
Ø1	3	3	-
FX	4	4	CC5
TD0	5	5	**BDO**
M109-6	6	6	SD4
nKCM	7	7	**MDO**
TD15	8	8	F(X+D)
FU	9	9	CC6
FD	10	10	**SDIN**
KAM	11	11	CC9
CLRB	12	12	**ADO**
PC3ENB	13	13	***3208.3***
nPC=DL	14	14	nCC5

A	C		
B	D		
CC(4+7)	1	1	CC1
CC4	2	2	CC7
SCT1	3	3	PC=0
nG-Y	4	4	SCT0
nENT	5	5	FG
FKRM	6	6	FN
nG-X	7	7	PEND
FK#	8	8	CC15
TB0	9	9	F=
nF(X+D)	10	10	CC8
nFG	11	11	ENT
CC0	12	12	nFN
FJ	13	13	CC3
V+5	14	14	nFJ

N4

GND	1	1	**nFJ**
nFCC1SE	2	2	**CC0**
PC=DL	3	3	**CC(8+9)**
CC5	4	4	K(C+CE)
nF=RE	5	5	nFKCE
CA	6	6	KAM
nFKENT	7	7	FX
F(X+D)	8	8	nFOF
KP	9	9	FU
CC2	10	10	**CC6**
CC9	11	11	FT
nK(C+CE)	12	12	nFH
nCScc	13	13	**CLRB**
nKC	14	14	**nCC5**

A	C		
B	D		
CC1	1	1	**CC(4+7)**
CC7	2	2	**CC4**
SCT1	3	3	PC=0
SCT0	4	4	nENT
FG	5	5	FKRM
FN	6	6	FK(X+D)
PEND	7	7	FKENT
CC15	8	8	nFKCM
F=	9	9	nF(X+D)
CC8	10	10	**nFG**
nFCC2SE	11	11	**nCC4**
nFN	12	12	nPEND
CC3	13	13	**FJ**
V+5	14	14	**nCC0**

N5

GND	1	1	**FSB**
CC0	2	2	PC=DL
CC(8+9)	3	3	CC1
CC5	4	4	FX
BDO	5	5	TD0
CA	6	6	**nFU**
MDO	7	7	nKCM
~~nFOF~~	8	8	TD15
F(X+D)	9	9	**FU**
CC6	10	10	FD
FT	11	11	CC9
nFH	12	12	ADO
3208.3	13	13	**nX–Y**
nCC5	14	14	nCA

A	C		
B	D		
CC(4+7)	1	1	CA10
CC4	2	2	nTD15
PC=0	3	3	SCT1
SCT0	4	4	FG
FKRM	5	5	nKST
FK(X+D)	6	6	KCE
nFKENT	7	7	**nSFOF2**
CPp	8	8	-
nFXDR	9	9	nF(X+D)
nFG	10	10	nCScc
K–	11	11	ENT
nF=	12	12	FN
n(Fmlt...K))	13	13	nKK
V+5	14	14	FJ

N6

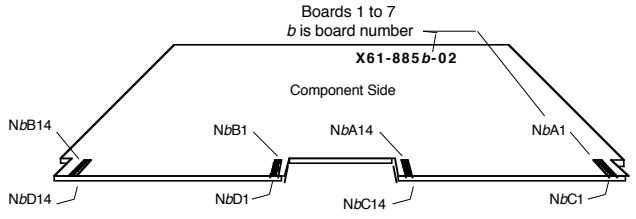
GND	1	1	FSB
nFJ	2	2	V–9
-	3	3	P1
-	4	4	P2
1208.3,6...	5	5	P3
-	6	6	P4
FKaa	7	7	nFK#
F(X+D)	8	8	**PCENB**
FKENT	9	9	PXTa
CC2	10	10	PXC=6
nSD4	11	11	KAM
P5	12	12	nSD1
nSD3	13	13	PD14B
nSD2	14	14	FPD16

A	C		
B	D		
PD15B	1	1	nTPNC
PXTb	2	2	nFPD16
SCT1	3	3	PC=0
FG	4	4	FKRM
FN	5	5	**PS**
PEND	6	6	nKAM
FK#	7	7	TPDC
-	8	8	V–22
nF(X+D)	9	9	nF=
FKCE	10	10	FKCM
FKX	11	11	FKC
nPEND	12	12	nFN
TPNC	13	13	FKD
V+5	14	14	FJ

N7

GND	1	1	**FPC3**
PC=DL	2	2	V–9
P1	3	3	K(C+CE)
P2	4	4	**nFPC2**
P3	5	5	nSFOF1
P4	6	6	**FPC2**
nKCM	7	7	MDO
nFOF	8	8	**nFPC1**
FT	9	9	**PC=15**
PXC=6	10	10	**FPC1**
CC2	11	11	*paper feed*
nKC•nKCE	12	12	**P5**
PC3ENB	13	13	**nP5**
nPC=DL	14	14	PD14B

A	C		
B	D		
nTPNC	1	1	CP
nFPD16	2	2	TB3
PC=0	3	3	**PXTb**
nFPC3	4	4	**LM**
TPN	5	5	**OF**
nSFOF2	6	6	TPD
TPDC	7	7	**CLA**
PXTa	8	8	PCENB
SCT1	9	9	**MO**
nCScc	10	10	GND
ENT	11	11	V+15
nFN	12	12	SW1
TPNC	13	13	SW2
V+5	14	14	SW3



Board	Primary Functions
Main	Keyboard Encoding and Latches
1	Timing and PD Counter
2	Arithmetic
3	Memory and Data Routing
4	Control (State Machine)
5	Control (Flags)
6	Character Encoding and Generation
7	Character Generation, Printer Interface, Point Counter

Notes:

❖ As viewed from bottom of main board/backplane.

❖ Bold-faced expressions are signal sources.