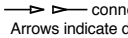
Casio AL-1000 Calculator

Contents

Notes

- Gate symbols and signal names are presented in accordance with:
  logic 0 = 0V, GND
  logic 1 = +12V
- The symbol  denotes a physical connector pin where *b*=board (1-7), *s*=section (A,B), and *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
-  connection between different sections.
   connection limited to same section.
  Arrows indicate direction of signal or energy flow.
- The symbol  denotes V+12. The symbol  denotes V–6.
- Capacitance in microfarads unless otherwise indicated.
- These drawings based on a unit missing the case and power supply. “7530” is stamped on some of the PCBs.
- Drawn Oct 2003 / Feb 2005 by bhilpert. See www.cs.ubc.ca/~hilpert/eec for additional information.

Gate Identification

Gates involving a transistor are identified by symbols taking the following form:

<board><function><enumeration>

where

<board> = 1 to 7

<function> =
NA for NAND
NO for NOR
N for NOT
E for Buffer (non-inverting)

<enumeration> = 1 to n

Flip-flops are identified by symbols taking the following form:

<board><name>

where

<board> = 1 to 7

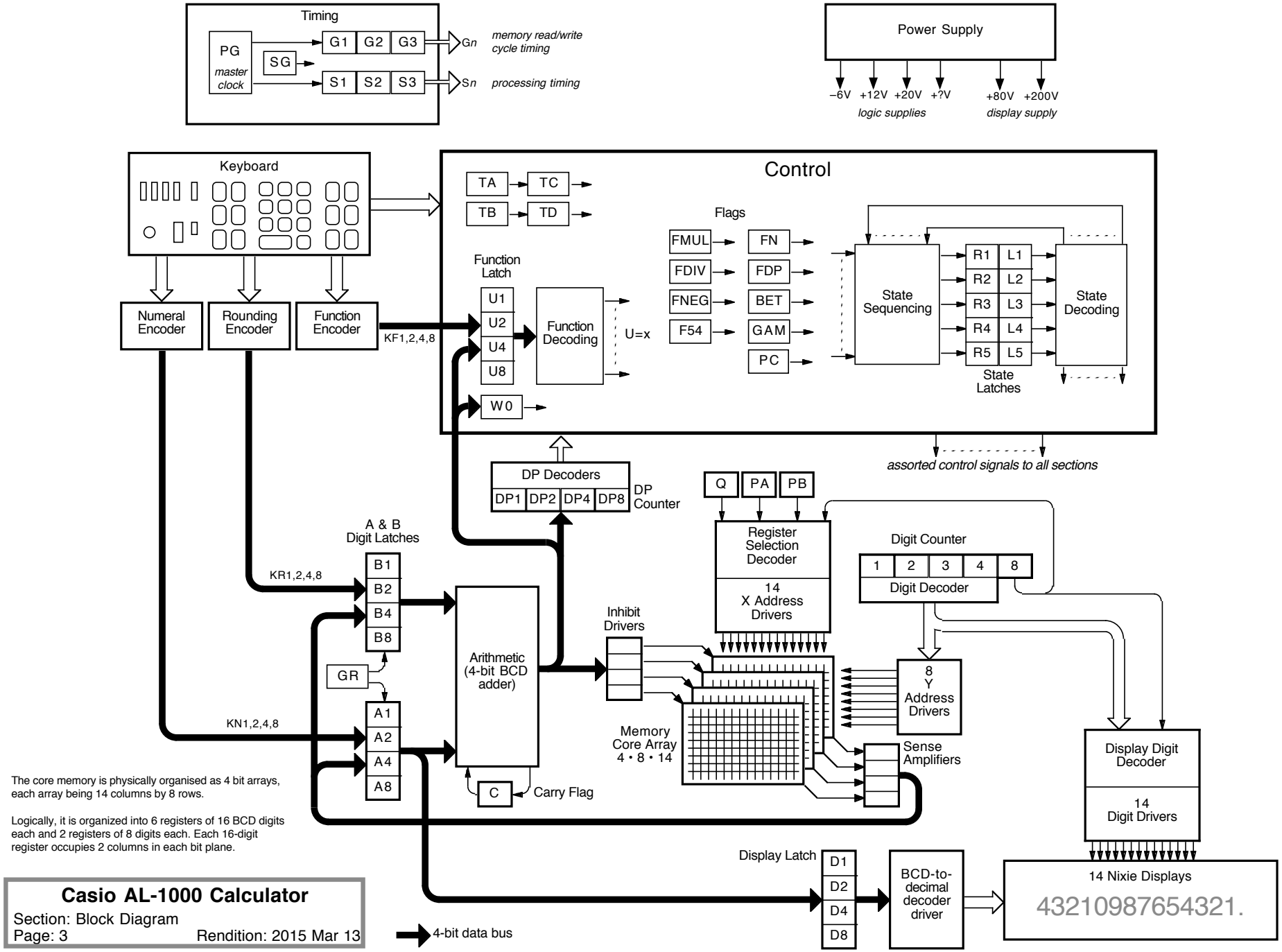
<name> = is taken from the name silkscreened on the board.

The preceding name formats are taken from silkscreening on the printed circuit boards. Names beginning with a “$” were created for the sake of a simulation and have no origin in the original machine.

Sections and Signal Descriptions

Signal names associated to a flip-flop are obtained from labeling on the printed circuit boards. A lowercase “n” at the beginning of a signal name indicates the logical NOT operation.

Section	Signal	Description
Timing	PG	Master clock.
	SG	A flag to select between memory cycles and state cycles.
	G1,2	Timing signals for core memory read/write cycles.
	S1,2,3	Timing signals for state cycling.
	POR…	Power-On-Reset.
Keyboard	KN1,2,4,8	Encoded numeral keys.
	KNP	Numeral key pressed.
	KF1,2,4,8	Encoded function keys.
	KFP	Function key pressed.
	KR1,2,4,8	Encoded position of the rounding switch.
Control	TA,B,C,D	Latch for the T state machine.
	TS…	Assorted states from the T state machine.
	U1,2,4,8	4-bit function latch.
	U=*x*	Function is *x*.
	U…	Function signals derived with additional logic.
	FMUL, FDIV	Flags indicating that the next add/subtract completes a multiply or divide.
	F54	Flag to take the state machine through the rounding sequence.
	FNEG	Flag indicating whether the displayed number is negative.
	NST*x*	Next state in function execution.
	L1…L5	Current function execution state in binary form(bits of L latch).
	ST*x*	Current function execution state in enumerated form.
	ST*name*	State combinations with a particular intent.
	CAR…	Control output to Arithmetic.
	FN	During number entry, flag indicating whether a new number or within a number.
	FDP	Flag indicating that the decimal point has been pressed during number entry.
	GAM	(Gamma) Flag to capture data states within a number cycle
	BET	(Beta) Flag for miscellaneous uses during function execution.
	W0	Flag to capture zero-state of output from arithmetic (W=0).
	PC	Flag indicating the completion of program execution.
Decimal Point Counter	DP=n	Assorted signals indicating when the DP counter matches n. Also used as a digit counter during multiply, divide and square root.
Digit Counter	DGT*n*	Individual digit timing.
	DGT*n.m*	1 to 8 digit scanning, address for memory Y-axis.
	DC8	8-th bit of memory digit scanning.
Register Selection	RS*rr*	Selected register, address for memory X-axis.
	Q	Selects the X or Y operand register.
	PA	Selects between data registers and program storage.
	PB	Selects between program 1 and program 2.
A, B Latches	A1,2,4,8	Two 4-bit latches to hold digits from memory and keyboard, and which feed the arithmetic unit.
	B1,2,4,8	
	GR	Flag to select the A or B latch to be loaded with data from core memory.
Arithmetic	W1,2,4,8	Result of addition or subtraction of digits in A and B latches.
	C	Tens Carry Flag.
Memory Data	MR1,2,4,8	4-bit digit read from memory.
D Latch	D1,2,4,8	A 4-bit latch to hold the digit being displayed.



The core memory is physically organised as 4 bit arrays, each array being 14 columns by 8 rows.

Logically, it is organized into 6 registers of 16 BCD digits each and 2 registers of 8 digits each. Each 16-digit register occupies 2 columns in each bit plane.

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Section: Block Diagram

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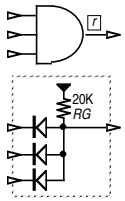
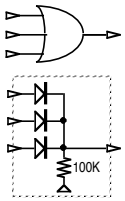
AND Gates



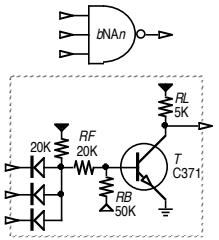
r	RG
%	10K
&	15K
%2	10K to V+20
@2	20K to V+20
-	none

The pull-up resistor on AND gates varies. Most are 20K, those that differ are indicated by a symbol at the output in accordance with the above table.

OR Gates



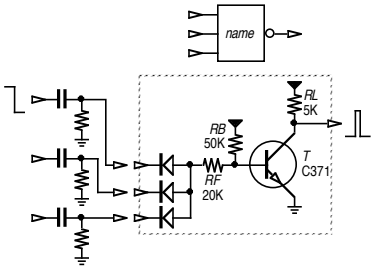
NAND Gates



NAND Gates - Exceptions

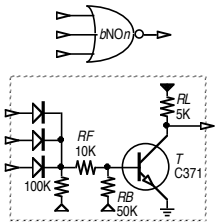
	Name	RF	RB	RL	T	Notes
6	NA1	10	100			EDGE
6	NA2	10	100			EDGE
6	NA3			2		
6	NA8					NOR
6	NA9					NOR
8	NA2			2	C641	
8	NA3			2	C641	
8	NA5			2	C641	
8	NA7				C641	
10	NA1			2		
10	NA2			2		CF=200PF
10	NA3			2		CF=200PF
10	NA4			2		CF=200PF
10	NA5			2		CF=200PF

Edge Pulse Gates



The 'Edge Pulse' gates are fed by differentiating capacitors and resistors and are biased in such a manner that the input normally appear as 1 and the ouput 0. A 1->0 transition at an input to a capacitor sends a differentiated negative-going pulse to the transistor, enough to briefly turn the transistor off so that a 1 pulse appears at the output.

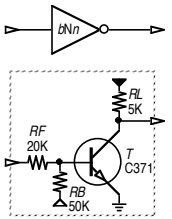
NOR Gates



NOR Gates - Exceptions

	Name	RF	RB	RL	T	Notes
2	NO1	15	100	2	C641	
2	NO2		100		C641	NAND
2	NO3	15		2	C641	
2	NO4				C641	INVERTER
3	NO1					NAND
3	NO2	15				
3	NO3	15				
3	NO4	15				
3	NO5	15				
4	NO16				C641	
5	NO2					NAND
5	NO8					NAND
5	NO14					NAND
5	NO15					BUFFER
6	NO1					EDGE
6	NO2					EDGE
6	NO5	20				
7	NO2			2		
7	NO4			2		
7	NO5			2		
7	NO7			2		
8	NO1		100		C641	EDGE
8	NO2		100			INVERTER, V+20
8	NO3	20	100		C372	V+20
10	NO1			2		NAND
10	NO2	20		2		
10	NO3	20		2		
10	NO4	20		2		
10	NO5	20		2		

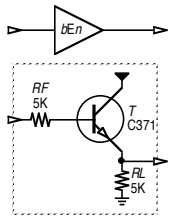
Inverters



Inverters - Exceptions

	Name	RF	RB	RL	T	Notes
1	N1	15			C641	EDGE
1	N2	15			C641	EDGE
1	N3	15			C641	EDGE
1	N4	15			C641	EDGE
2	N1		100	2	C641	
2	N2			2	C641	NAND
2	N3	15		2		
2	N7	10				
2	N9	15	50		C641	EDGE
4	N7			2		
5	N3		100			
8	N1				C372	
8	N3			2	C641	
8	N4		100			V+20
8	N5			2	C641	
8	N6		100			V+20
8	N7				C641	
8	N8				C641	
8	N9			2	C641	
9	N1	10		2		EDGE (no diode)
9	N2	10		2		EDGE (no diode)
10	N5	10		2	C641	EDGE (no diode)

Buffers

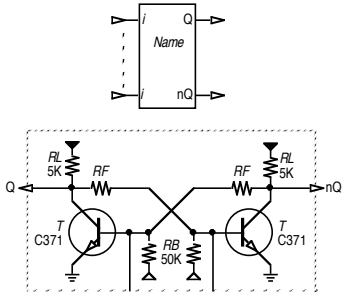


Buffers - Exceptions

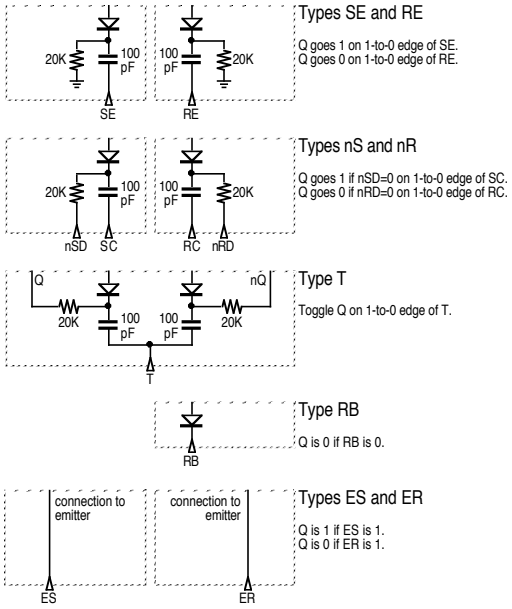
	Name	RF	RB	RL	T	Notes
6	E1	2	-	2		
6	E2	2	-			

- Logic 0 = GND
- Logic 1 = V+12
- Most gates adhere to the standard construction and component values as indicated in the above module diagrams. Exceptions are noted in the tables.
- A few gates are mislabeled relative to their construction. These are indicated in the Notes column with their correct function.
- The load resistor of a few gates is supplied from V+20 rather than V+12. These are noted in the Notes column.

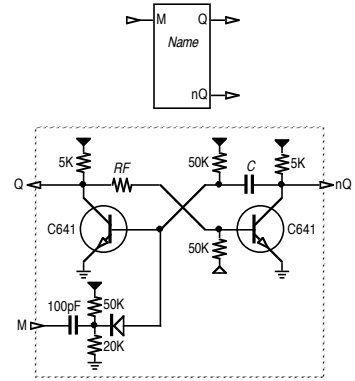
Bistable Flip-Flops



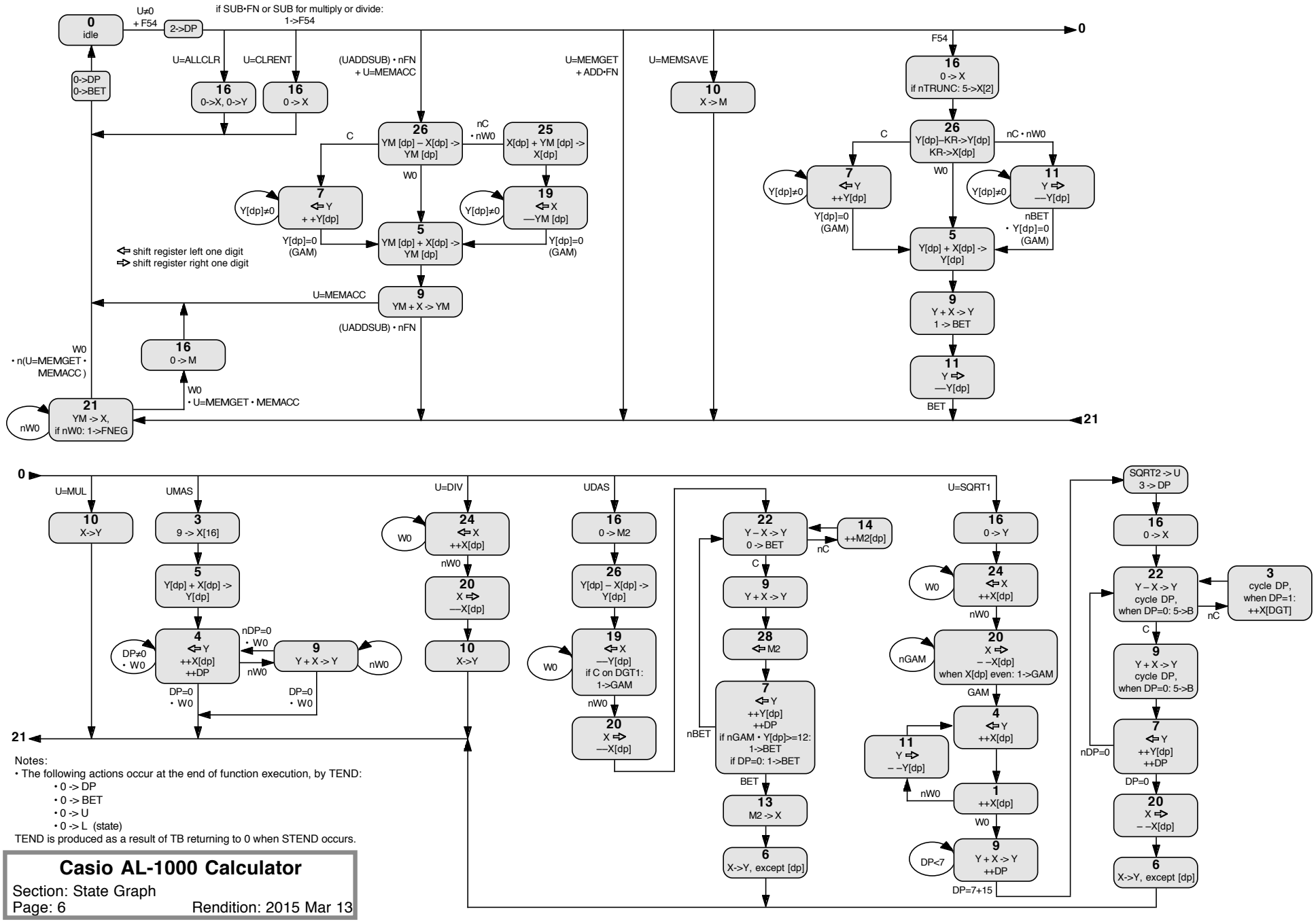
Bistable Flip-Flop Input Options



Monostable Flip-Flops



Flip	Flops						Flip	Flops					
	Name	RF	RB	RL	T	Notes		Name	RF	RB	RL	T	Notes
1	D1	15		2	C641		6	PG	-		2	C641	astable
1	D2	15		2	C641		6	SG	20	30, 68	2		
1	D4	15		2	C641		6	S1	20		2		
1	D8	15		2	C641		6	S2	20		2		
							6	S3	20		2		
2	ST	20	100				6	G1	15		2	C641	
2	Sr	20	-		C641	monostable C=0.0047	6	G2	15		1	C641	
2	DP1	15		2	C641		6	G3	15		2	C641	
2	DP2	15		2	C641		6	GR	15		2	C641	
2	DP4	15		2	C641		6	AC	20	30, 68			
2	DP8	15		2	C641		6	TA	15		2	C641	
							6	TB	15		2	C641	
3	FMUL	30	100				6	TC	15		2	C641	
3	FDIV	30	100				6	TD	15	68, 50	2	C641	
3	F54	30	100				6	h	15	-		C641	monostable C=0.2
3	FNEG	15		2	C641								
3	FN	30	100				7	A1	15		2		
3	FDP	30	100				7	A2	15		2		
3	U1	30	100		C372	V+20	7	A4	15		2		
3	U2	30	100			V+20	7	A8	15		2		
3	U4	30	100			V+20	7	B1	15		2		
3	U8	30	100			V+20	7	B2	15		2		
							7	B4	15		2		
4	BET	15		2	C641		7	B8	15		2		
4	GAM	15		2	C641		7	C	30	100			
5	L1	20	100				8	PA	30	100		C641	V+20
5	L2	20	100				8	PB	30	100		C641	V+20
5	L3	20	100				8	PC	30	100			
5	L4	20	100				8	Q	30	100		C641	V+20
5	L5	20	100				8	1	30	100		C641	V+20
5	R1	30	100				8	2	30	100		C641	V+20
5	R2	30	100				8	3	30	100		C641	V+20
5	R3	30	100				8	4	30	100	2 + 3	C641	V+20
5	R4	30	100				8	8	30		2	C641	V+20
5	R5	30	100										
							10	W0	20		2		



Notes:

- The following actions occur at the end of function execution, by TEND:
  - 0 -> DP
  - 0 -> BET
  - 0 -> U
  - 0 -> L (state)

TEND is produced as a result of TB returning to 0 when STEND occurs.

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Section: State Graph

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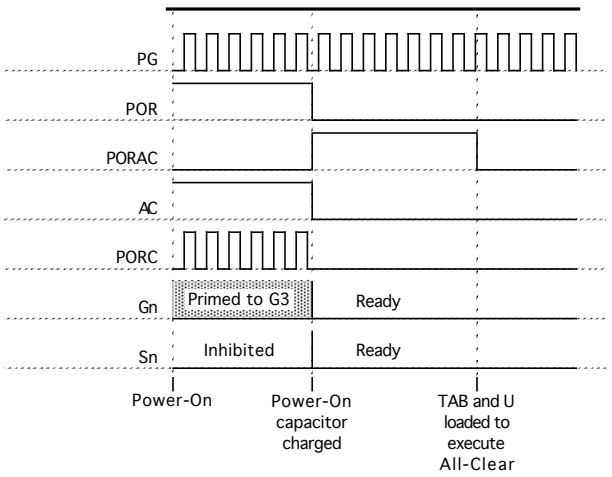
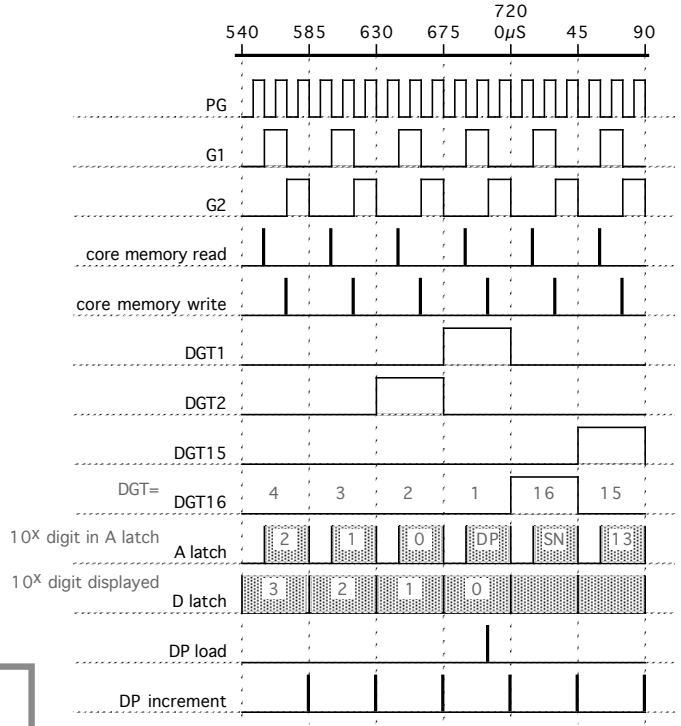
Group	State	Used During	Actions	ST2DGT	STCOPY	STSHIFT	STDPONLY	STYFIRST	CARSUB	STDGTINC	Other State Signals
Idle	0	-	-								
Shift Left	4	UMAS,SQRT1	shift Y left, ++X[dp]			•					STFLIPRADP
		UMAS	++DP			•					STFLIPRADP
	7	UADDSUB,UDAS,SQRT2,F54	shift Y left, ++Y[dp]			•		•	DGT1		
		UDAS,SQRT2	++DP			•		•	DGT1		
		UDAS	if nGAM•Y[dp]>=12 or DP=0: 1->BET			•		•	DGT1		
	19	UADDSUB,UDAS	shift X left, --Y[dp]			•		•	DGT1		STFLIPRADP
		UDAS	if C on DGT1: 1->GAM			•		•	DGT1		STFLIPRADP
	24	DIV,SQRT1	shift X left, ++X[dp]			•					
	28	UDAS	shift M2 left including [dp]			•		•			STM2FORY
Shift Right	11	SQRT1,F54	shift Y right, --Y[dp]			•		•	DGT1		STDGTDOWN
	20	DIV,UDAS,SQRT1,SQRT2	shift X right, --X[dp]			•			DGT1		STDGTDOWN
		SQRT1	if X[dp]=even after decrement: 1->GAM			•			DGT1		STDGTDOWN
Arithmetic	9	UADDSUB,UMAS,UDAS,SQRT1,SQRT2,F54	YM + X -> YM, 0 -> FNEG	•					negate*	•	
		F54	1 -> BET	•					negate*	•	
		SQRT1	++DP	•						•	
		SQRT2	cycle DP, when DP=0: 5->B	•						•	
	22	UDAS,SQRT2	Y - X -> Y, 0 -> BET	•					•	•	
		SQRT2	cycle DP, when DP=0: 5->B	•					•	•	
Register Copy	6	UDAS,SQRT2	X -> Y, but [dp] not copied	•	•					•	
	10	MUL,DIV	X -> Y	•	•				negate*		
		MEMSAVE	X -> M	•	•				negate*		
	13	UDAS	M2 -> X	•	•			•			STM2FORY
	21	fin	YM -> X, if nW0: 1->FNEG	•	•			•	negate		
Decimal Point Only	1	SQRT1	++X[dp]				•				
	5	UADDSUB,UMAS,F54	Y[dp] + X[dp] -> Y[dp]	•			•				
	14	UDAS	++M2[dp]				•	•			STM2FORY
	25	UADDSUB	X[dp] + Y[dp] -> X[dp]	•			•	•			
	26	UADDSUB,UDAS	Y[dp] - X[dp] -> Y[dp]	•			•		•		
		F54	Y[dp] - KR -> Y[dp], KR -> X[dp]	•			•		•		
Clearing	16	ALLCLR	0 -> X, 0 -> Y	•	•						
		CLRENT,SQRT2,F54,fin	0 -> X								
		UDAS	0 -> M2					•			STM2FORY
		SQRT1	0 -> Y					•			
		MEMGET	0 -> M					•			
		F54	if nTRUNC: 5 -> X[2]								
Other	3	UMAS	9 -> X[16]								
		SQRT2	cycle DP, when DP=1: ++X[DGT]								

negate: if FNEG: CARSUB occurs during nDGT1
negate*: may negate under some circumstances(?)

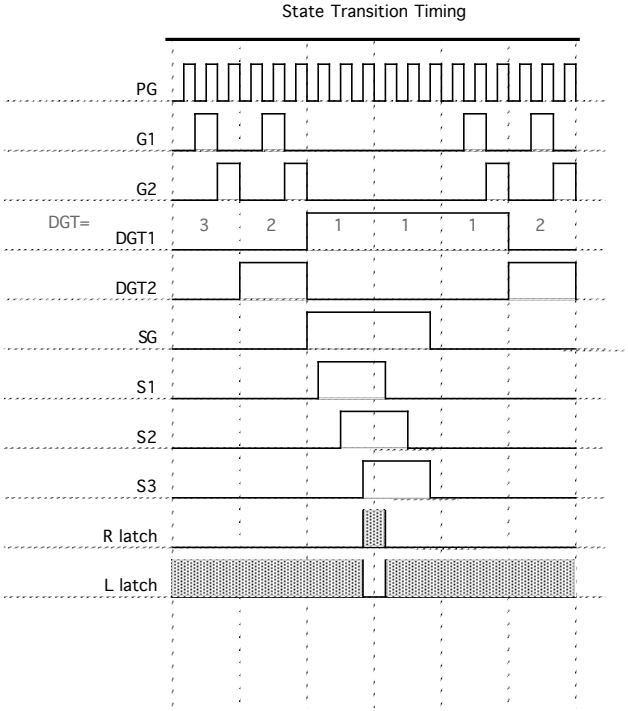
Power-On Timing Sequence



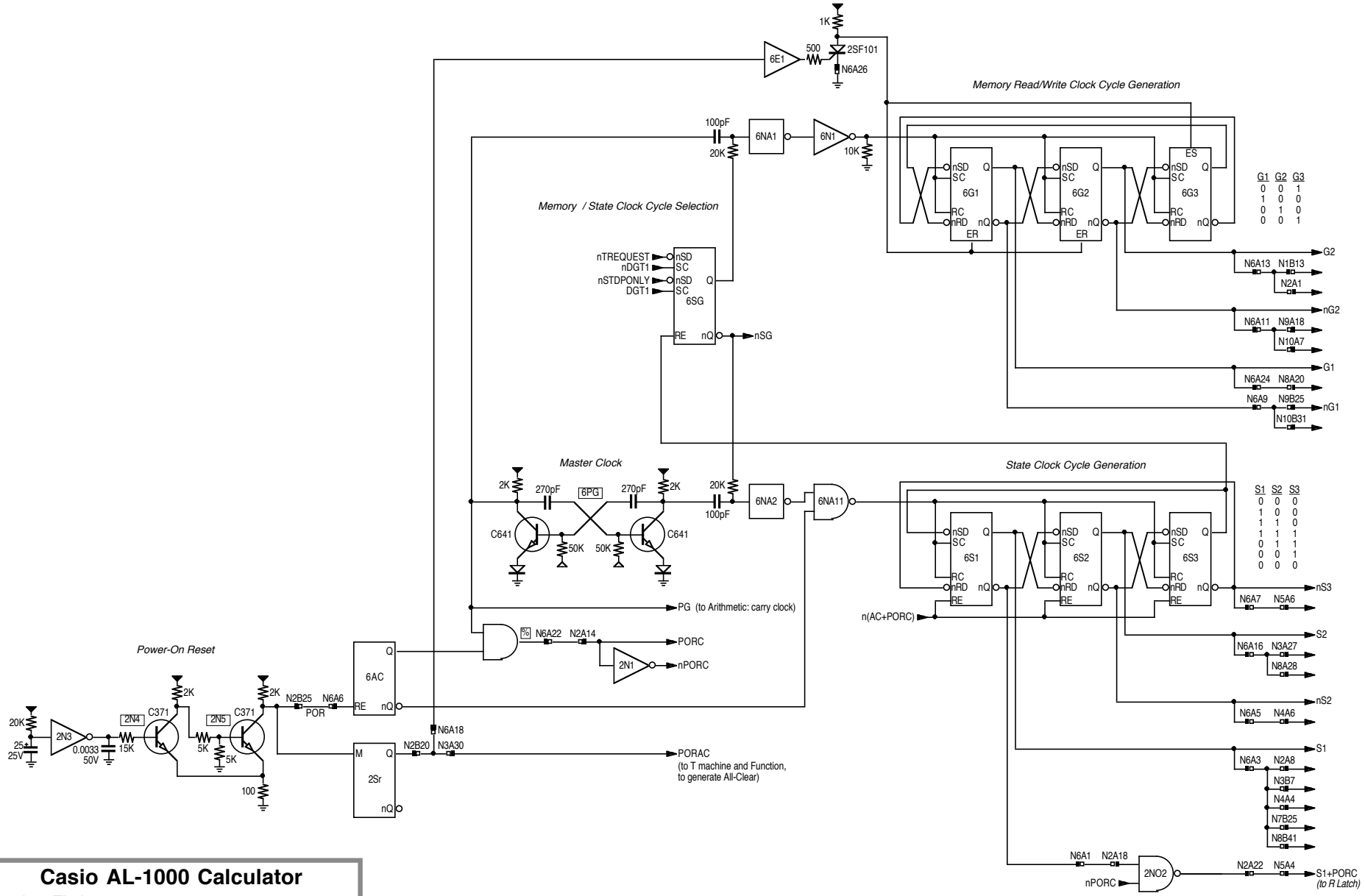
Basic Core Memory Timing and the Display Cycle



State Transition Timing



• PG measured as 66 KHz.



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Section: Timing

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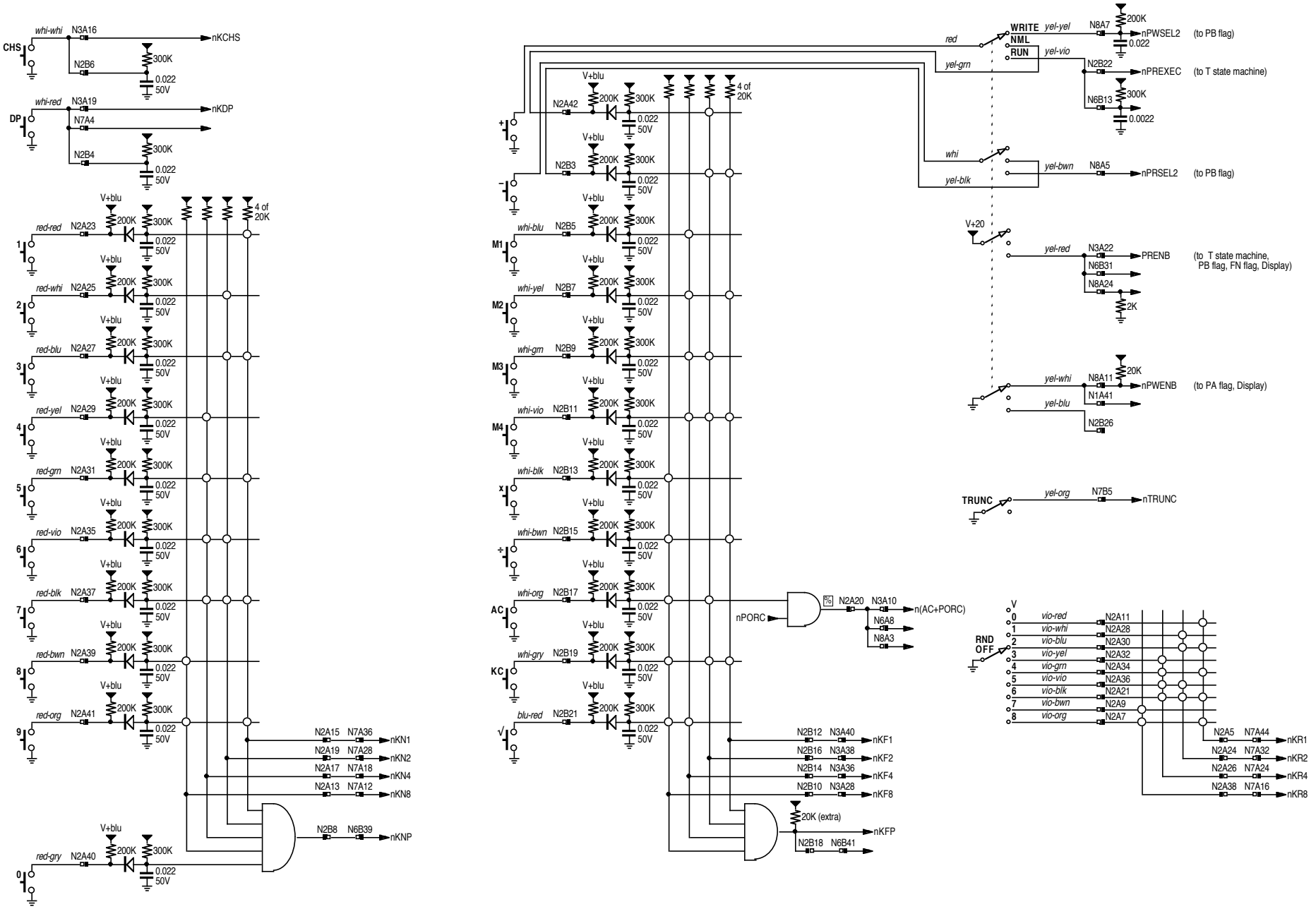

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Section: Keyboard

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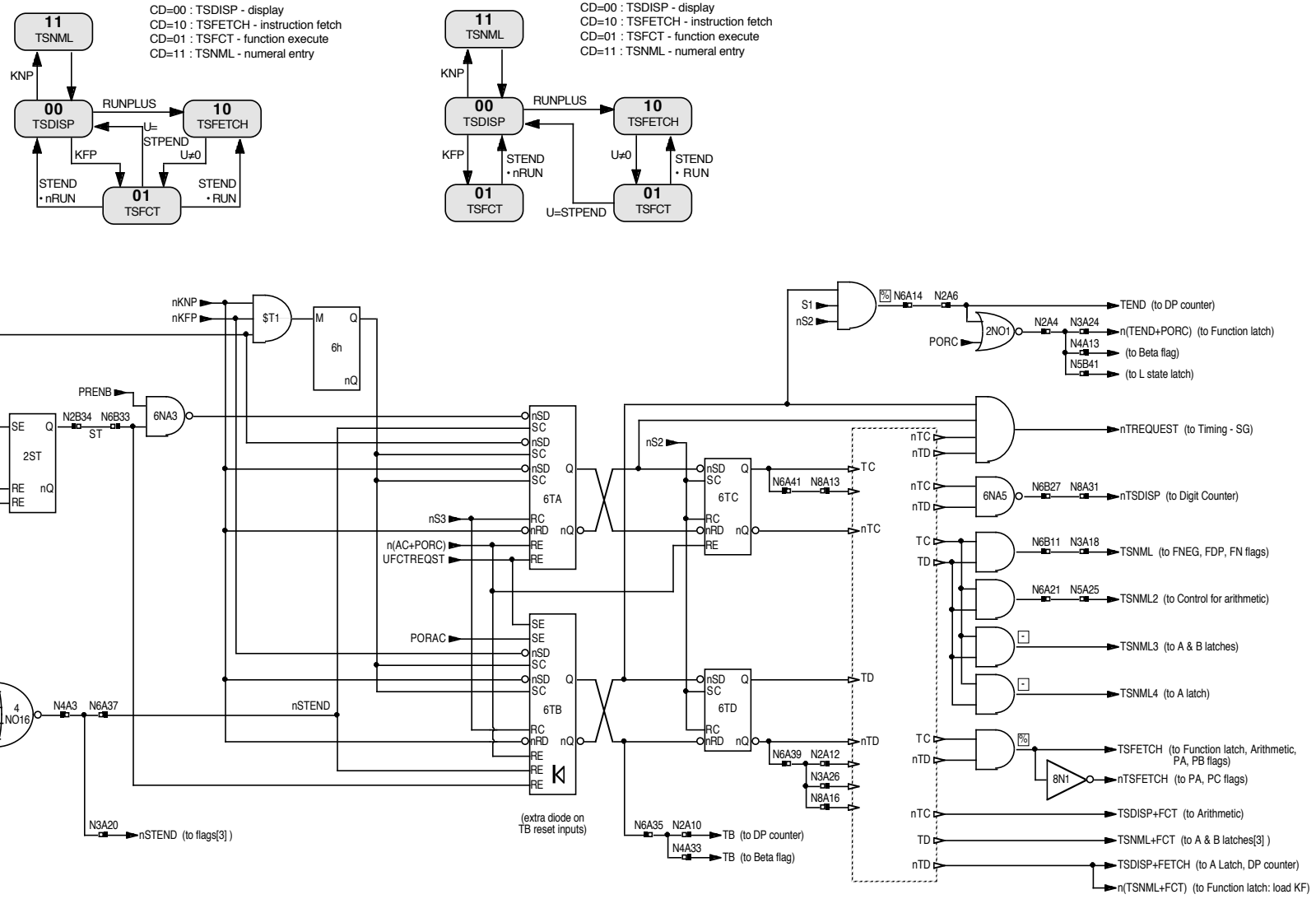
○ =



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Section: Control - T State

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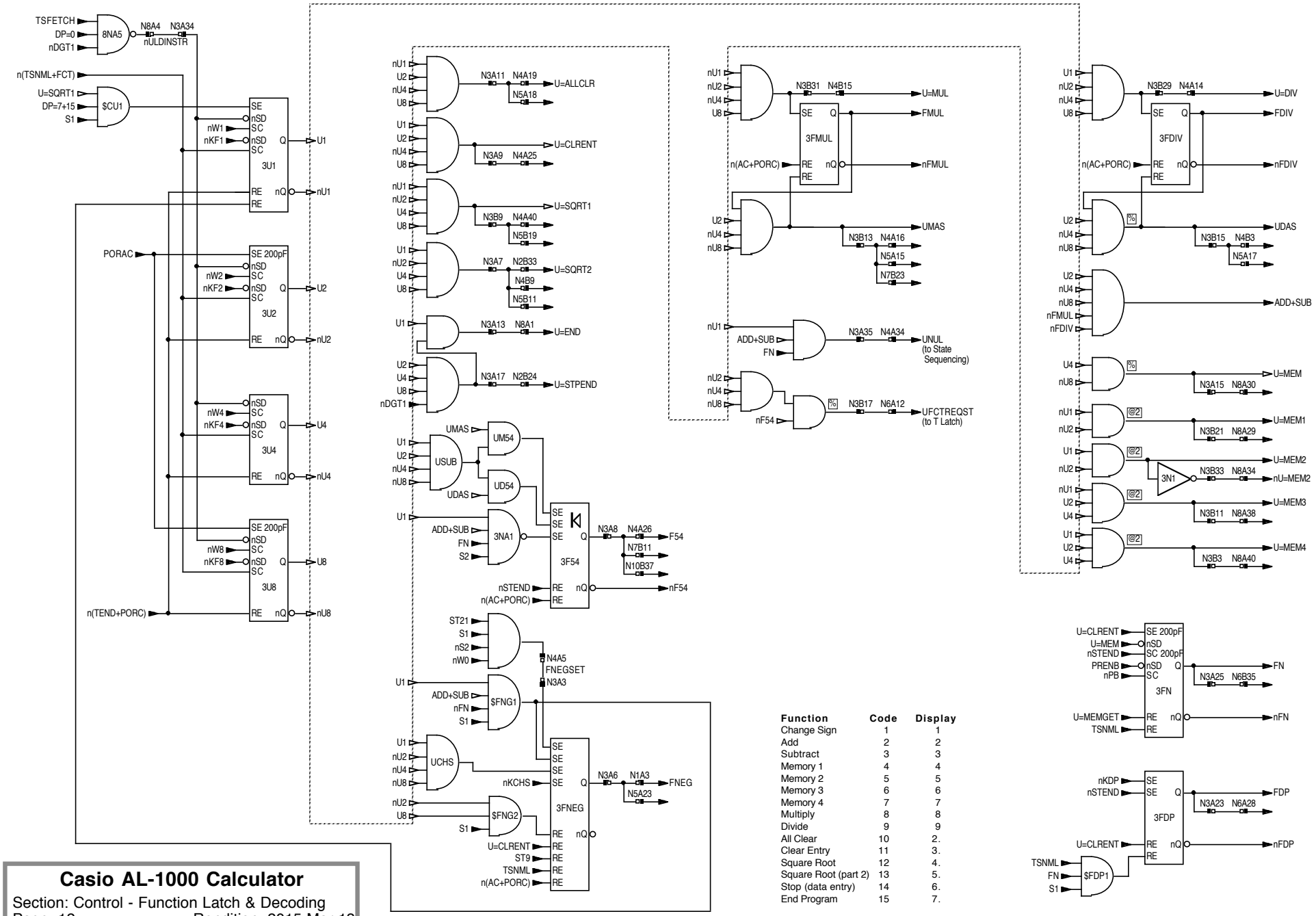
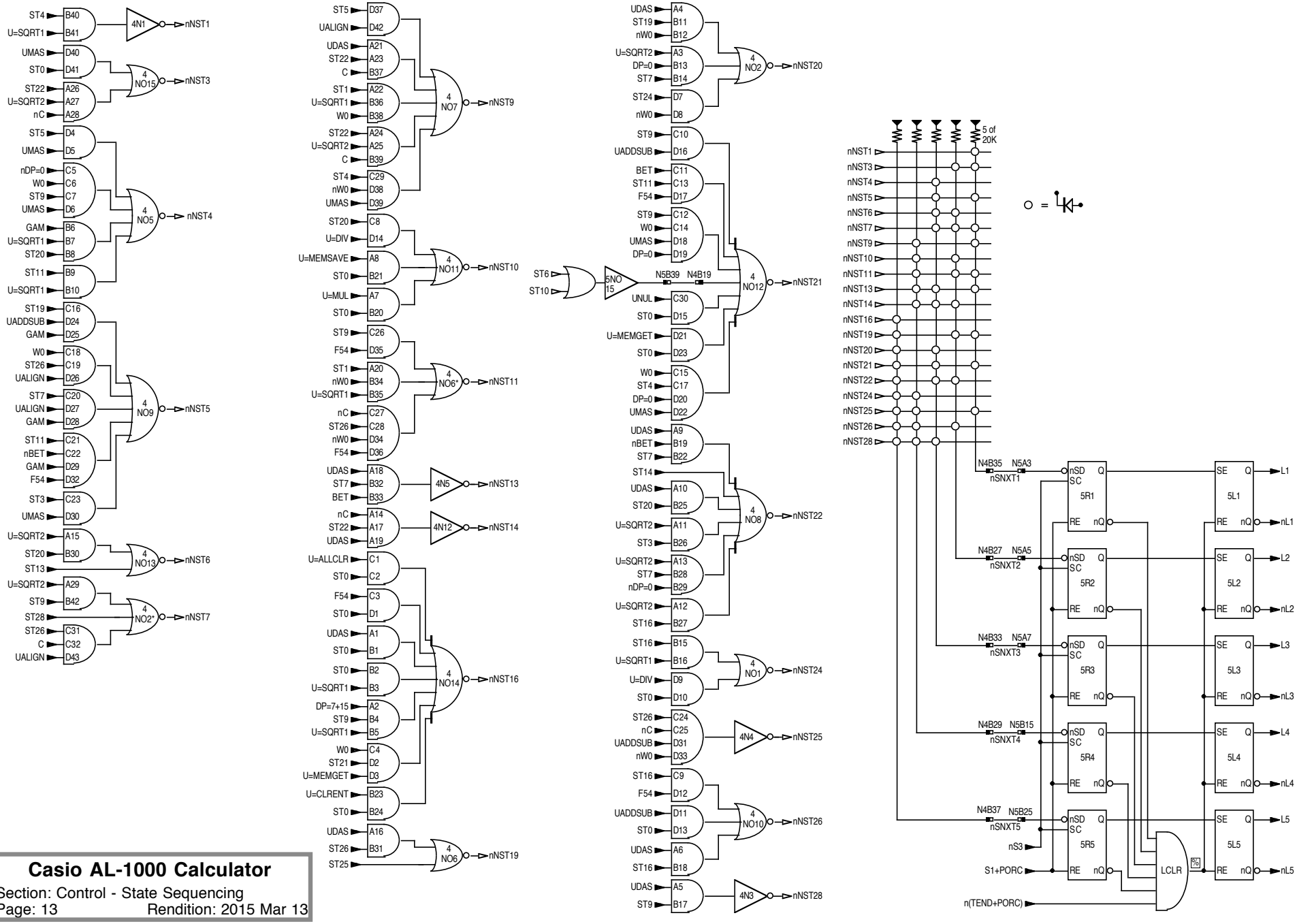


Function	Code	Display
Change Sign	1	1
Add	2	2
Subtract	3	3
Memory 1	4	4
Memory 2	5	5
Memory 3	6	6
Memory 4	7	7
Multiply	8	8
Divide	9	9
All Clear	10	2.
Clear Entry	11	3.
Square Root	12	4.
Square Root (part 2)	13	5.
Stop (data entry)	14	6.
End Program	15	7.



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Section: Control - State Sequencing
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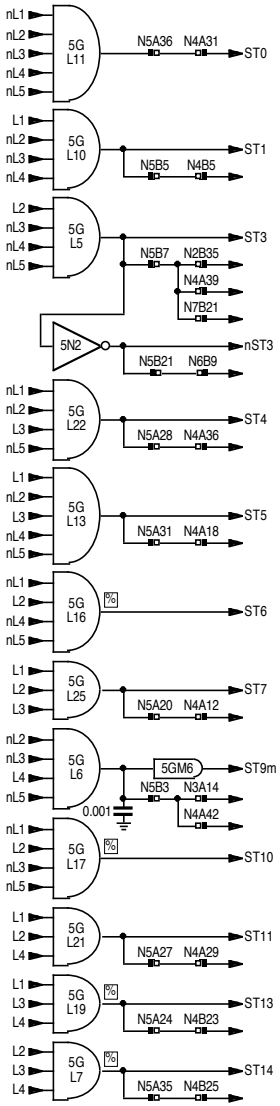
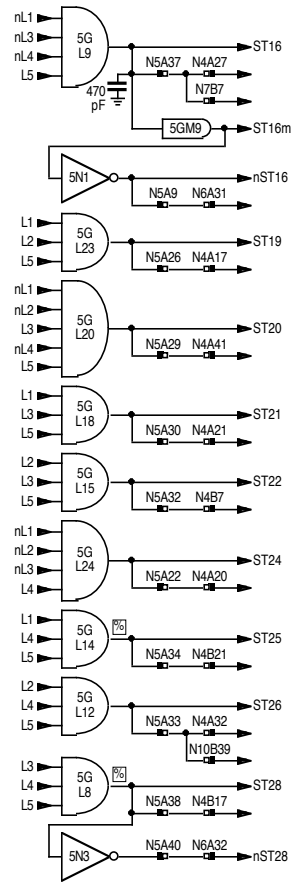
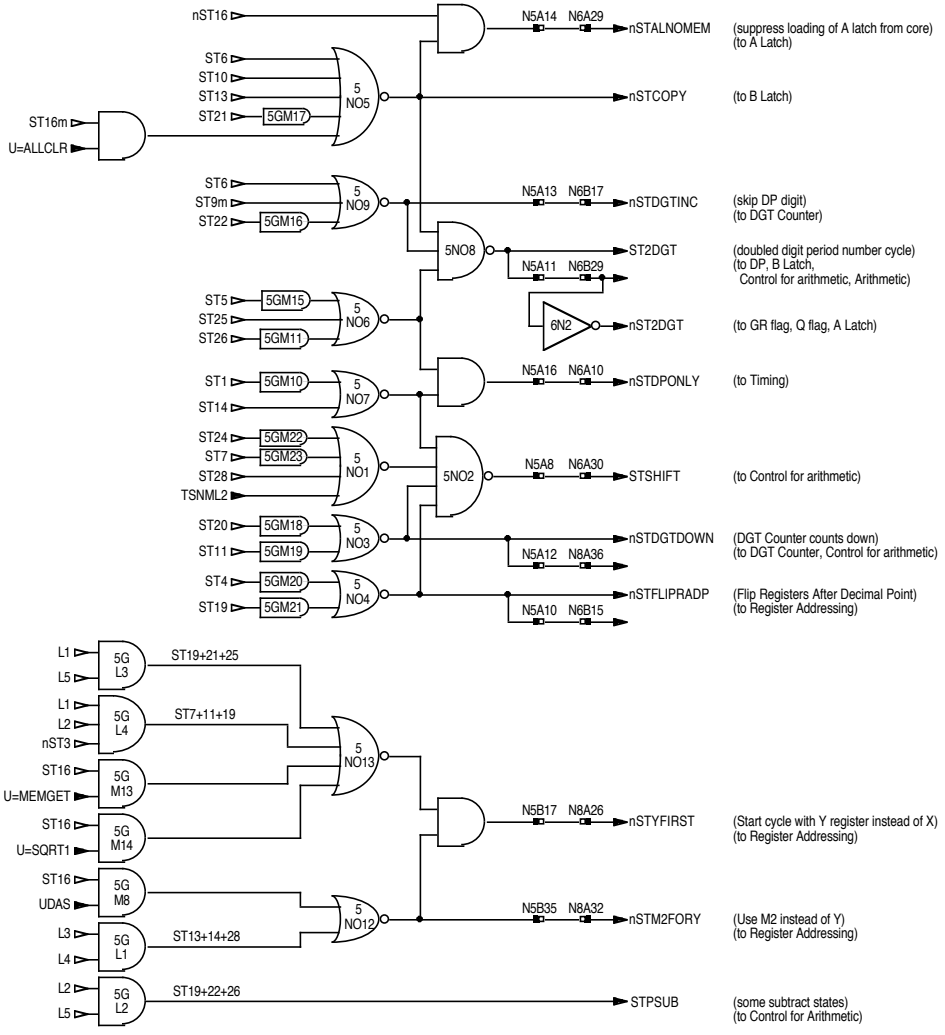






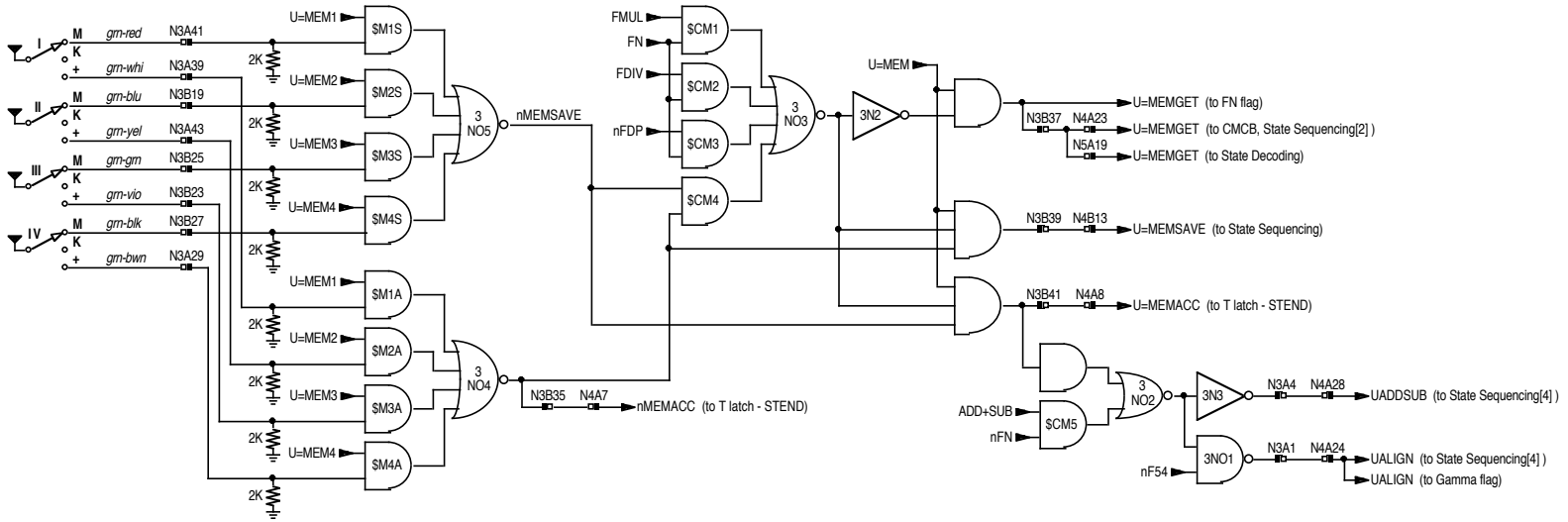
Other State Destinations

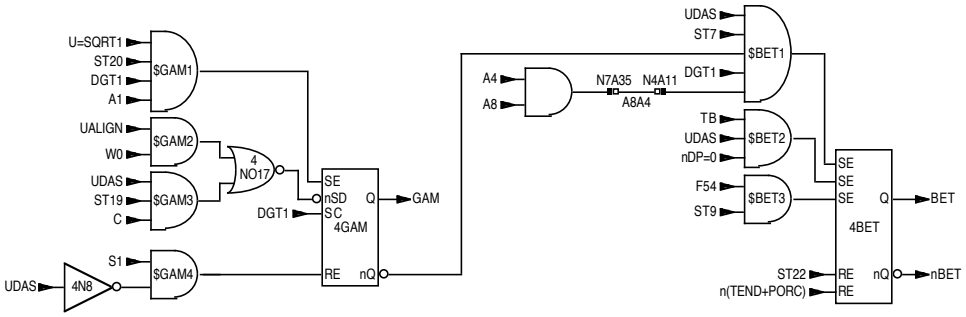
ST3 (to DP Counter)	ST19 (to GAM)
ST3 (to Arithmetic[2])	
nST3 (to A,B Latch)	ST20 (to GAM)
ST4 (to DP Counter)	ST21 (to STEND,FNEG)
ST7 (to BET)	
ST7 (to DP Counter)	ST22 (to BET)
ST9 (to DP Counter)	ST26 (to B Latch)
ST9 (to BET)	
ST9 (to STEND,FNEG)	nST28 (to Control for Arithmetic)
nST16 (to B Latch)	
ST16 (to Arithmetic)	
ST16 (to STEND)	

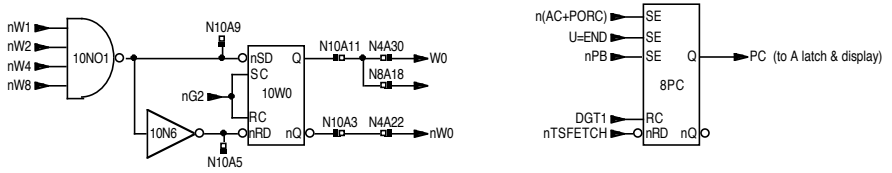
Resistor on 5GL5 and U=MEMGET (fed by 3N2) is 20K, consistency with others would suggest it should be 10K.

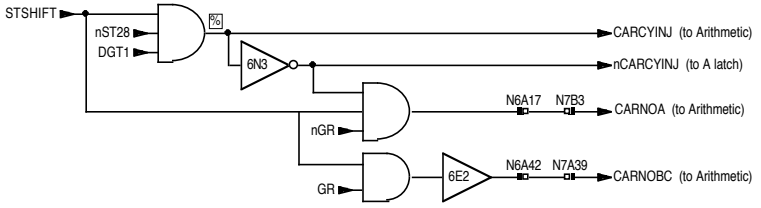
Casio AL-1000 Calculator

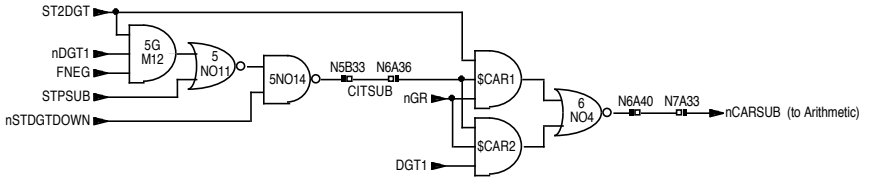
Section: Control - State Decoding











Casio AL-1000 Calculator

Section: Control - Miscellaneous

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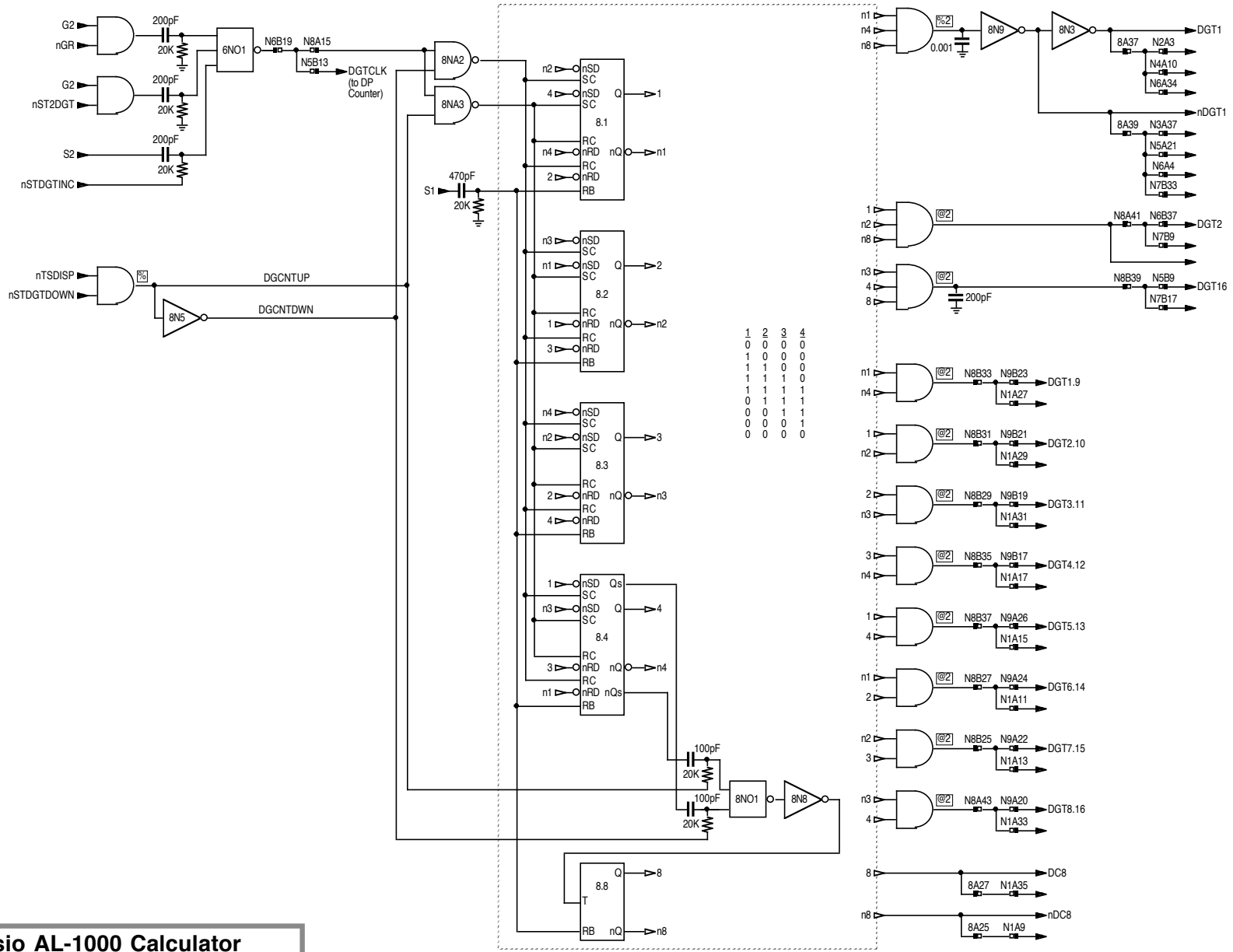

Casio AL-1000 Calculator

Section: Digit Counter

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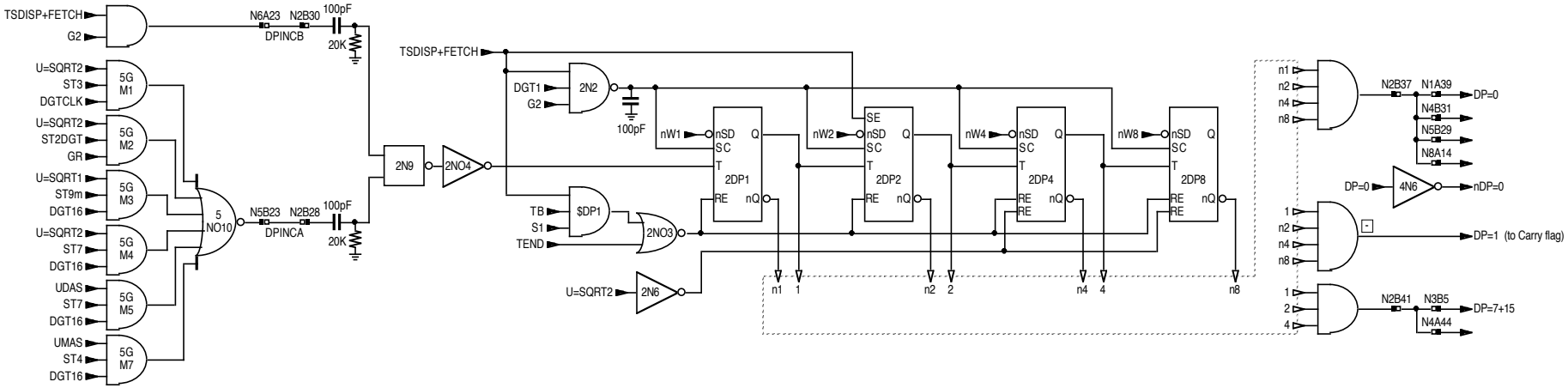

Casio AL-1000 Calculator

Section: Decimal Point

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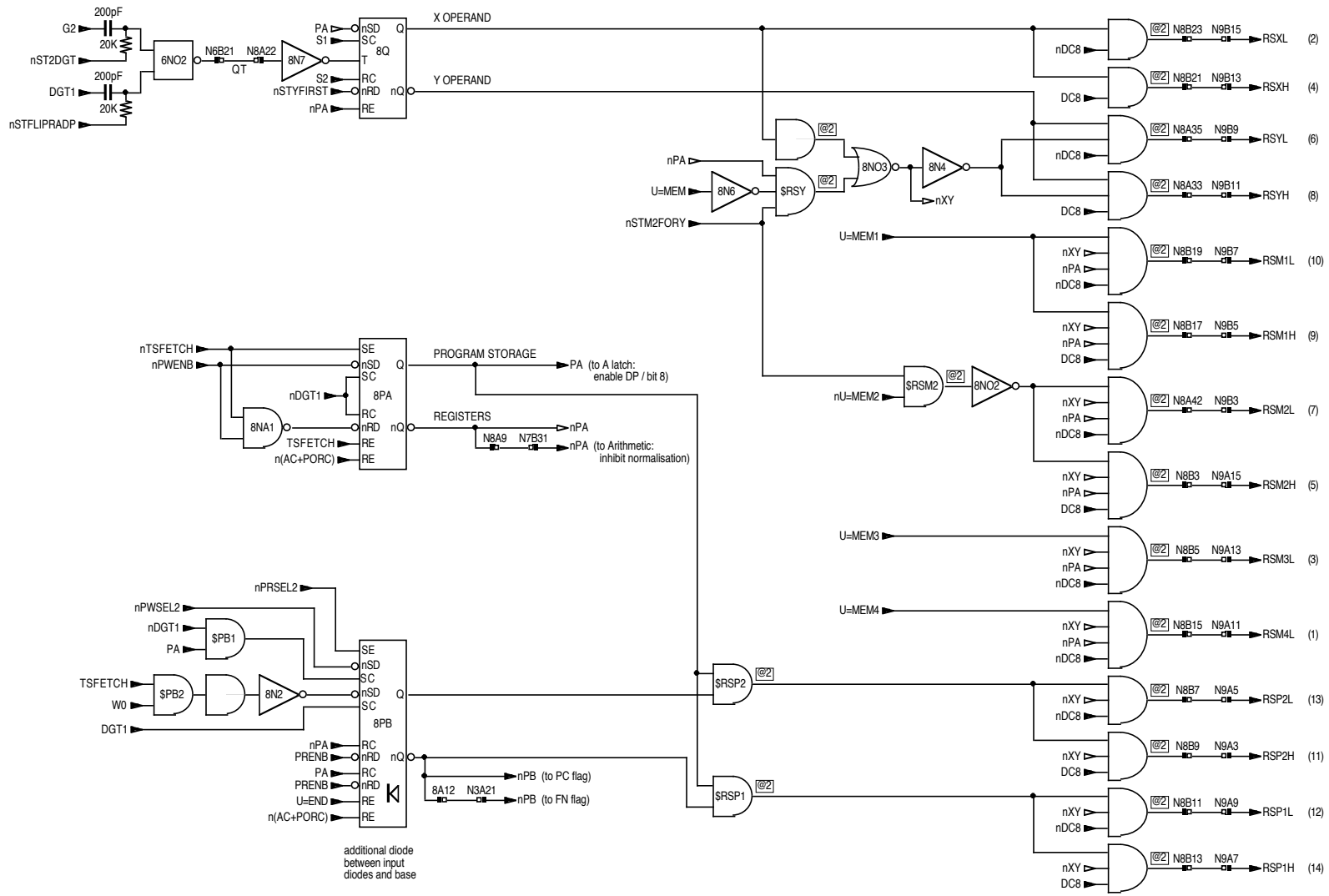

Casio AL-1000 Calculator

Section: Register Selection

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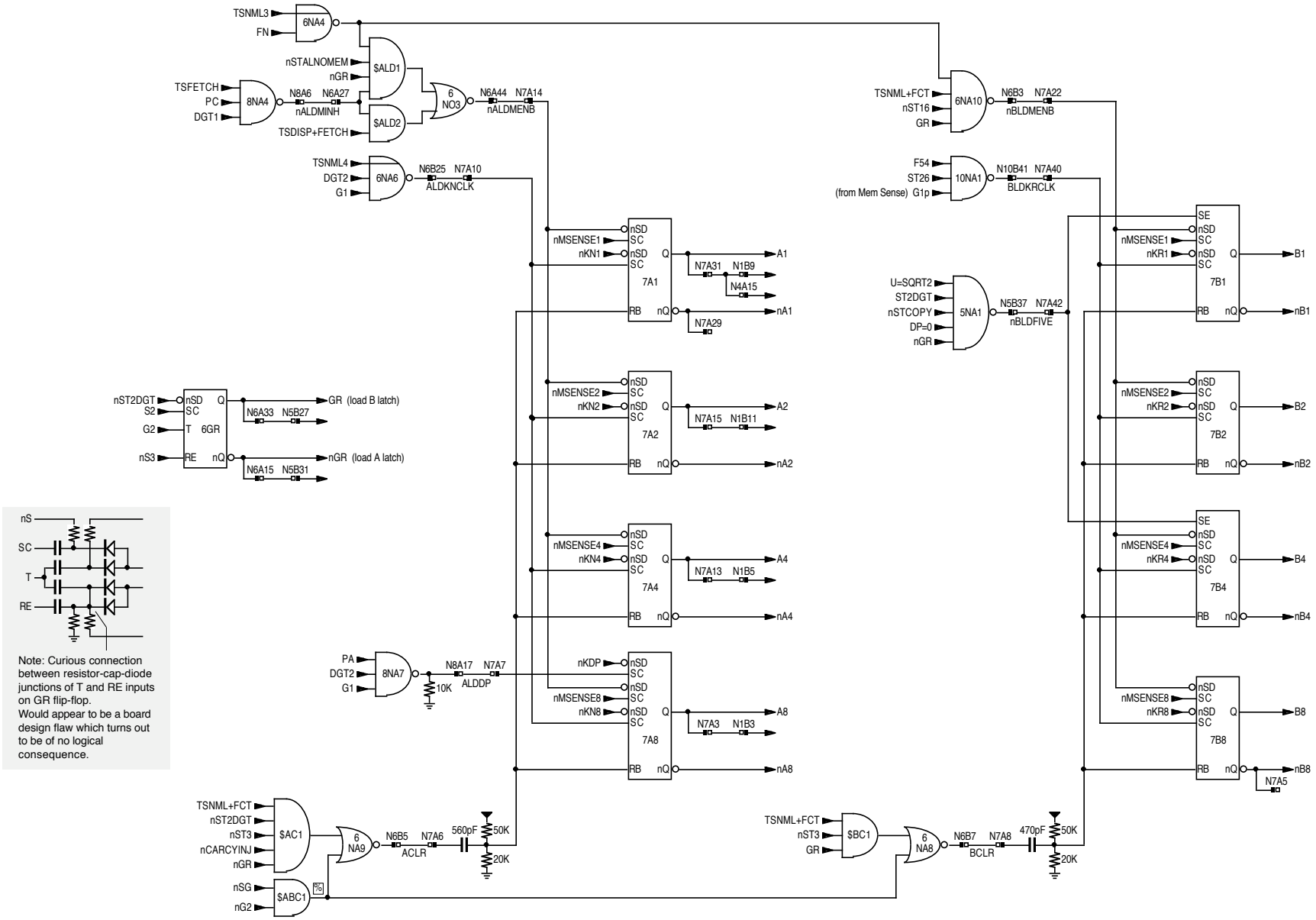

Casio AL-1000 Calculator

Section: A & B Latches

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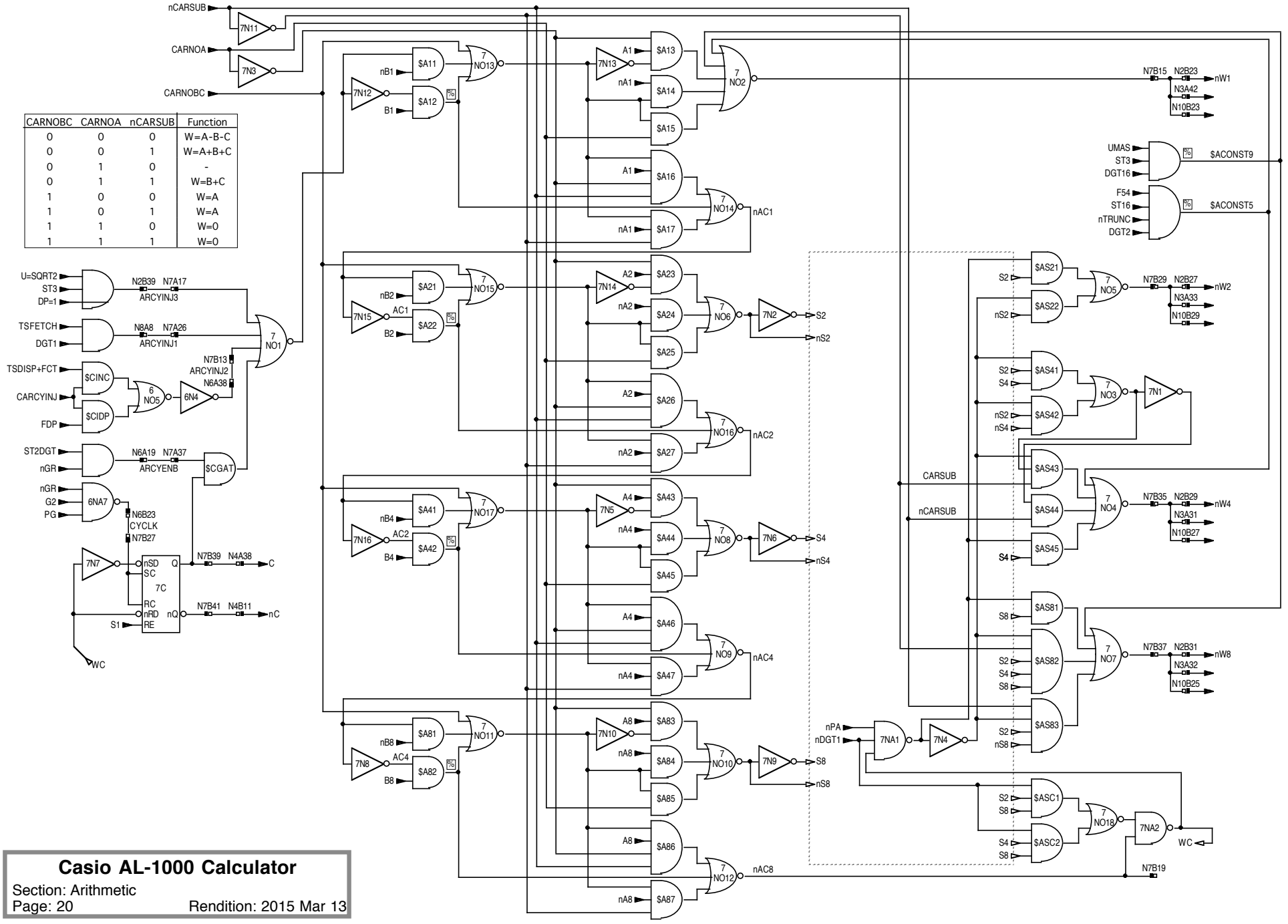

CARNOBC	CARNOA	nCARSUB	Function
0	0	0	W=A-B-C
0	0	1	W=A+B+C
0	1	0	-
0	1	1	W=B+C
1	0	0	W=A
1	0	1	W=A
1	1	0	W=0
1	1	1	W=0

Casio AL-1000 Calculator

Section: Arithmetic

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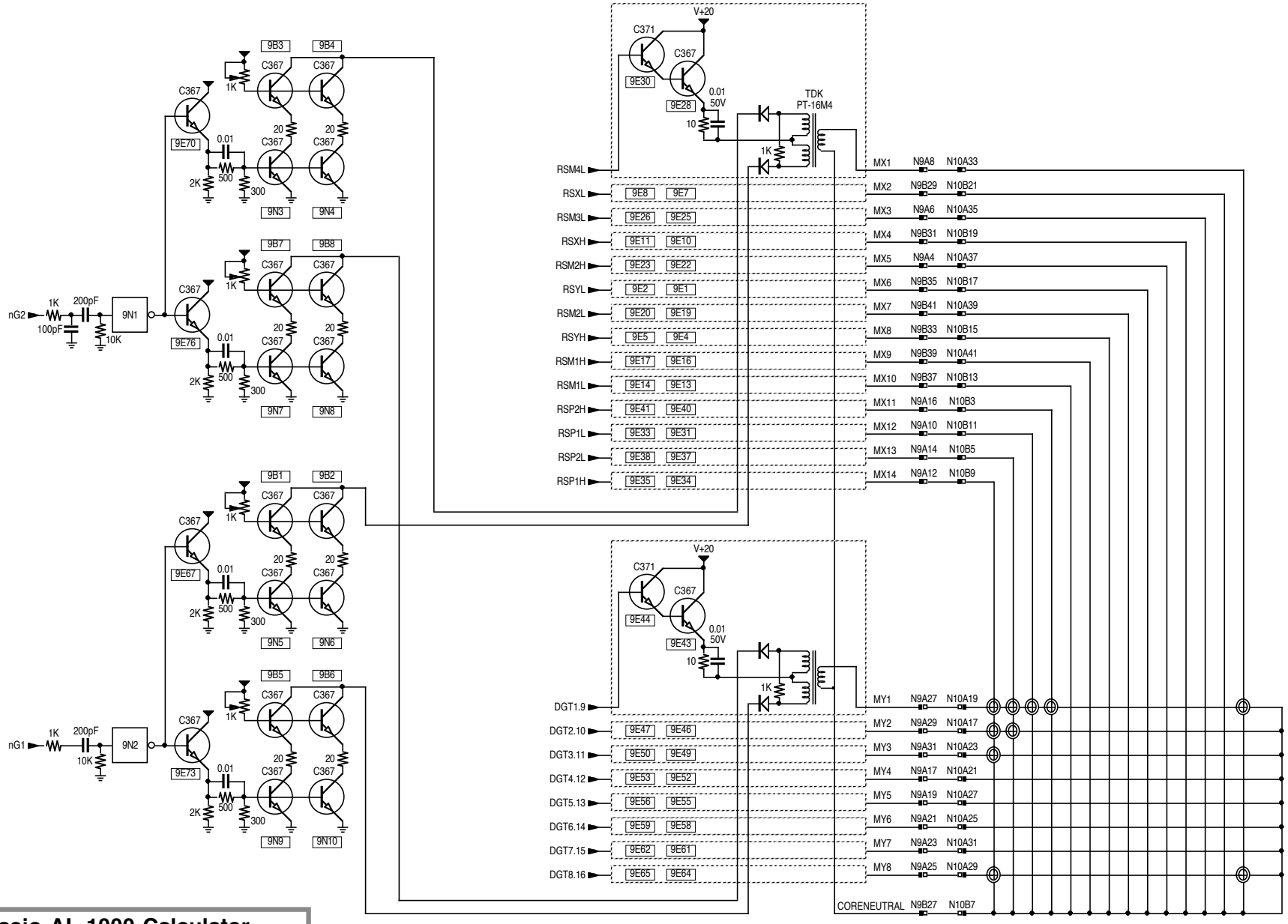

Address lines flow through all 4 core planes (only one shown).

Casio AL-1000 Calculator

Section: Memory Address Drivers

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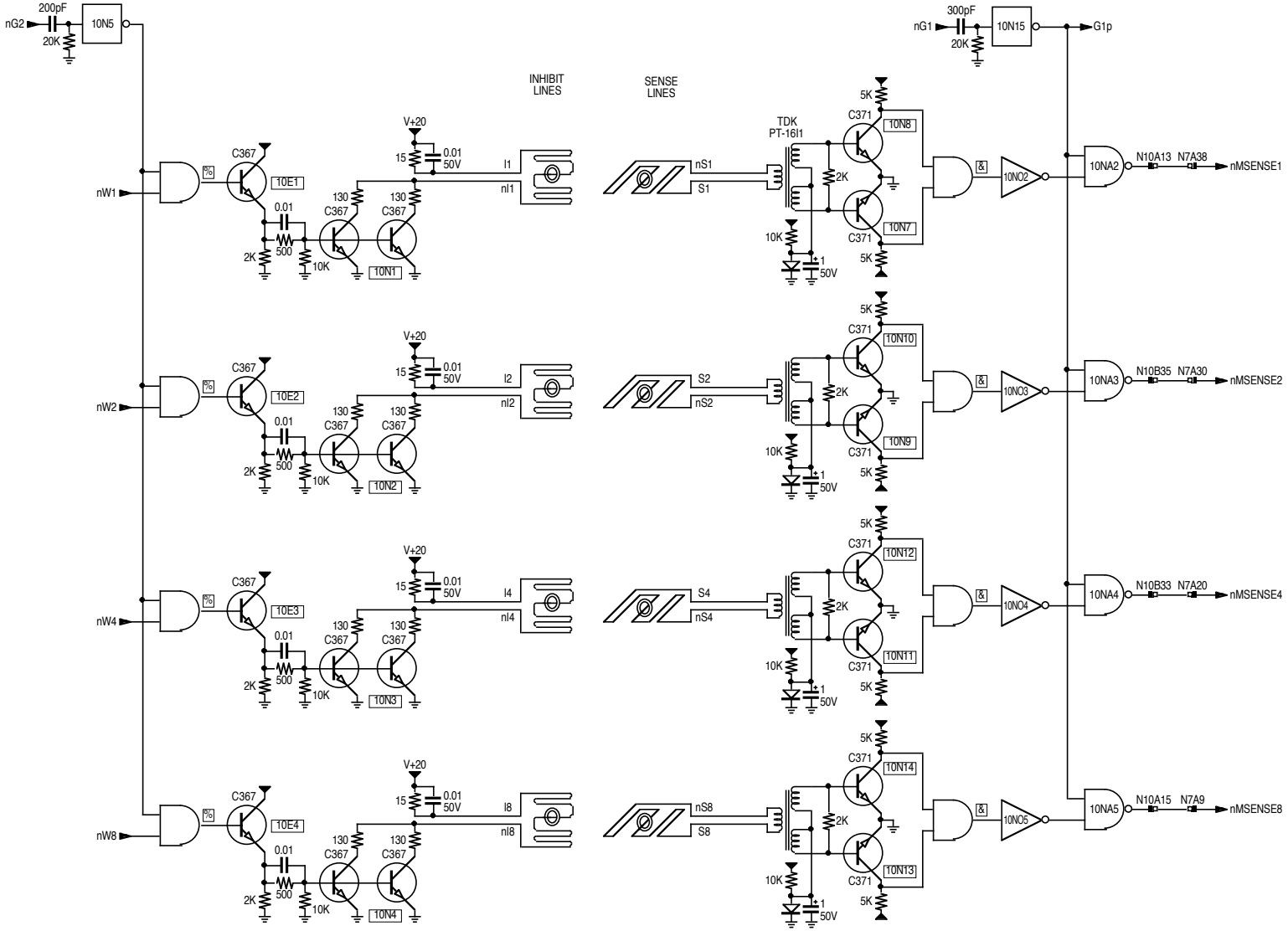

Casio AL-1000 Calculator

Section: Memory Inhibit & Sense

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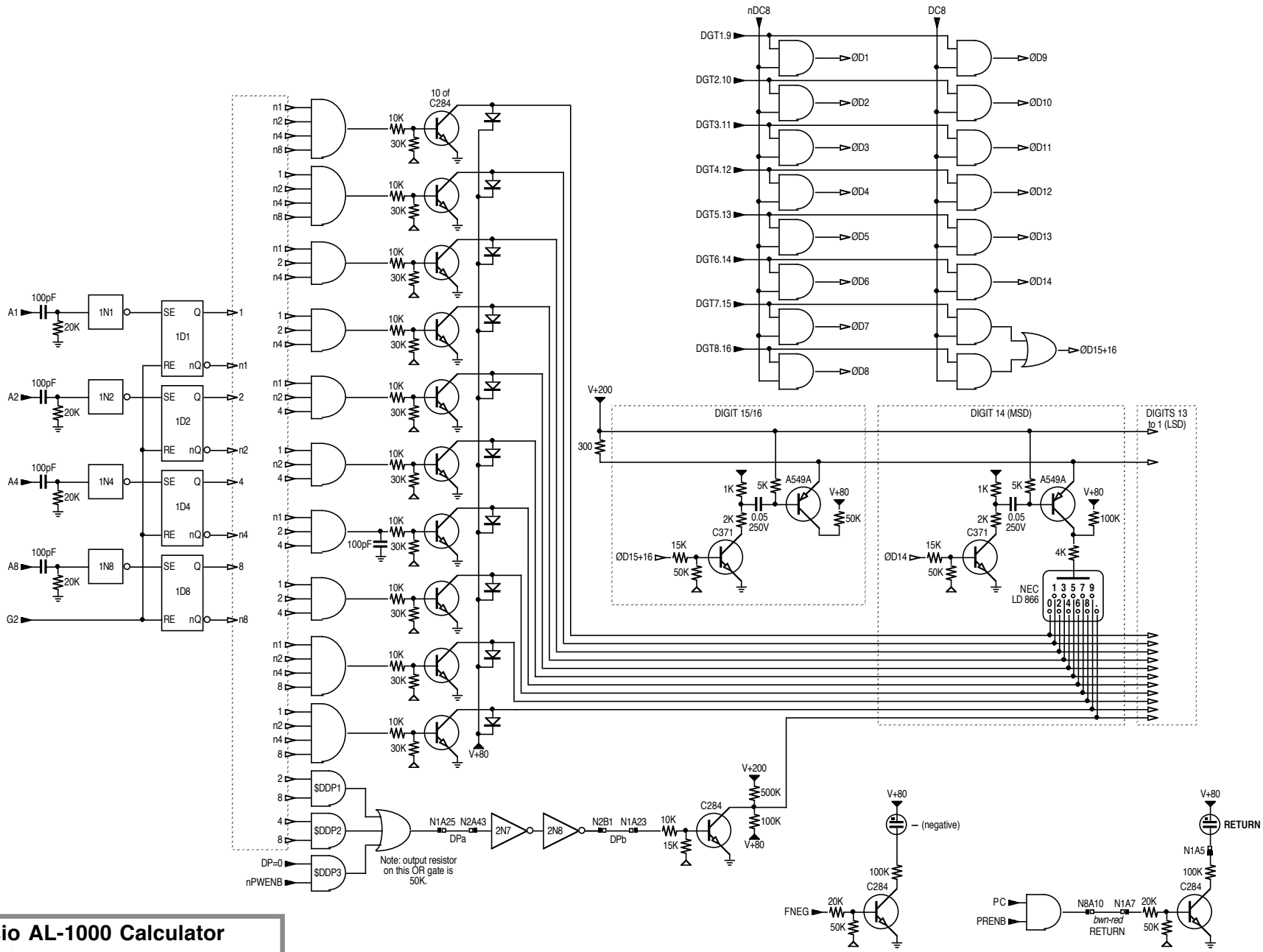

Casio AL-1000 Calculator

Section: Display

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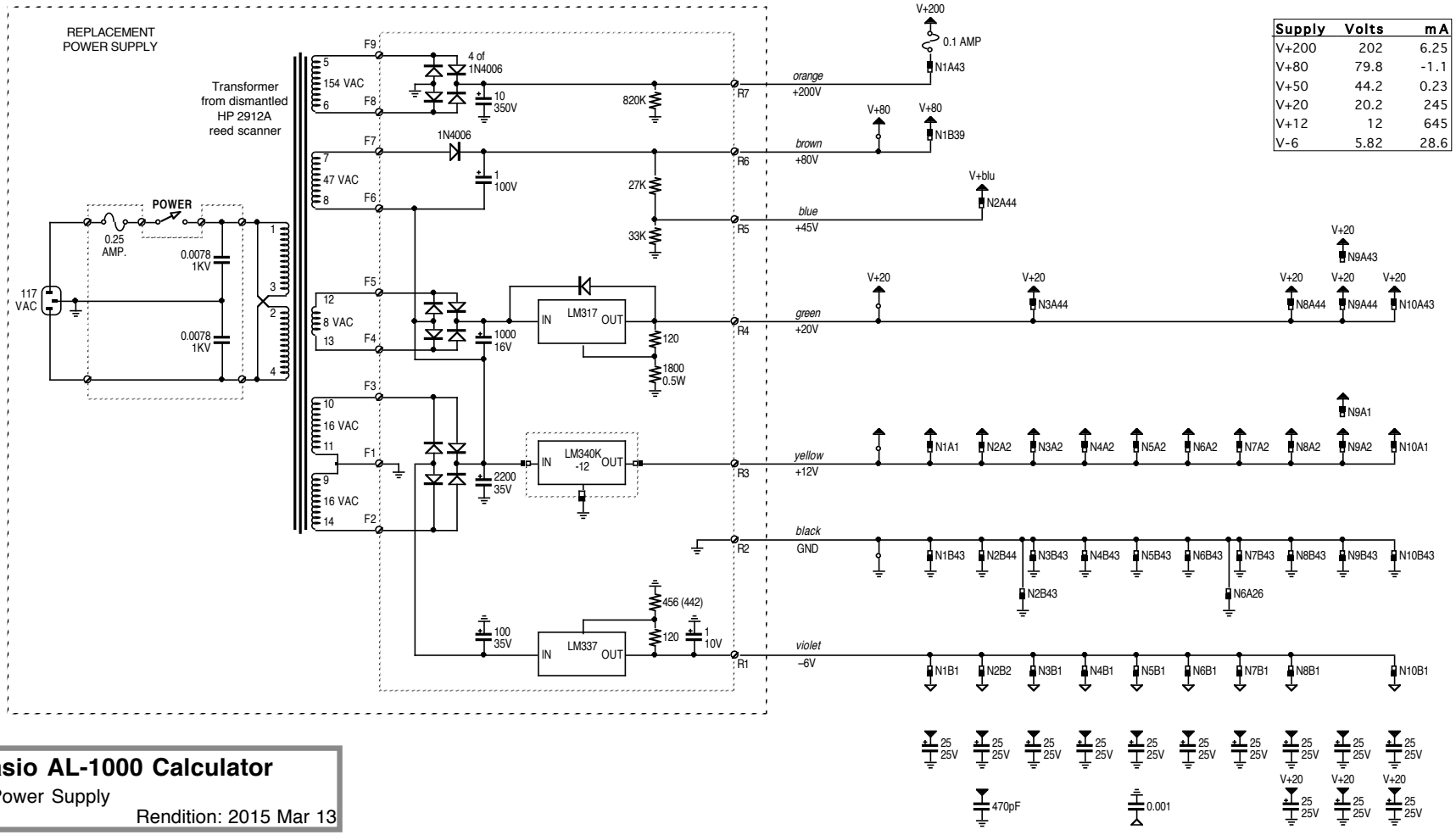
	V	Rt	Rb	I	P(Rb)
-6 Reg calc	6	120	456	0.010	0.049
-20 Reg calc	20	121	1815	0.010	0.194
-6 Reg calc	5.81612	121	442	0.010	0.047
-20 Reg calc	19.9483	121	1810	0.010	0.193
	8.11983	121	665	0.010	0.071
-6 Reg calc	5.96891	121	592	0.008	0.041
			2000		
-20 Reg calc	19.6901	121	3570	0.005	0.102
			3570		

	V	I	R	P
+200 use	202	0.00625		1.26
+20 use	20.2	0.245		4.95
+12 use	12	0.645		7.74
-6 use	5.8	0.0286		0.17
+20 power reg	4.8	0.245		1.18
+12 power reg	4	0.645		2.58
-6 power reg	10.2	0.0286		0.29
				18.17
+200V bleed	200	0.0002	820000	0.05
+80 divider	80.0			
	36.0	0.0013	27000	0.05
	44.0	0.0013	33000	0.06
+200V divider	200.0			
	114.3	0.006	20000	0.65
	42.9	0.006	7500	0.24
	42.9	0.006	7500	0.24



Supply	Volts	mA
V+200	202	6.25
V+80	79.8	-1.1
V+50	44.2	0.23
V+20	20.2	245
V+12	12	645
V-6	5.82	28.6

Casio AL-1000 Calculator

Section: Power Supply

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N1A

1	V+12
3	FNEG
5	RETLAMP
7	RETURN
9	nMB8
11	MDY6
13	MDY7
15	MDY5
17	MDY4
19	-
21	-
23	DPb
25	**DPa**
27	MDY1
29	MDY2
31	MDY3
33	MDY8
35	MB8
37	-
39	DP=0
41	nPWENB
43	V+200

N2A

G2	1	2	V+12
DGT1	3	4	**n(TEND+PORC)**
nKR1	5	6	TEND
nRND8	7	8	S1
nRND7	9	10	TB
nRND0	11	12	nTD
nKN8	13	14	PORC
nKN1	15	16	-
nKN4	17	18	nS1
nKN2	19	20	**n(AC+PORC)**
nRND6	21	22	**S1+PORC**
nK1	23	24	**nKR2**
nK2	25	26	**nKR4**
nK3	27	28	nRND1
nK4	29	30	nRND2
nK5	31	32	nRND3
-	33	34	nRND4
nK6	35	36	nRND5
nK7	37	38	**nKR8**
nK8	39	40	nK0
nK9	41	42	nKADD
DPa	43	44	V+blu

N3A

UALIGN	1	2	V+12
FNEGSET	3	4	**UADDSUB**
-	5	6	**FNEG**
U=13	7	8	**F54**
U=CLRENT	9	10	n(AC+PORC)
U=ALLCLR	11	12	-
U=END	13	14	ST9
U=MEM	15	16	nKCHS
U=STPEND	17	18	TSNML
nKDP	19	20	nSTEND
nPB	21	22	PRENB
FDP	23	24	n(TEND+PORC)
FN	25	26	nTD
S2	27	28	nKF8
M4ACC	29	30	PORAC
nW4	31	32	nW8
nW2	33	34	**nULDINSTR**
UNUL	35	36	nKF4
nDGT1	37	38	nKF2
M1ACC	39	40	nKF1
M1MEM	41	42	nW1
M2ACC	43	44	V+20

N4A

-	1	2	V+12
nSTEND	3	4	S1
FNEGSET	5	6	nS2
nMEMACC	7	8	U=MEMACC
-	9	10	DGT1
A8A4	11	12	ST7
n(TEND+PORC)	13	14	U=DIV
A1	15	16	UMAS
ST19	17	18	ST5
U=ALLCLR	19	20	ST24
ST21	21	22	nW0
U=MEMGET	23	24	UALIGN
U=CLRENT	25	26	F54
ST16	27	28	UADDSUB
ST11	29	30	W0
ST0	31	32	ST26
TB	33	34	UNUL
-	35	36	ST4
-	37	38	C
ST3	39	40	U=SQRRT
ST20	41	42	ST9
-	43	44	DP=7+15

N5A

-	1	2	V+12
nSNXT1	3	4	S1+PORC
nSNXT2	5	6	nS3
nSNXT3	7	8	**STSHIFT**
nST16	9	10	**nSTFLIPRADP**
ST2DGT	11	12	**nSTDGTDOWN**
nSTDGTINC	13	14	**nSTALNOMEM**
UMAS	15	16	**nSTDPONLY**
UDAS	17	18	U=ALLCLR
U=MEMGET	19	20	**ST7**
nDGT1	21	22	**ST24**
FNEG	23	24	**ST13**
TSNML2	25	26	**ST19**
ST11	27	28	**ST4**
ST20	29	30	**ST21**
ST5	31	32	**ST22**
ST26	33	34	**ST25**
ST14	35	36	**ST0**
ST16	37	38	**ST28**
-	39	40	**nST28**
-	41	42	-
-	43	44	-

N1B

1	V–6
3	A8
5	A4
7	-
9	A1
11	A2
13	G2
15	-
17	-
19	-
21	-
23	-
25	-
27	-
29	-
31	-
33	-
35	-
37	-
39	V+80
41	-
43	GND

N2B

DPb	1	2	V–6
nKSUB	3	4	nKDP
nKM1	5	6	nKCHS
nKM2	7	8	**nKNP**
nKM3	9	10	**nKF8**
nKM4	11	12	**nKF1**
nKMUL	13	14	**nKF4**
nKDIV	15	16	**nKF2**
nKAC	17	18	**nKFP**
nKKC	19	20	**PORAC**
nKSQR	21	22	nPREXEC
nW1	23	24	U=STPEND
POR	25	26	nPRENB (not used)
nW2	27	28	DPINCA
nW4	29	30	DPINCB
nW8	31	32	-
U=13	33	34	**ST**
ST3	35	36	-
DP=0	37	38	-
ARCYINJ3	39	40	-
DP=7+15	41	42	-
GND	43	44	GND

N3B

1	V–6
3	**U=MEM4**
5	DP=7+15
7	S1
9	**U=SQRRT**
11	**U=MEM3**
13	**UMAS**
15	**UDAS**
17	**UFCTREQST**
19	M2MEM
21	**U=MEM1**
23	M3ACC
25	M3MEM
27	M4MEM
29	**U=DIV**
31	**U=MUL**
33	**nU=MEM2**
35	**nMEMACC**
37	**U=MEMGET**
39	**U=MEMSAVE**
41	**U=MEMACC**
43	GND

N4B

1	V–6
3	UDAS
5	ST1
7	ST22
9	U=13
11	nC
13	U=MEMSAVE
15	U=MUL
17	ST28
19	ST6+10
21	ST25
23	ST13
25	ST14
27	**nSNXT2**
29	**nSNXT4**
31	DP=0
33	**nSNXT3**
35	**nSNXT1**
37	**nSNXT5**
39	-
41	-
43	GND

N5B

1	V–6
3	**ST9**
5	**ST1**
7	**ST3**
9	DGT16
11	U=13
13	DGTCLK
15	nSNXT4
17	**nSTYFIRST**
19	U=SQRRT
21	**nST3**
23	**DPINCA**
25	nSNXT5
27	GR
29	DP=0
31	nGR
33	**CITSUB**
35	**nSTM2FORY**
37	**nBLDFIVE**
39	**ST6+10**
41	n(TEND+PORC)
43	GND

Casio AL-1000 Calculator

Section: Connectors 1-5
Page: 25 Rendition: 2015 Mar 13

Note: Bold-faced expressions are signal source.

N6A

nS1	1	2	V+12
S1	3	4	nDGT1
nS2	5	6	POR
nS3	7	8	n(AC+PORC)
nG1	9	10	nSTDPONLY
nG2	11	12	UFCTREQST
G2	13	14	**TEND**
nGR	15	16	**S2**
CARNOA	17	18	PORAC
ARCYENB	19	20	-
TSNML2	21	22	**PORC**
DPINCB	23	24	**G1**
-	25	26	GND
nALDMINH	27	28	FDP
nSTALNOMEM	29	30	STSHIFT
nST16	31	32	nST28
GR	33	34	DGT1
TB	35	36	CITSUB
nSTEND	37	38	**ARCYINJ2**
nTD	39	40	**nCARSUB**
TC	41	42	**CARNOBC**
-	43	44	**nALDMENB**

N7A

-	1	2	V+12
A8	3	4	nKDP
(nB8) -	5	6	ACLR
ALDDP	7	8	BCLR
nMSENSE8	9	10	ALDKNCLK
-	11	12	nKN8
A4	13	14	nALDMENB
A2	15	16	nKR8
ARCYINJ3	17	18	nKN4
-	19	20	nMSENSE4
-	21	22	nBLDMENB
-	23	24	nKR4
-	25	26	ARCYINJ1
-	27	28	nKN2
(nA1) -	29	30	nMSENSE2
A1	31	32	nKR2
nCARSUB	33	34	-
A8A4	35	36	nKN1
ARCYENB	37	38	nMSENSE1
CARNOBC	39	40	BLDKRCLK
-	41	42	nBLDFIVE
-	43	44	nKR1

N8A

U=END	1	2	V+12
n(AC+PORC)	3	4	nULDINSTR
nPRSEL2	5	6	**nALDMINH**
nPWSEL2	7	8	**ARCYINJ1**
nPA	9	10	**RETLAMP**
nPWENB	11	12	**nPB**
TC	13	14	DP=0
DGTCLK	15	16	nTD
ALDDP	17	18	W0
-	19	20	G1
-	21	22	QT
-	23	24	PRENB
nMB8	25	26	nSTYFIRST
MB8	27	28	S2
U=MEM1	29	30	U=MEM
nTSIDLE	31	32	nSTM2FORY
RSYH	33	34	nU=MEM2
RSYL	35	36	nSTDGTDOWN
DGT1	37	38	U=MEM3
nDGT1	39	40	U=MEM4
DGT2	41	42	**RSM2L**
DGT8.16	43	44	V+20

N9A

(V+12)	1	2	V+12
RSP2H	3	4	**MX5**
RSP2L	5	6	**MX3**
RSP1H	7	8	**MX1**
RSP1L	9	10	**MX12**
RSM4L	11	12	**MX14**
RSM3L	13	14	**MX13**
RSM2H	15	16	**MX11**
MY4	17	18	nG2
MY5	19	20	DGT8.16
MY6	21	22	DGT7.15
MY7	23	24	DGT6.14
MY8	25	26	DGT5.13
MY1	27	28	-
MY2	29	30	-
MY3	31	32	-
-	33	34	-
-	35	36	-
-	37	38	-
-	39	40	-
-	41	42	-
(V+20)	43	44	V+20

N10A

1		V+12
3		**nW0**
5		-
7		nG2
9		-
11		**W0**
13		**nMSENSE1**
15		**nMSENSE8**
17		MY2
19		MY1
21		MY4
23		MY3
25		MY6
27		MY5
29		MY8
31		MY7
33		MX1
35		MX3
37		MX5
39		MX7
41		MX9
43		V+20

N6B

1	V–6
3	**nBLDMENB**
5	**ACLR**
7	**BCLR**
9	nST3
11	**TSNML**
13	nPREXEC
15	nSTFLIPRADP
17	nSTDGTINC
19	**DGTCLK**
21	**QT**
23	**CYCLK**
25	**ALDKNCLK**
27	**nTSIDLE**
29	ST2DGT
31	PRENB
33	ST
35	FN
37	DGT2
39	nKNP
41	nKFP
43	GND

N7B

1	V–6
3	CARNOA
5	nTRUNC
7	ST16
9	DGT2
11	F54
13	ARCYINJ2
15	**nW1**
17	DGT16
19	- (pre-norm carry)
21	ST3
23	UMAS
25	S1
27	CYCLK
29	**nW2**
31	nPA
33	nDGT1
35	**nW4**
37	**nW8**
39	**C**
41	**nC**
43	GND

N8B

1	V–6
3	**RSM2H**
5	**RSM3L**
7	**RSP2L**
9	**RSP2H**
11	**RSP1L**
13	**RSP1H**
15	**RSM4L**
17	**RSM1H**
19	**RSM1L**
21	**RSXH**
23	**RSXL**
25	**DGT7.15**
27	**DGT6.14**
29	**DGT3.11**
31	**DGT2.10**
33	**DGT1.9**
35	**DGT4.12**
37	**DGT5.13**
39	**DGT16**
41	S1
43	GND

N9B

1	-
3	RSM2L
5	RSM1H
7	RSM1L
9	RSYL
11	RSYH
13	RSXH
15	RSXL
17	DGT4.12
19	DGT3.11
21	DGT2.10
23	DGT1.9
25	nG1
27	**CORENEUTRAL**
29	**MX2**
31	**MX4**
33	**MX8**
35	**MX6**
37	**MX10**
39	**MX9**
41	**MX7**
43	GND

N10B

1	V–6
3	MX11
5	MX13
7	CORENEUTRAL
9	MX14
11	MX12
13	MX10
15	MX8
17	MX6
19	MX4
21	MX2
23	nW1
25	nW8
27	nW4
29	nW2
31	nG1
33	**nMSENSE4**
35	**nMSENSE2**
37	F54
39	ST26
41	**BLDKRCLK**
43	GND

Note: Bold-faced expressions are signal source.