IME 84 Calculator

Schematic

Contents

Notes

- Gate symbols and signal names are presented in accordance with:
  logic 0 = 0V, GND
  logic 1 = –12V

- The symbol N*bb.pp* denotes a physical connector pin. *bb*=board, *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.

- Arrows indicate direction of signal or energy flow.

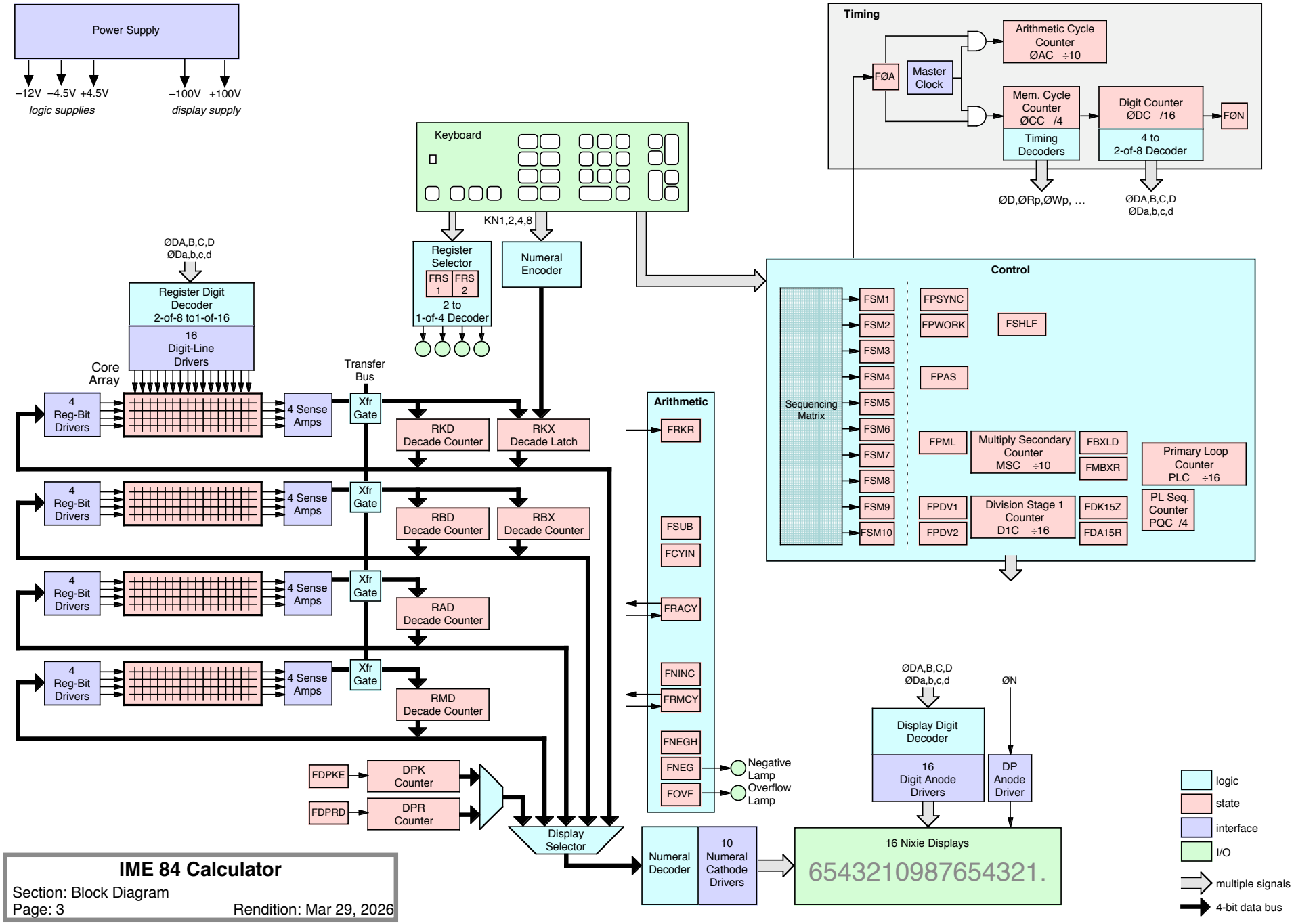
- The symbol with no label denotes –12V.

- The symbol with no label denotes +4.5V.

- These drawings are based on three sources:
  - Redrawing and interpretation to logic of the reverse-engineered discrete-component schematic produced by K. Krause in 1986-7.
  - Photos and examination of Unit 1.8400903 by J.Ongena.
  - Board photos of a unit, from DoPecc.

Revision Log

- 2025 Sep: Initial drawing / bhilpert.



IME 84 Calculator

Section: Block Diagram

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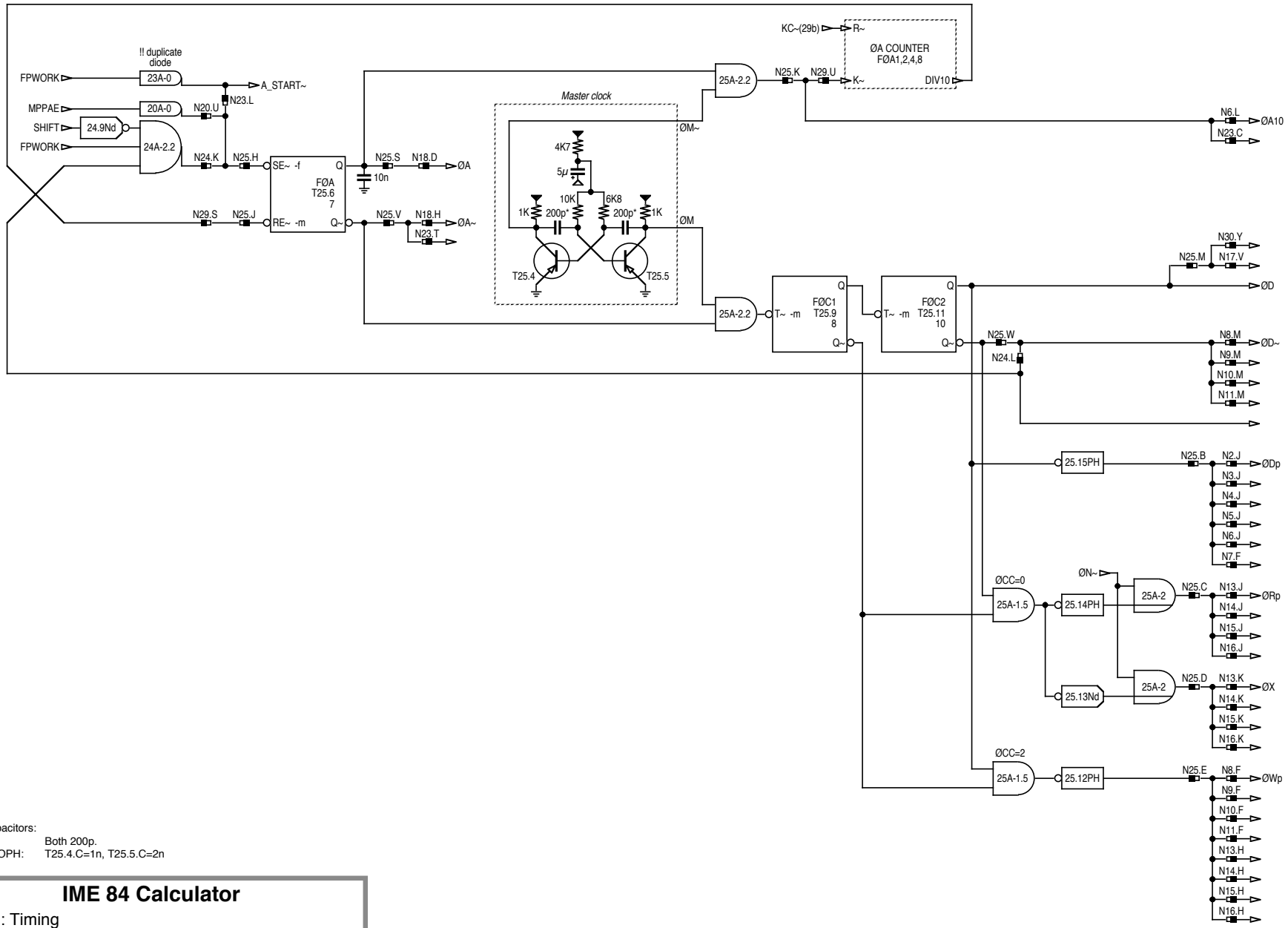

*ØM capacitors:
K87: Both 200p.
#903, DOPH: T25.4.C=1n, T25.5.C=2n

IME 84 Calculator

Section: Timing
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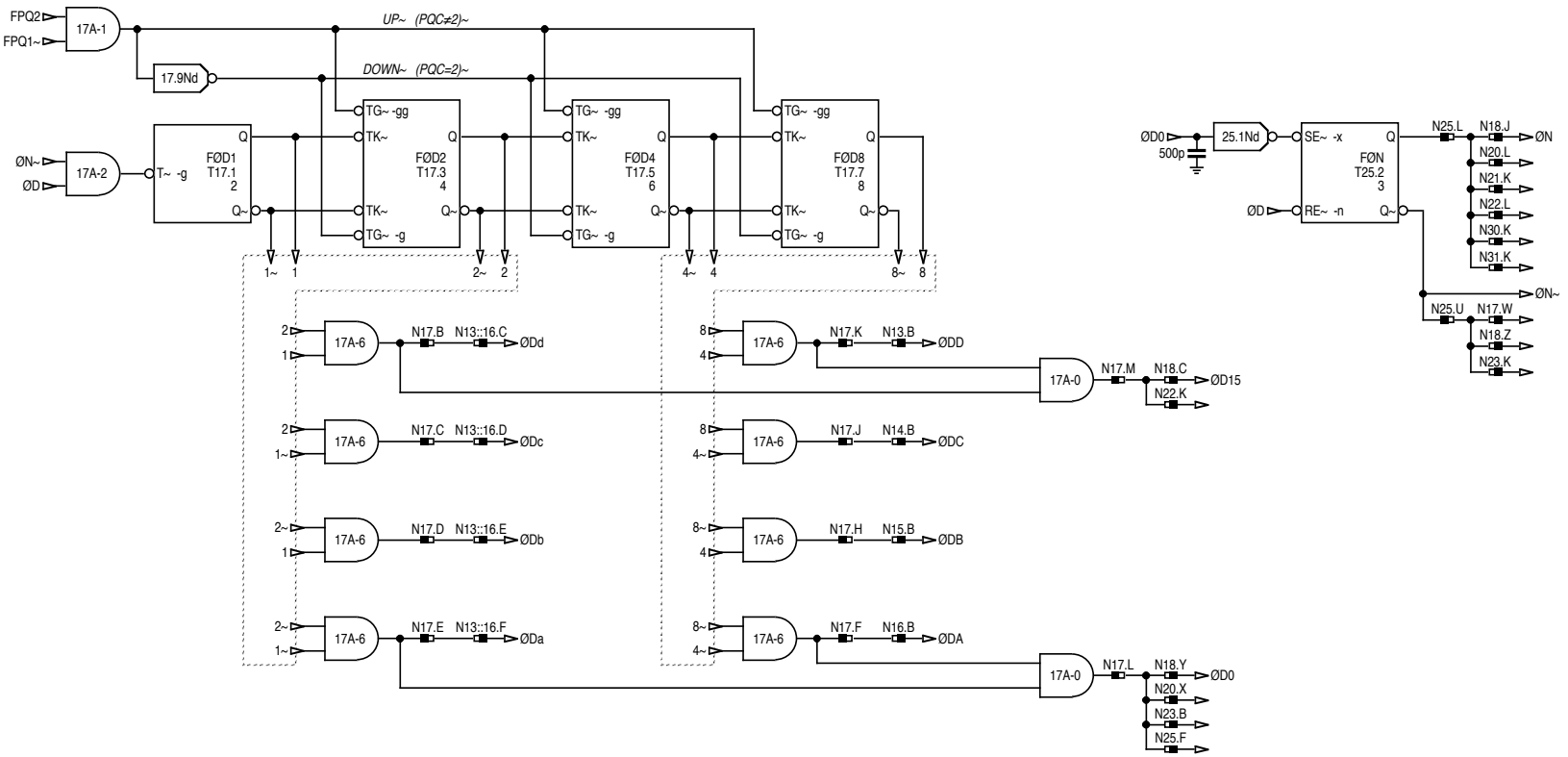
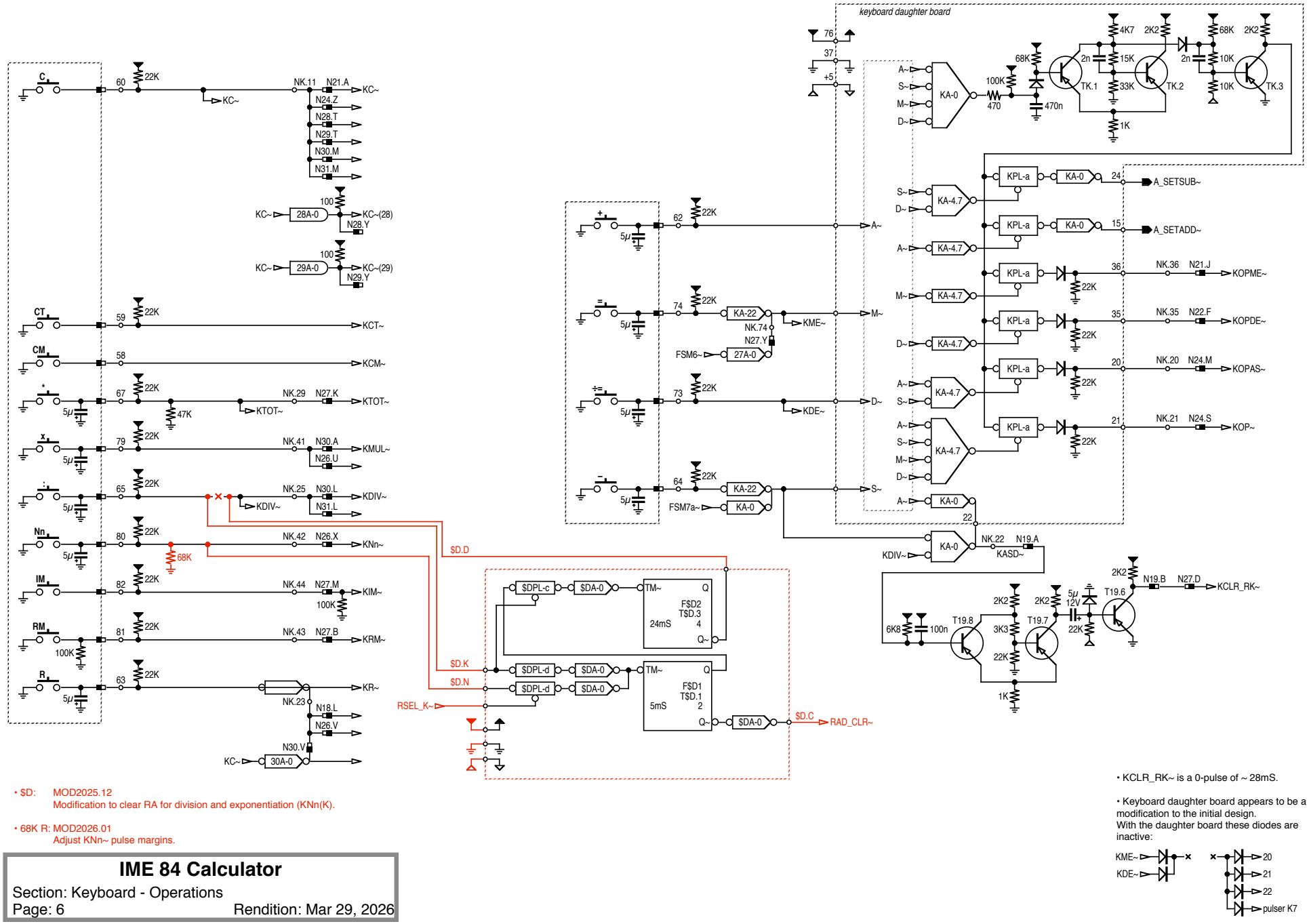


Major-minor Decoding

2 ● (1-of-4)

	a	b	c	d
A	0	1	2	3
B	4	5	6	7
C	8	9	10	11
D	12	13	14	15



• $D: MOD2025.12
Modification to clear RA for division and exponentiation (KNn(K).

• 68K R: MOD2026.01
Adjust KNn~ pulse margins.

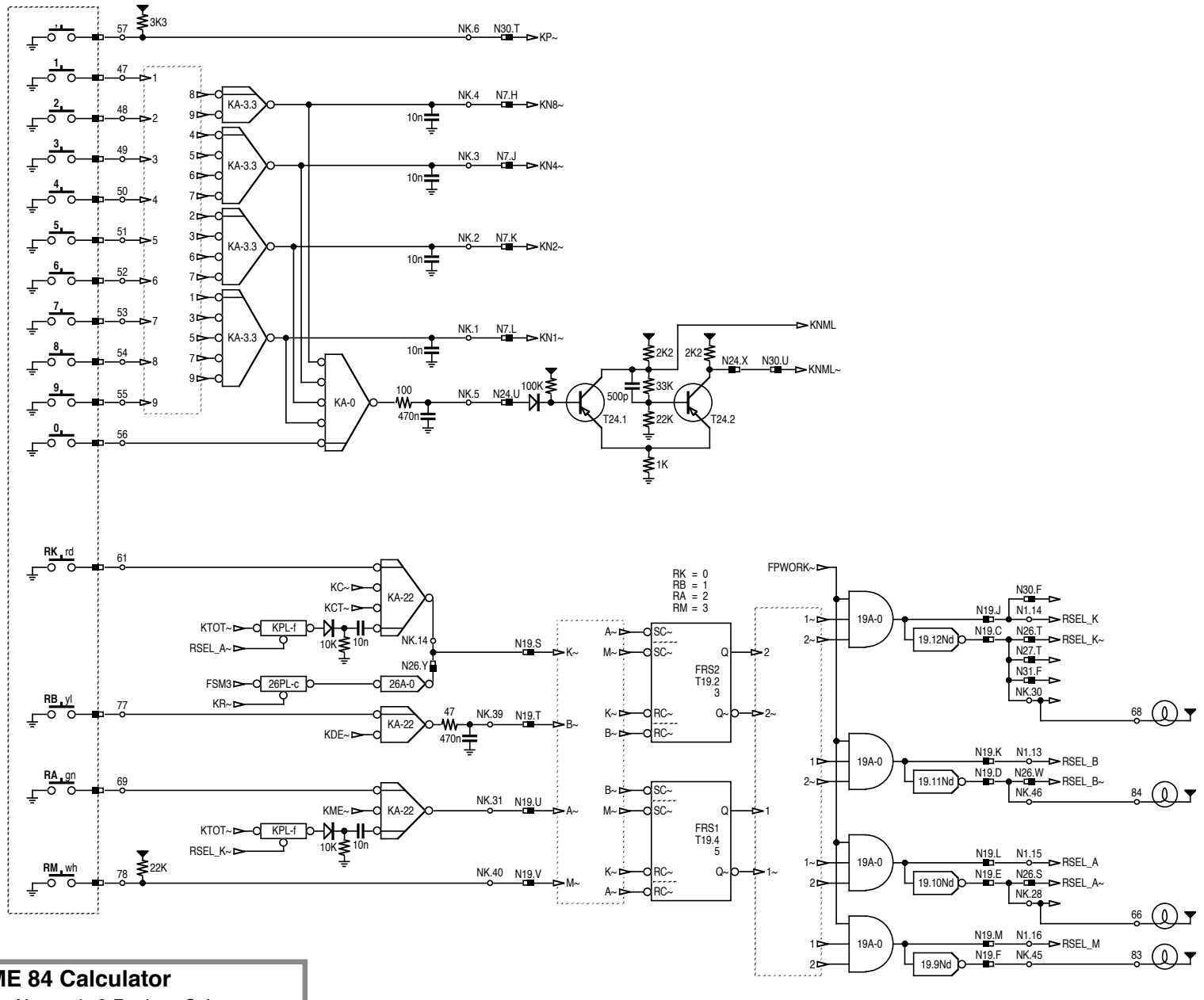
• KCLR_RK~ is a 0-pulse of ~ 28mS.

• Keyboard daughter board appears to be a modification to the initial design.
With the daughter board these diodes are inactive:

IME 84 Calculator

Section: Keyboard - Operations

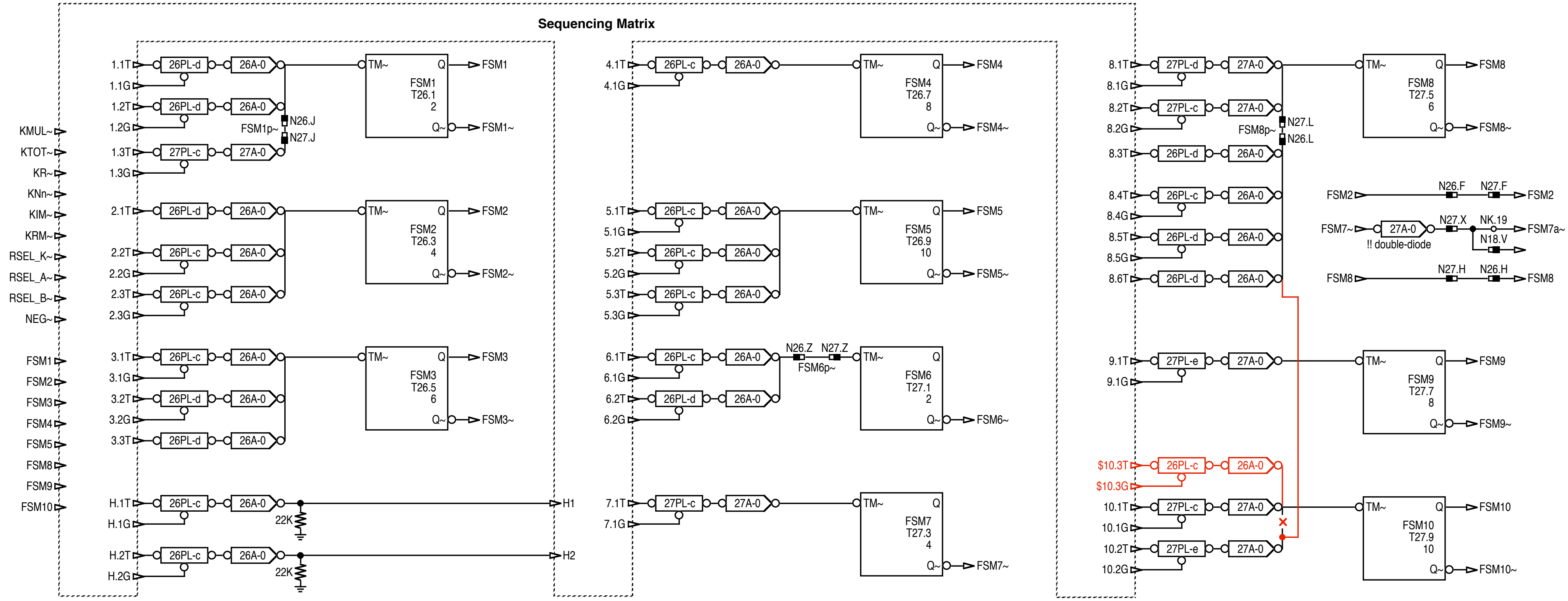
Page: 6 Rendition: Mar 29, 2026



IME 84 Calculator

Section: Keyboard - Numerals & Register-Select

Rendition: Mar 29, 2026



Sequences

Initiator	Triggered Pulsers					
KMUL:	3.3	5.1	8.4	(2.2)		
KTOT(NEG):	8.1	1.3	2.1	7.1		
KR(A):	8.6	H1	1.2	2.1	3.1	
KR(B):	8.6	H1	5.3	2.3	3.1	
KNn (K):	3.2	5.2	4.1	8.3	H2	6.2
KNn (A):	8.5	H2	1.1	2.1	6.1	
KIM(K):	9.1	10.1	8.2			
KRM(K):	10.2					
KRM(K):	8 via 10.2		$10.3			

• $10.3: MOD2026.02
Modification to clear RK for Recall-Memory.

• #903: Pulser 2.2 is absent. RA is not pre-cleared.

• K87: PL 91 & 102 are both type e.
DOPH: PL 91 is type c while PL 102 is type e.

Actions

Mono	Period	Action	Description
FSM1:	24mS	RK <=> RA	Enable transfer RK & RA
FSM2:	5mS	0 => RA	Clear decade RAD
FSM3:	5mS	0 => RB Select RK if KR	Clear decades RBD & RBX Pulse KRK if KR
FSM4:	24mS	RA <=> RB	Enable transfer RA & RB
FSM5:	24mS	RK <=> RB	Enable transfer RK & RB
FSM6:	5mS	Trigger Multiply	Pulse KME
FSM7:	18mS	Trigger Subtract Suppress RM Incr.	Pulse KSUB
FSM8:	5mS	0 = >RK	Clear decades RKD & RKX
FSM9:	5mS	0 => RM	Clear decade RMD
FSM10:	24mS	RK <=> RM	Enable transfer RK & RM

Sequencing Matrix Connections

Source Outputs	Destination Pulsers 1			2			3			4	5			6		7	8						9	10			H	
	1	2	3	1	2	3	1	2	3	1	1	2	3	1	2	1	1	2	3	4	5	6	1	1	2	3	1	2
KMUL~					G				T		G									G								
KTOT~			G													G	T											
KR~						G	G															T					G	
KNn~								T		G		G		G							T							G
KIM~																		G					T	G				
KRM~																									T	G		
RSEL_K~								G							G								G		G			
RSEL_A~	G	G																			G							
RSEL_B~													G															
NEG~																	G											
FSM1				T																								
FSM2							T							T		T												
FSM3											T	T																
FSM4																			T									
FSM5						T				T										T								
FSM8			T		T																					T	T	T
FSM9																								T				
FSM10																		T										
H1		T											T															
H2	T														T													

IME 84 Calculator

Section: Control - Sequencer
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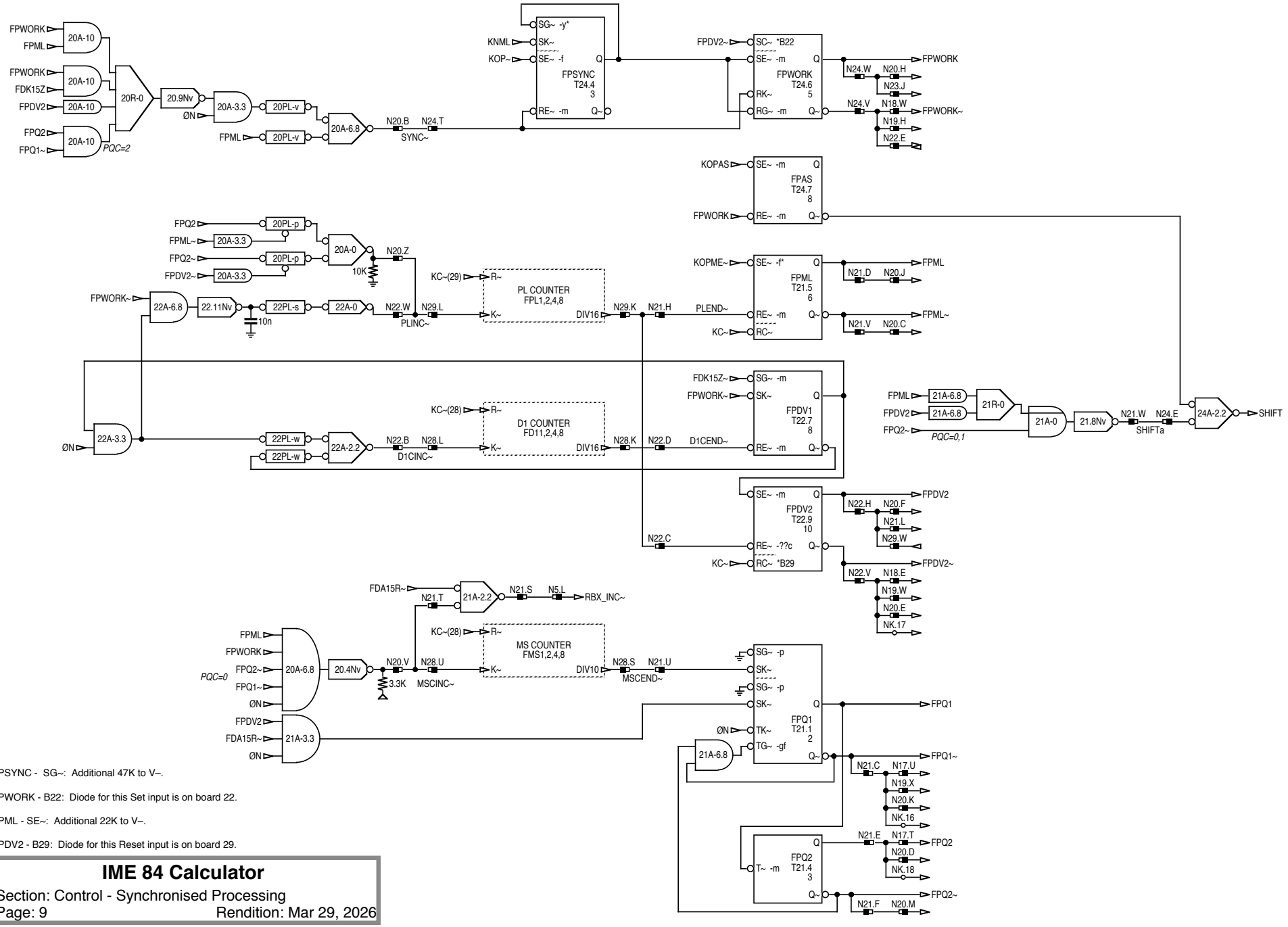


*FPSYNC - SG~: Additional 47K to V–.

*FPWORK - B22: Diode for this Set input is on board 22.

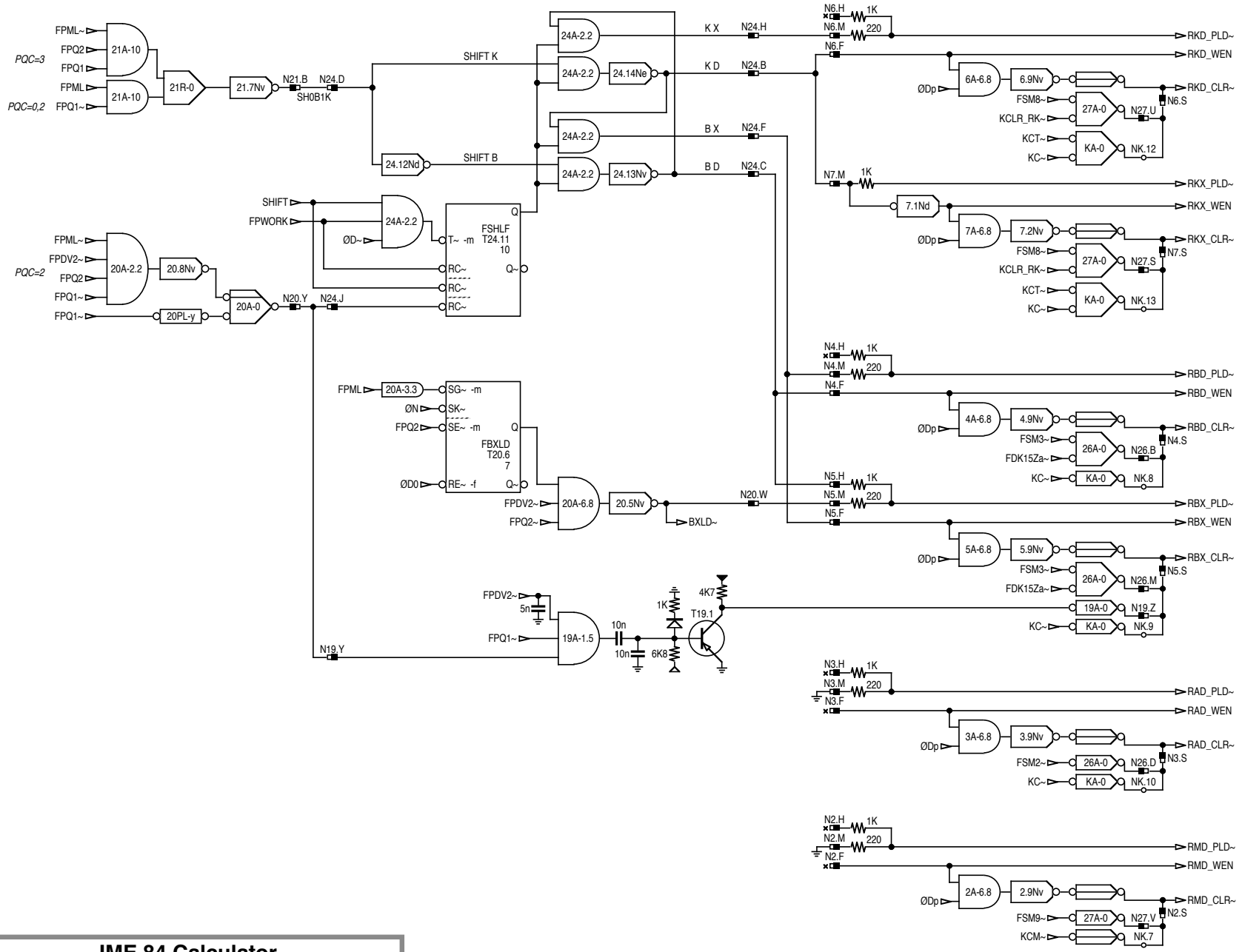
*FPML - SE~: Additional 22K to V–.

*FPDV2 - B29: Diode for this Reset input is on board 29.

IME 84 Calculator

Section: Control - Synchronised Processing

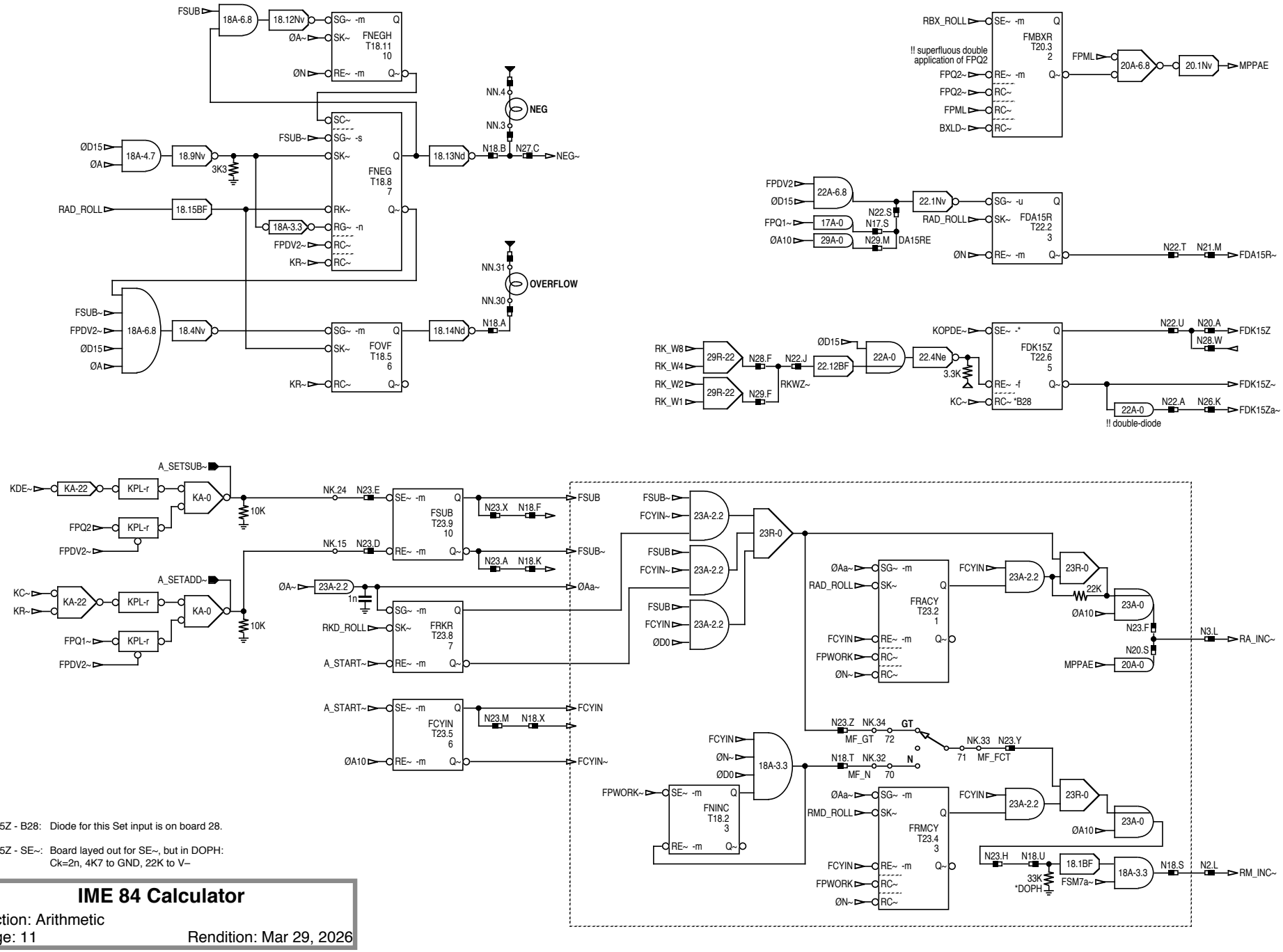
Page: 9 Rendition: Mar 29, 2026



IME 84 Calculator

Section: Control - Register Controls & Shift Logic

 Rendition: Mar 29, 2026



*FDK15Z - B28: Diode for this Set input is on board 28.

*FDK15Z - SE~: Board layed out for SE~, but in DOPH:
Ck=2n, 4K7 to GND, 22K to V–

IME 84 Calculator

Section: Arithmetic

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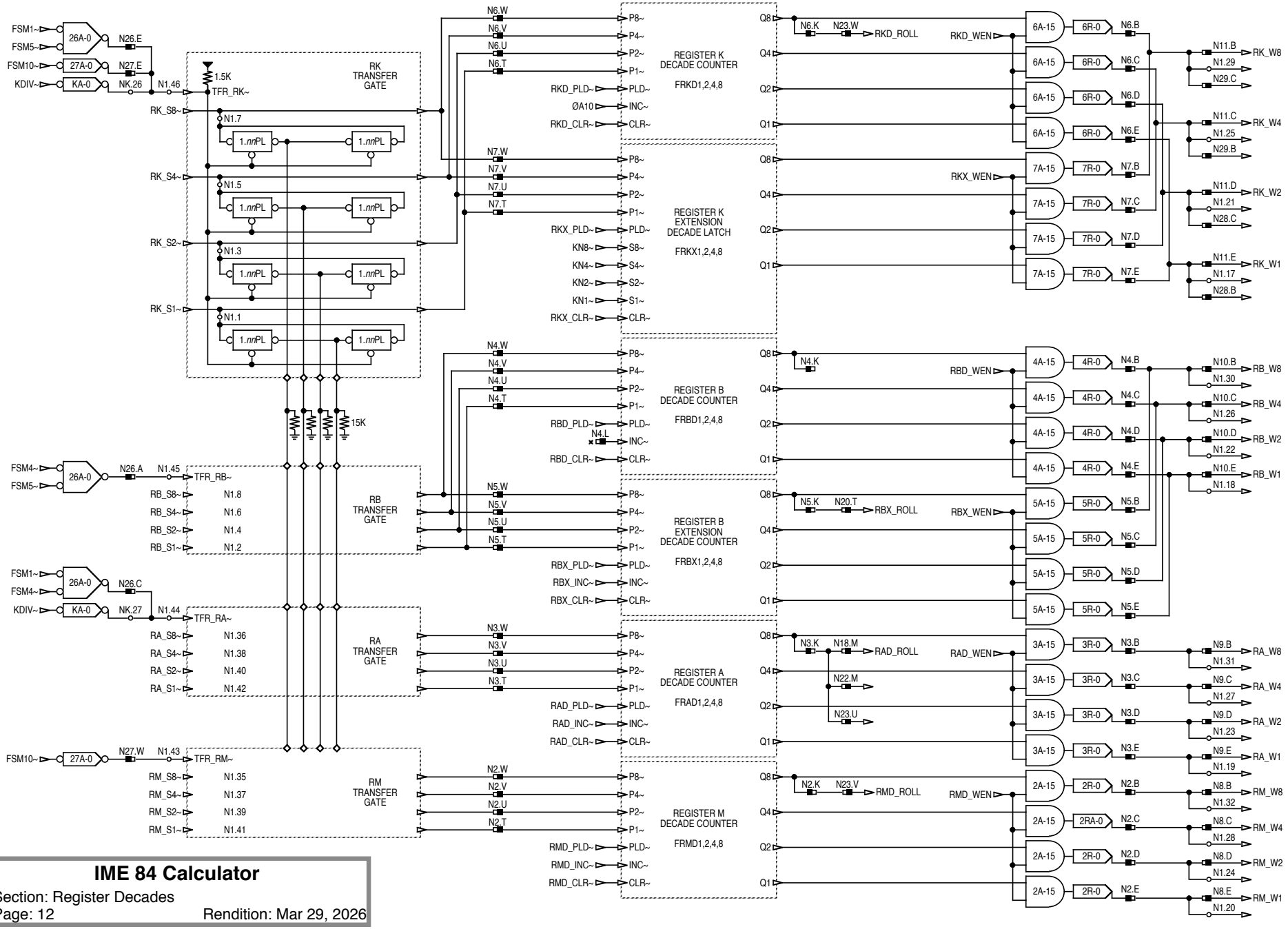

IME 84 Calculator

Section: Register Decades

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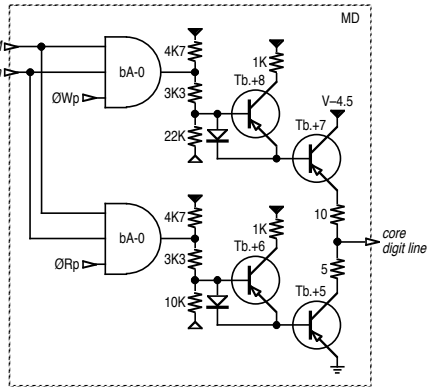
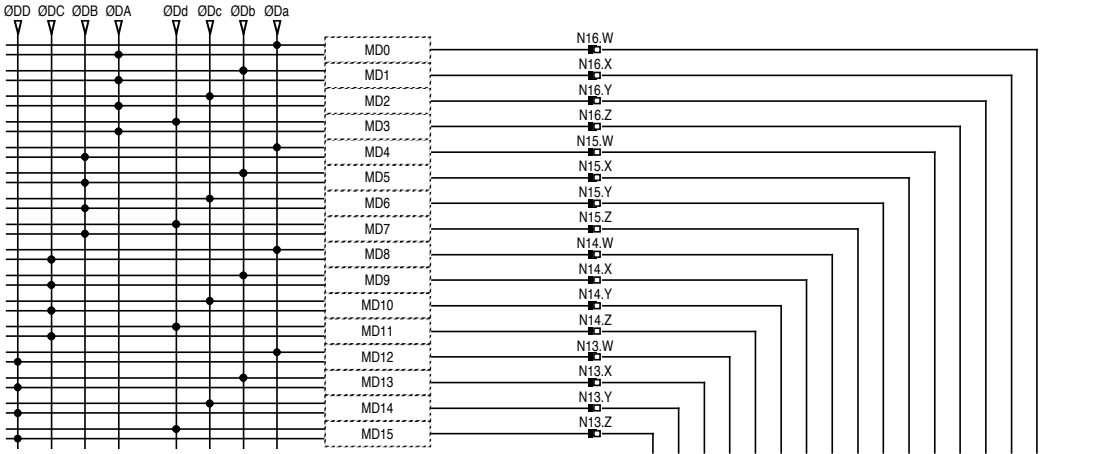
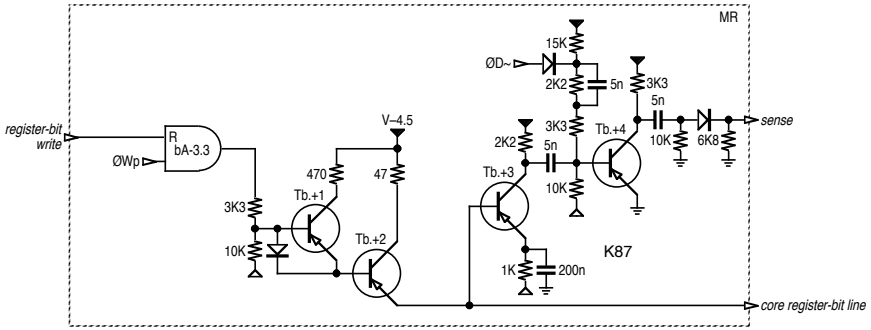
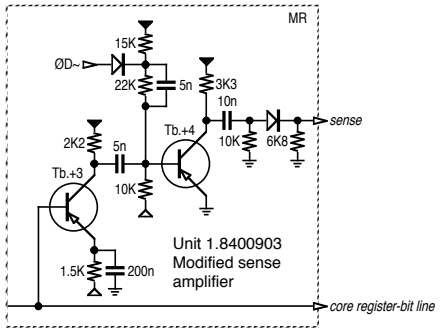


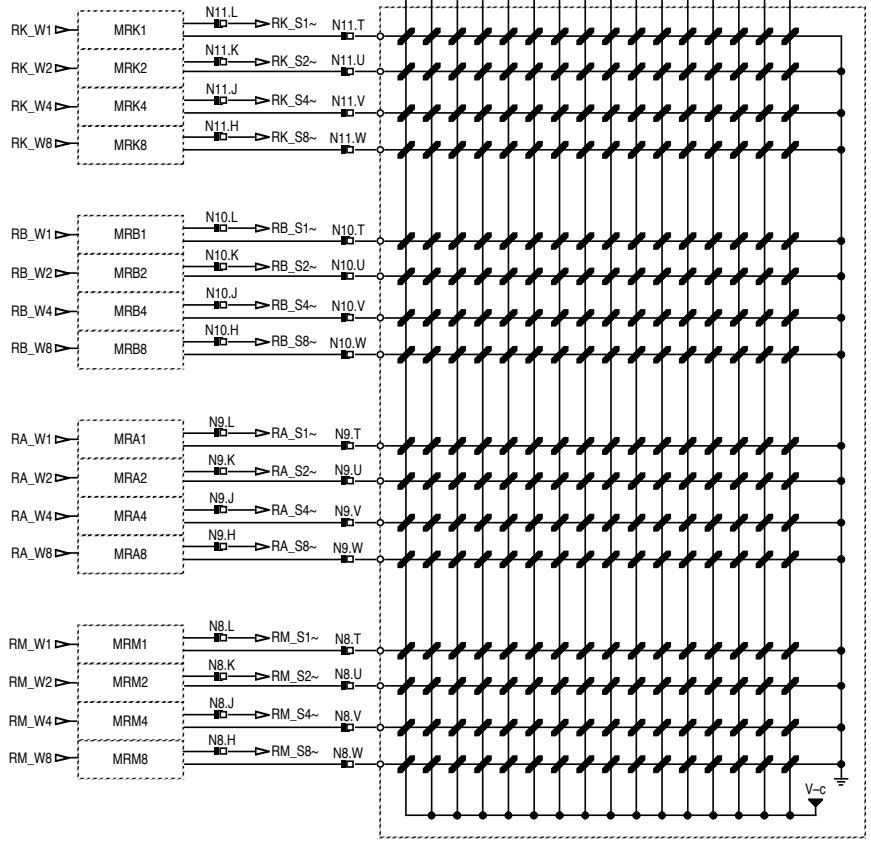
MD	+5	+6	+7	+8
0	T16.5	T16.6	T16.7	T16.8
1	T16.9	T16.10	T16.11	T16.12
2	T16.13	T16.14	T16.15	T16.16
3	T16.17	T16.18	T16.19	T16.20
4	T15.5	T15.6	T15.7	T15.8
5	T15.9	T15.10	T15.11	T15.12
6	T15.13	T15.14	T15.15	T15.16
7	T15.17	T15.18	T15.19	T15.20
8	T14.5	T14.6	T14.7	T14.8
9	T14.9	T14.10	T14.11	T14.12
10	T14.13	T14.14	T14.15	T14.16
11	T14.17	T14.18	T14.19	T14.20
12	T13.5	T13.6	T13.7	T13.8
13	T13.9	T13.10	T13.11	T13.12
14	T13.13	T13.14	T13.15	T13.16
15	T13.17	T13.18	T13.19	T13.20





MR	+1	+2	+3	+4
K1	T11.1	T11.2	T11.3	T11.4
K2	T11.5	T11.6	T11.7	T11.8
K4	T11.9	T11.10	T11.11	T11.12
K8	T11.13	T11.14	T11.15	T11.16
B1	T10.1	T10.2	T10.3	T10.4
B2	T10.5	T10.6	T10.7	T10.8
B4	T10.9	T10.10	T10.11	T10.12
B8	T10.13	T10.14	T10.15	T10.16
A1	T9.1	T9.2	T9.3	T9.4
A2	T9.5	T9.6	T9.7	T9.8
A4	T9.9	T9.10	T9.11	T9.12
A8	T9.13	T9.14	T9.15	T9.16
M1	T8.1	T8.2	T8.3	T8.4
M2	T8.5	T8.6	T8.7	T8.8
M4	T8.9	T8.10	T8.11	T8.12
M8	T8.13	T8.14	T8.15	T8.16





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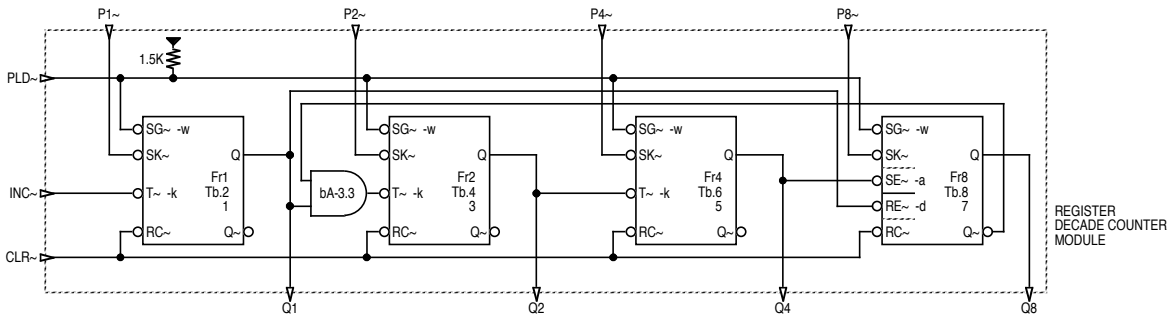
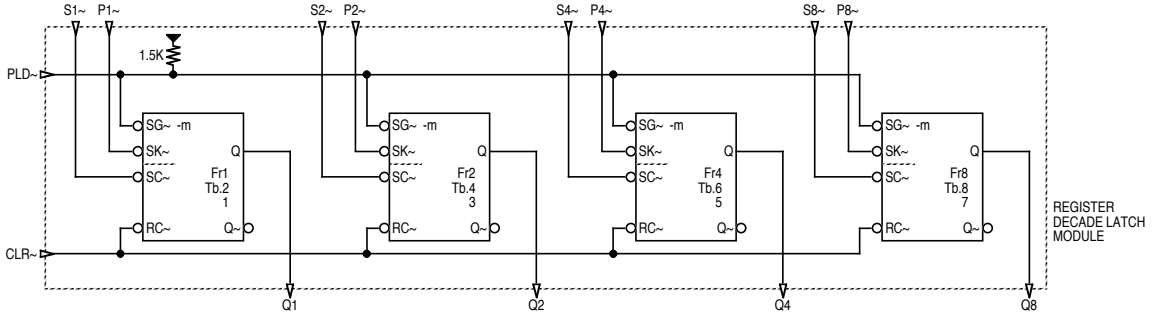
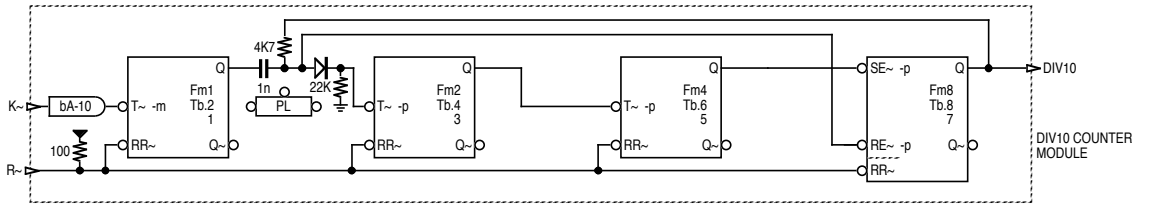
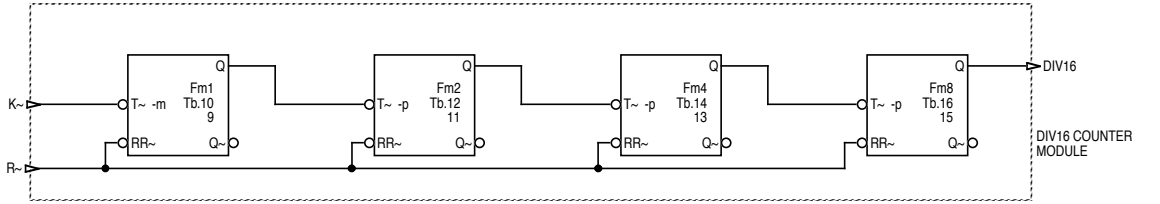
Section: Register Core Matrix, Drivers & Sense Amps

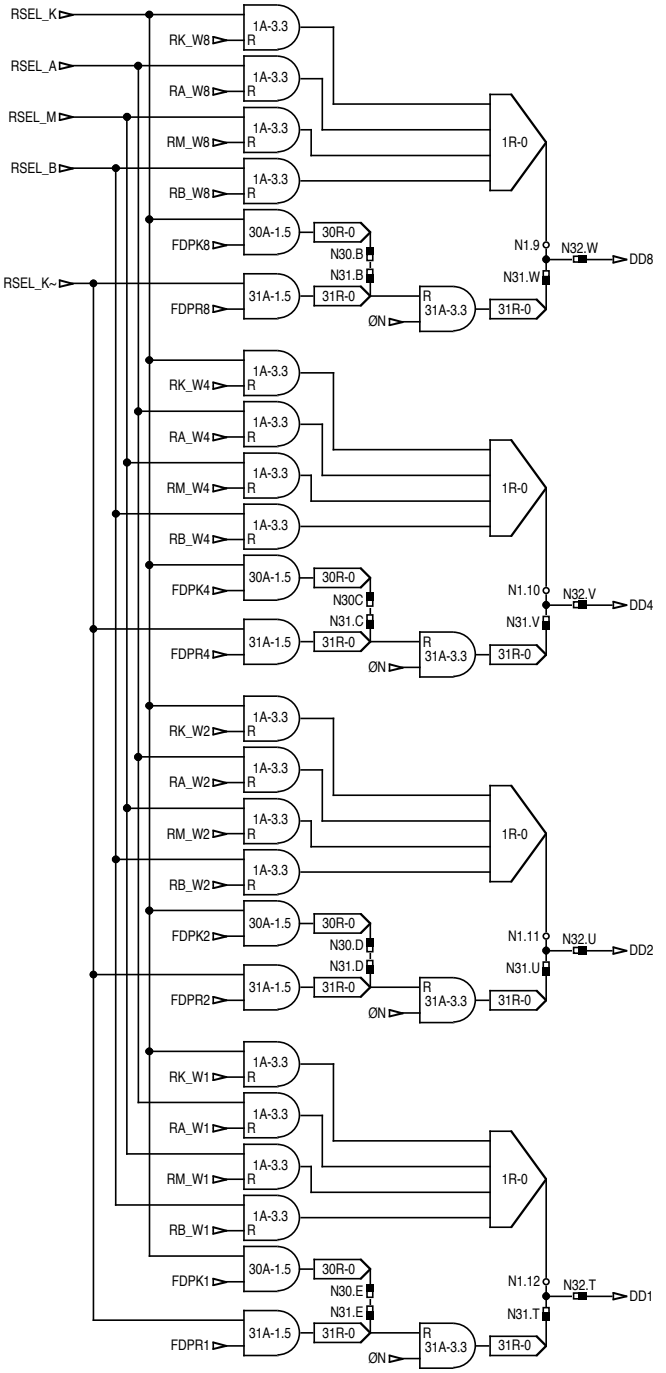
 Rendition: Mar 29, 2026











IME 84 Calculator

Section: Counter Modules & Display Selector

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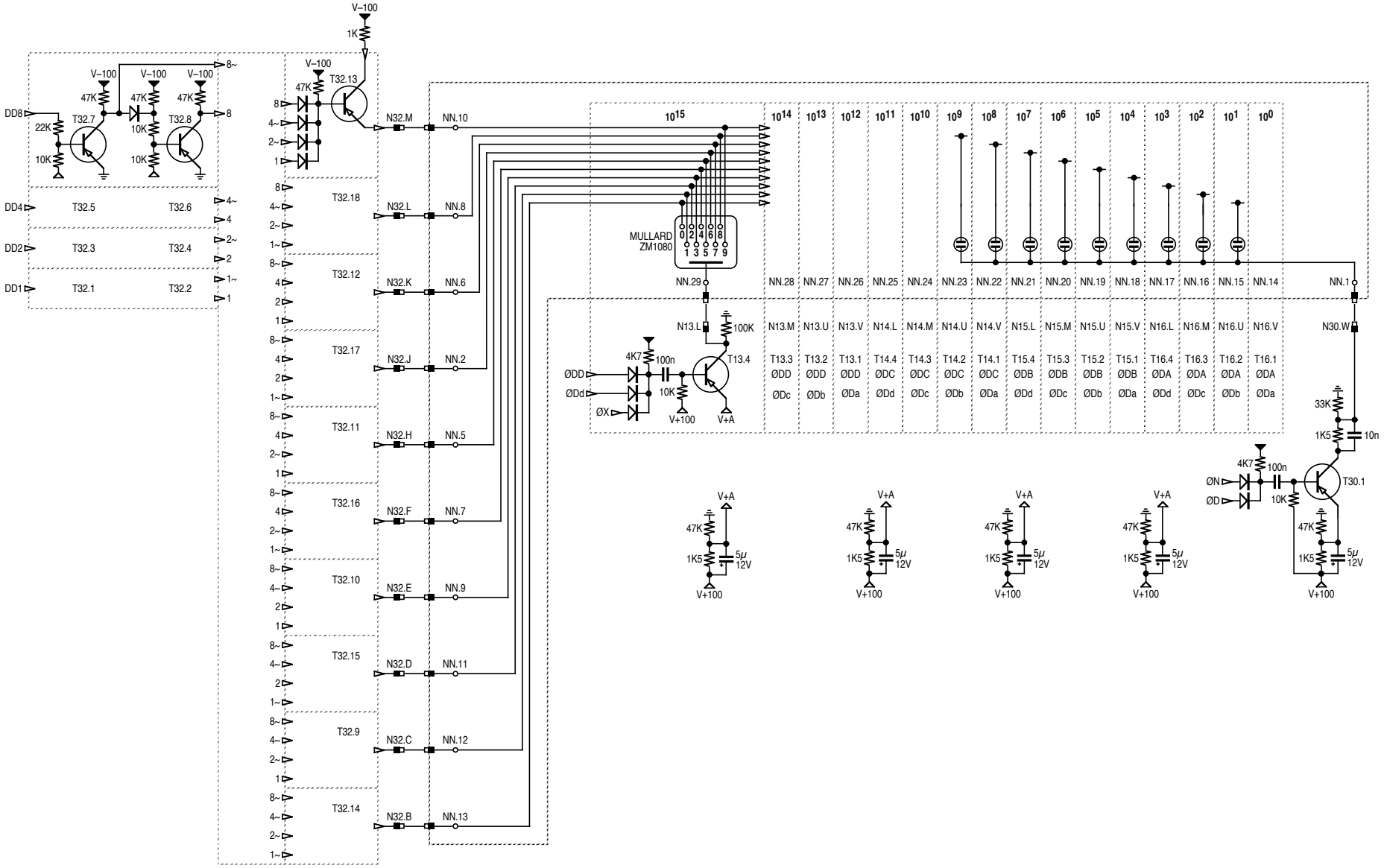

IME 84 Calculator

Section: Display

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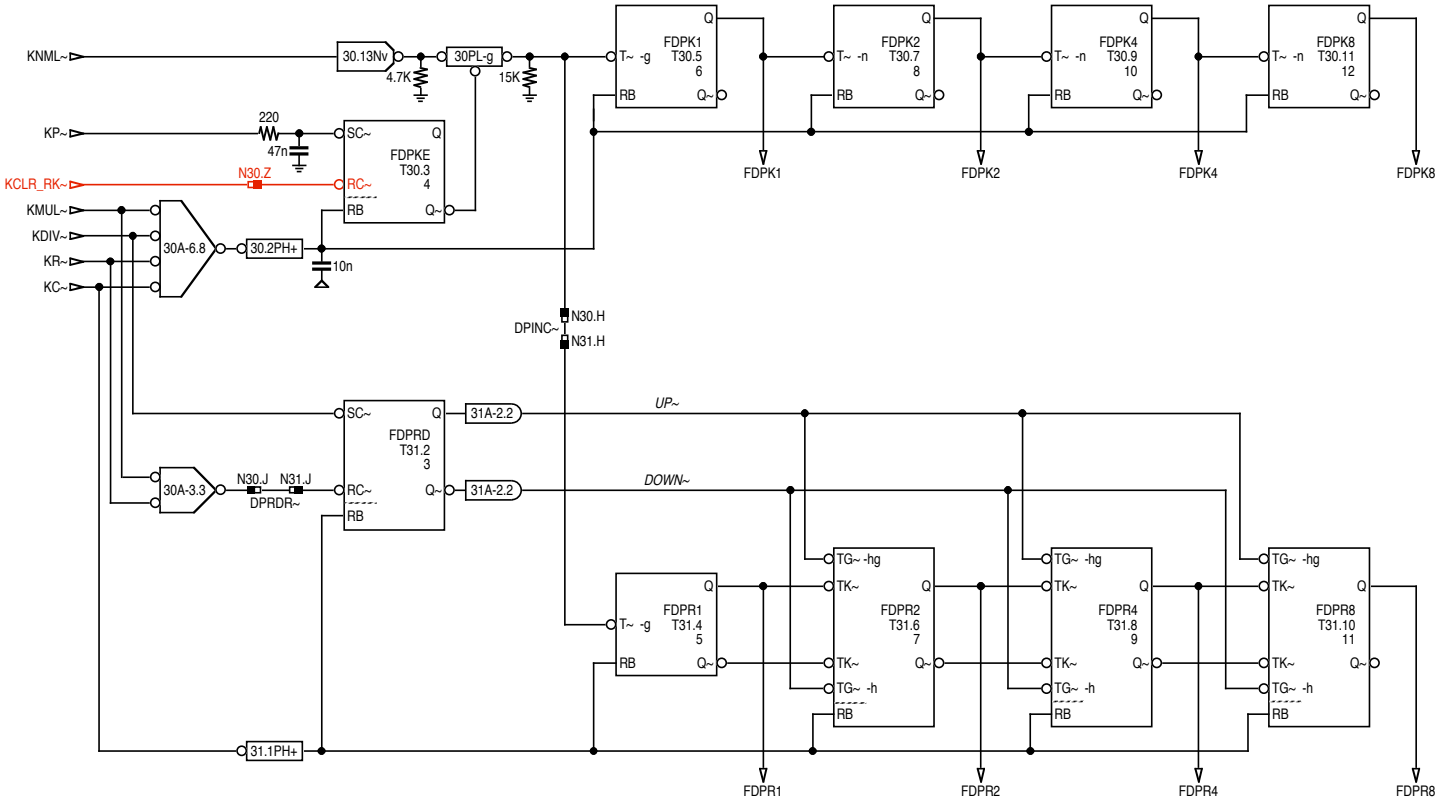
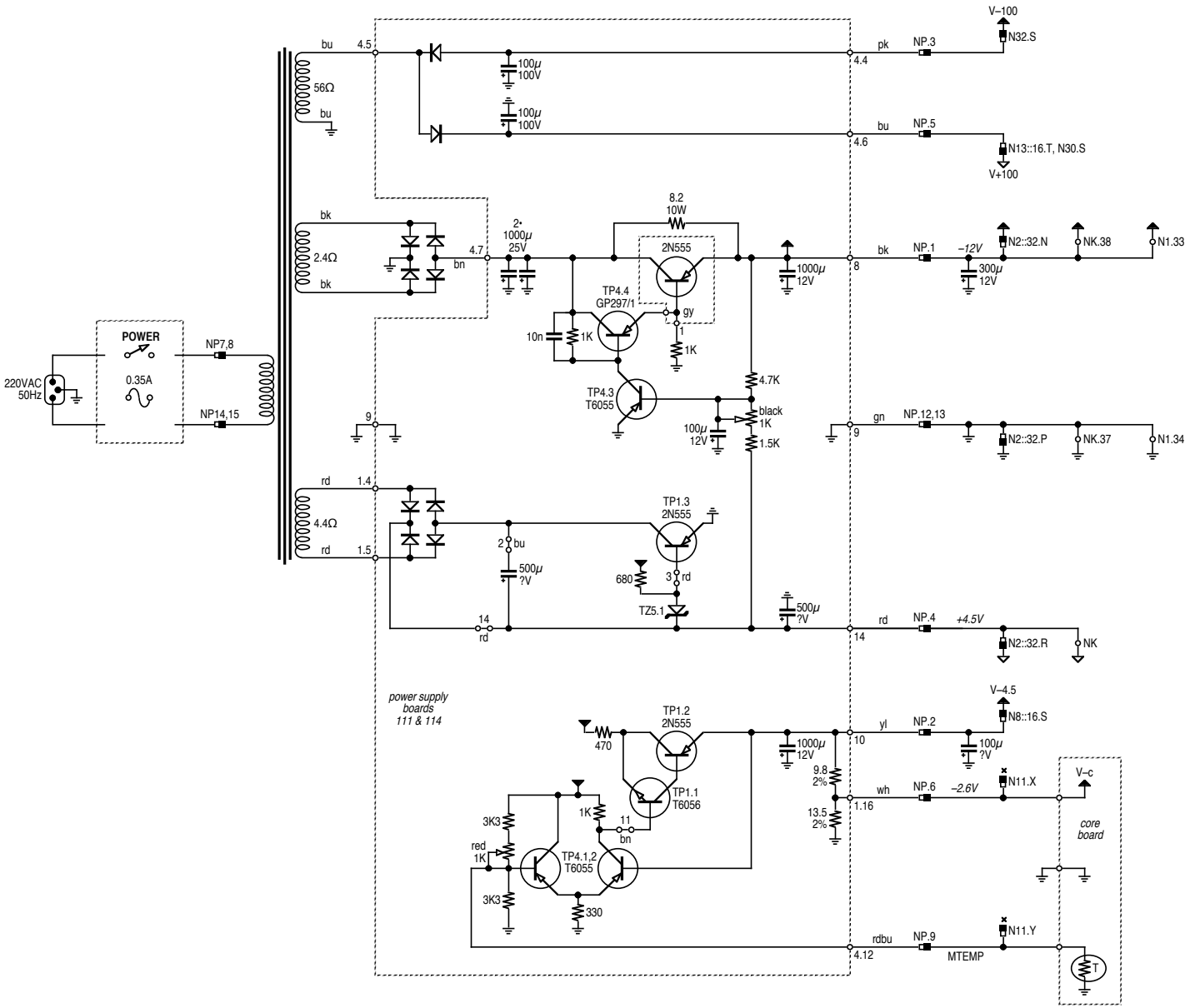


N30.Z: MOD2025.11
Modification to allow the DP to be set & fixed
for the duration of a summation.



IME 84 Calculator

Section: Power Supply

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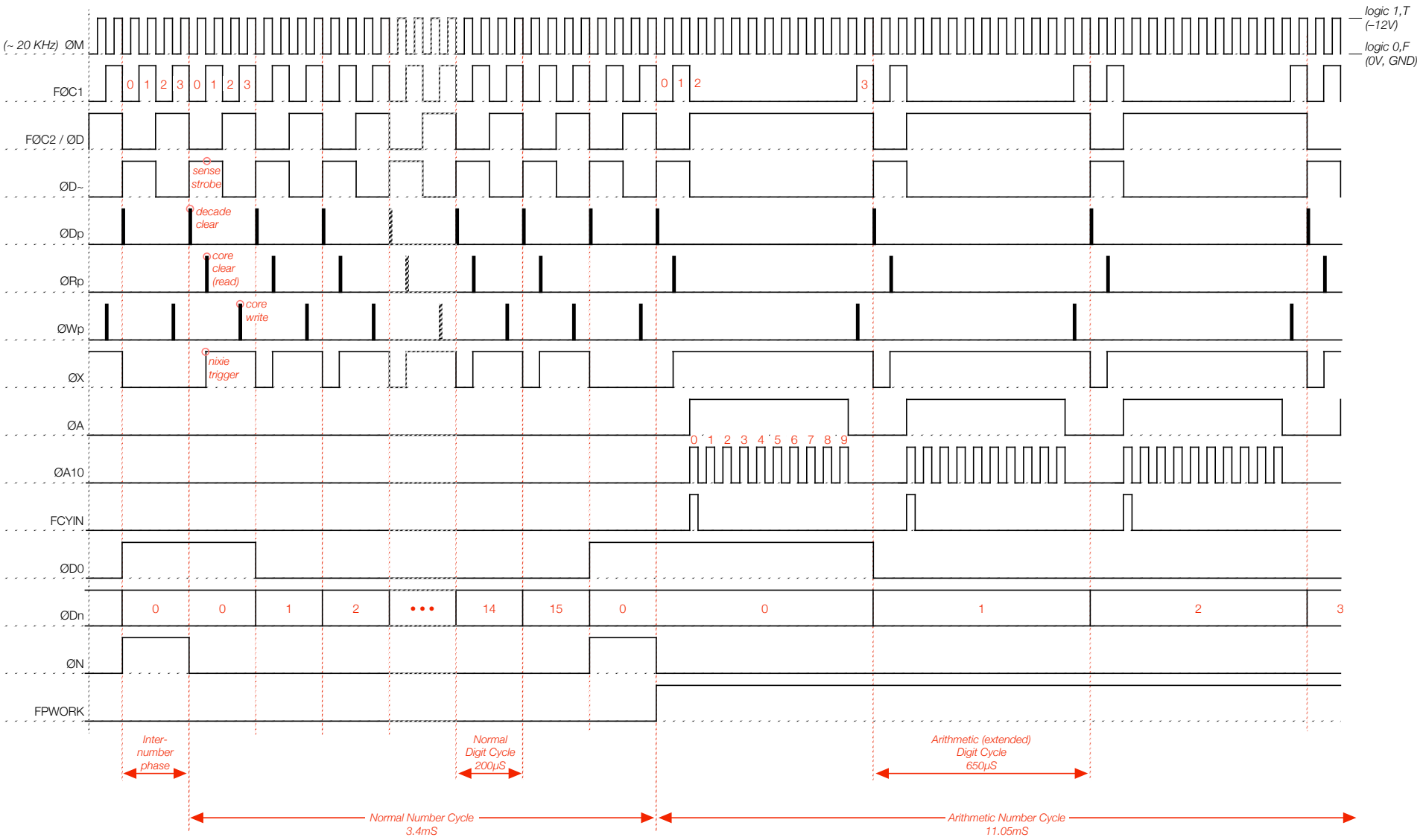

IME 84 Calculator

Section: Timing Graph

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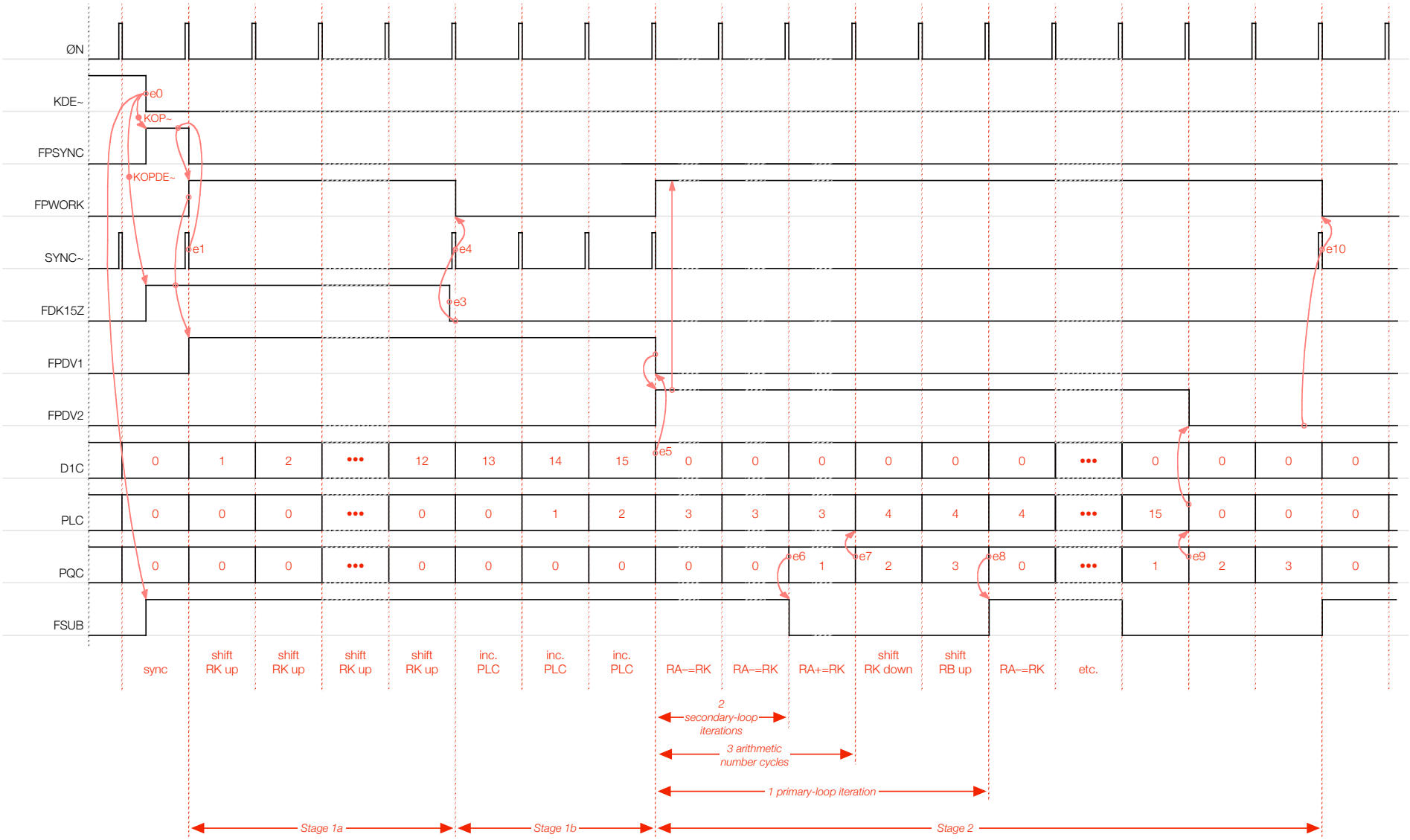
Rendition: Mar 29, 2026

- The diagram shows the transition from a normal number cycle to an arithmetic number cycle such as occurs when FPWORK asserts for an ADD or SUBTRACT procedure.
- Unit 1.8400903: ØM = 18.9 KHz

Pulser-generated pulse (RC)



IME 84 Calculator

Section: Timing Graph - Division

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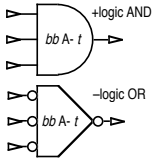
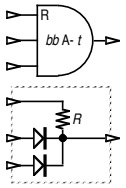
- Division example with a 4-digit divisor, and for which the first digit of the quotient will be 1.

AND-Form Gates

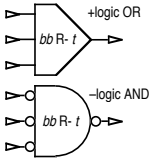


R = *t* •1000
If *t*=0, no resistor is present.

AND-Form with pull-up as input:

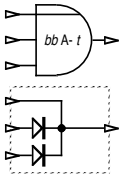


OR-Form Gates

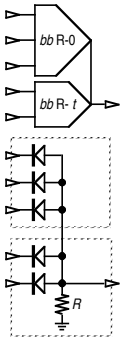


R = *t* •1000
If *t*=0, no resistor is present.

Wired Inputs
(AND-form example)



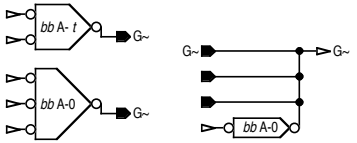
Distributed Gates
(OR-form example)



The perpendicular output line on a gate symbol indicates this is part of a distributed gate.

One of the contributors provides the load R while the others are (typically) type-0 (no load R).

Distributed Gate Separated on Pages
(–logic OR example)



This gate has 6 inputs in total.

The black tab symbol indicates this circuit electrically has multiple sources.

Gate Identification

Gates are identified with a label of the form:

bb gg - t
or *bb . tt gg - t*

where:

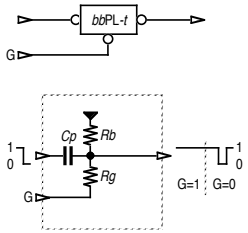
bb = board [1::34]
tt = transistor number in PCB foil
gg = gate type
t = optional type variation

gg =

A	AND
R	OR
Nv	NOT
Nd	NOT with diode & Rh
Ne	NOT with delay cap on base
BF	buffer
PL	pulse 0 on 0-edge
PH	pulse 1 on 0-edge
PH+	like PH but swings down to + for FF-RB inputs

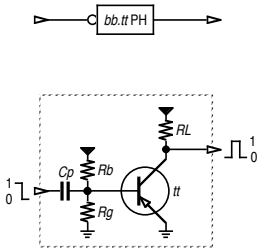
• Logic 0, F = 0V, GND
Logic 1, T = –12V

Pulsers

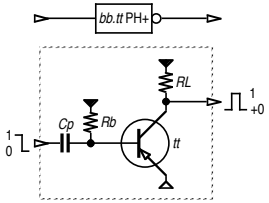


t	Cp	Rg	Rb
a	10n	6K8	-
c	10n	22K	-
d	10n	22K	47K
e	10n	22K	22K
f	10n	10K	-
g	10n	47K	-
p	5n	4K7	-
r	5n	10K	-
s	5n	15K	-
v	5n	-	6K8
w	5n	-	10K
y	10n	-	4K7

If the gate input is not present on a symbol instance, Rg is grounded (always enabled).

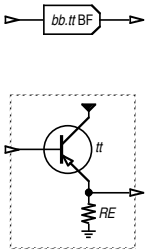


bb.tt	Rg	Cp	Rb	RL
25.12	-	2n	4K7	2K2
25.14	-	?2n	4K7	2K2
25.15	-	5n	4K7	2K2

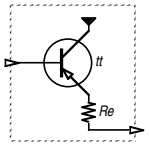


bb.tt	Rb	Cp	RL
30.2	33K	10n	2K2
31.1	33K	10n	1K5

Buffers

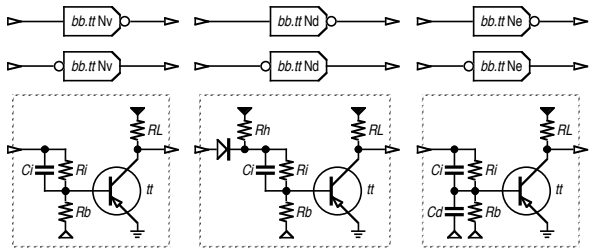


bb.tt	RE
18.1	220
18.15	33?330



bb.tt	Re
22.12	3K3

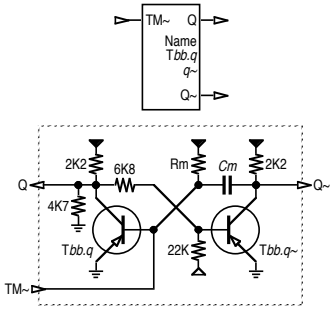
Inverters



bb.tt	Rh	Ri	Rb	RL	Ci
2.9	-	4K7	15K	4K7	1n
3.9	-	4K7	15K	4K7	1n
4.9	-	4K7	15K	4K7	1n
5.9	-	4K7	15K	4K7	1n
6.9	-	4K7	15K	4K7	1n
7.1	6K8	4K7	15K	3K3	1n
7.2	-	4K7	15K	3K3	1n
17.9	6K8	4K7	15K	2K2	-
18.4	-	4K7	15K	2K2	500p
18.9	-	6K8	15K	2K2	1n
18.12	-	4K7	15K	2K2	500p
18.13	2K2	3K3	10K	-	-
18.14	2K2	3K3	10K	-	-
19.9	2K2	3K3	10K	-	-
19.10	2K2	3K3	10K	-	-
19.11	2K2	3K3	10K	-	-
19.12	2K2	3K3	10K	-	-
20.1	-	4K7	15K	2K2	5n
20.4	-	4K7	15K	2K2	500p
20.5	-	4K7	15K	2K2	500p
20.8	-	4K7	15K	2K2	10n
20.9	-	4K7	15K	2K2	500p
21.7	-	4K7	15K	2K2	500p
21.8	-	4K7	15K	2K2	500p
22.1	-	4K7	15K	2K2	-
22.4	-	6K8	15K	2K2	500p
22.11	-	4K7	15K	2K2	500p
24.9	6K8	4K7	15K	2K2	470p
24.12	6K8	4K7	15K	2K2	470p
24.13	-	4K7	15K	2K2	470p
24.14	-	4K7	15K	2K2	-
25.1	6K8	4K7	15K	2K2	500p
25.13	2K2	15K	15K	2K2	-
30.13	-	22K	15K	2K2	-

Ne Special:
22.4: 2n capacitor base-GND
24.14: 1n capacitor base-GND

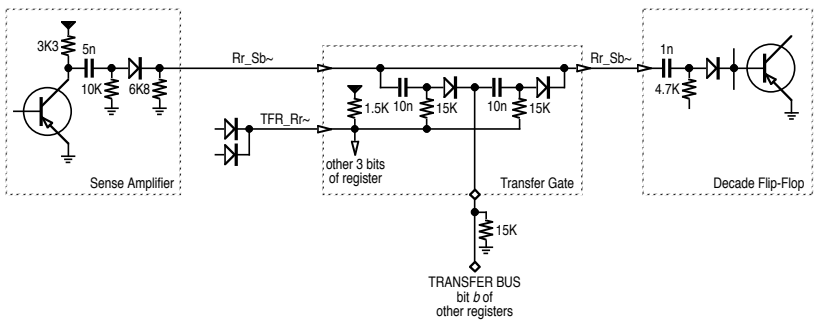
Monostable Flip-flops



MONO	Cm	Rm	mS
#903:			
FSM1	470n	68K	24
FSM2	100n	68K	5
FSM3	100n	68K	
FSM4	470n	68K	
FSM5	470n	68K	
FSM6	100n	68K	
FSM7	220n	100K	18
FSM8	100n	68K	5
FSM9	100n	68K	
FSM10	470n	68K	
DOPH:			
FSM6	"	33K	
FSM7	470n	47K	

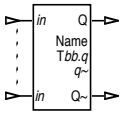
FSM7: MOD196X.A
Stabilise FSM7 by changing RC values per DOPH above.

Register Transfer Gate Circuit



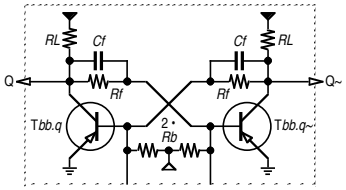
Flip-Flops

Flip-Flop Base

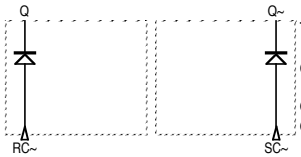


in are input options.

q & *q~* are transistor numbers in PCB foil.



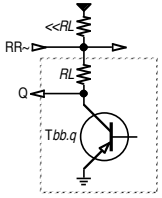
Input Options Level-Set



Types SC~ and RC~

Collector Set & Reset.

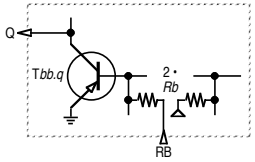
Q goes 1 if SC~ = 0.
Q goes 0 if RC~ = 0.



Type RR~

Similar to RC~.

Q goes 0 if RR~ = 0.

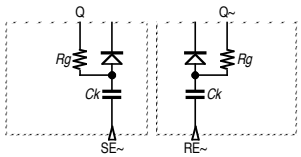


Type RB

Reset by raising bias R.
Must be driven by a source that swings + and –.

Q goes 0 when RB is –.

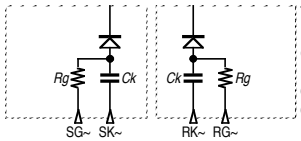
Input Options Edge-Triggered



Types SE~ and RE~

Edge-triggered Set & Reset.

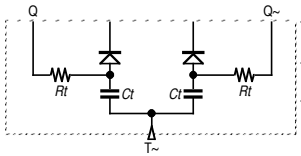
Q goes 1 on 1-to-0 edge of SE~.
Q goes 0 on 1-to-0 edge of RE~.



Types SG~ and RG~

Gated Edge-triggered Set & Reset.

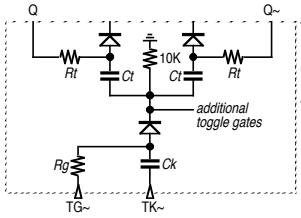
Q goes 1 if SG~=0 on 1-to-0 edge of SK~.
Q goes 0 if RG~=0 on 1-to-0 edge of RK~.



Type T

Toggle.

Toggle Q on 1-to-0 edge of T~.



Type TG

Gated Toggle.

Toggle Q if TG~=0 on 1-to-0 edge of TK~.

Base Component Values

Flip-Flop	RL	Rf	Cf	Rb
Timing				
FØA	1K	6K8	500p	22K
FØA1,2,4,8	2K2	10K	500p	22K
FØC1,2	680	6K8	500p	22K
FØD1,2,4,8	2K2	4.7K	1n	15K
FØN	2K2	4.7K	500p	22K
Registers				
FRS1,2	2K2	6K8	5n	22K
FRKD1,2,4,8	2K2	10K	470p	22K
FRKX1,2,4,8	2K2	10K	470p	22K
FRBD1,2,4,8	2K2	10K	470p	22K
FRBX1,2,4,8	2K2	10K	470p	22K
FRAD1,2,4,8	2K2	10K	470p	22K
FRMD1,2,4,8	2K2	10K	470p	22K
FBXLD	2K2	6K8	500p	22K
Arithmetic				
FSUB	2K2	6K8	-	22K
FCYIN	2K2	6K8	500p	22K
FRKR	2K2	6K8	500p	22K
FRACY	2K2	6K8	500p	22K
FRMCY	2K2	6K8	500p	22K
FNINC	2K2	6K8	500p	22K
FMBXR	2K2	6K8	500p	22K
FDK15Z	2K2	6K8	-	22K
FDA15R	2K2	6K8	500p	22K

Flip-Flop	RL	Rf	Cf	Rb
Control				
FPSYNC	2K2	6K8	??	22K
FPWORK	2K2	6K8	500p	22K
FPAS	2K2	6K8	-	22K
FPML	2K2	6K8	500p	22K
FPDV1	2K2	6K8	500p	22K
FPDV2	2K2	6K8	500p	22K
FPQ1	2K2	6K8	5n	22K
FPQ2	2K2	6K8	500p	22K
FSHLF	2K2	6K8	5n	22K
FNEG	2K2	6K8	500p	22K
FNEGH	2K2	6K8	*	22K
FOVF	2K2	6K8	500p	22K
Control Counters				
FPL1,2,4,8	2K2	10K	500p	22K
FMS1,2,4,8	2K2	10K	500p	22K
FD11,2,4,8	2K2	10K	500p	22K
DP Counters				
FDPK1,2,4,8	2K2	10K	500p	22K
FDPR1,2,4,8	2K2	10K	500p	22K
FDPKE	2K2	22K	500p	22K
FDPRD	2K2	10K	-	22K

*FNEGH: In DOPH,
Cf(Q.C)=500p
Cf(Q~.C)=5n

Input Component Value Codes

SG,RG : - *cRC* *cRC* –> Ck,Rg
SE,RE : - *cRC* *cRC* –> Ck,Rg
T : - *cRC* *cRC* –> Ct,Rt
TG : - *gcRC* *tcRC* *gcRC* –> Ck,Rg; *tcRC* –> Ct,Rt

cRC	R	C
a	3K3	470p
d	15K	470p
u	10K	220p
k	3K3	1n
m	4K7	1n
n	6K8	1n
p	10K	1n
s	22K	1n
f	4K7	5n
g	6K8	5n
h	15K	5n
w	4K7	2n
x	6K8	2n
y	10K	2n

Pin	N17	N16	N15	N14	N13
A	-	-	-	-	-
B	**ØDd**	ØDA	ØDB	ØDC	ØDD
C	**ØDc**	ØDd	ØDd	ØDd	ØDd
D	**ØDb**	ØDc	ØDc	ØDc	ØDc
E	**ØDa**	ØDb	ØDb	ØDb	ØDb
F	**ØDA**	ØDa	ØDa	ØDa	ØDa
H	**ØDB**	ØWp	ØWp	ØWp	ØWp
J	**ØDC**	ØRp	ØRp	ØRp	ØRp
K	**ØDD**	ØX	ØX	ØX	ØX
L	**ØD0**	**NXA3**	**NXA7**	**NXA11**	**NXA15**
M	**ØD15**	**NXA2**	**NXA6**	**NXA10**	**NXA14**
N	V–12	V–12	V–12	V–12	V–12
P	GND	GND	GND	GND	GND
R	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5
S	DA15RE	V–4.5	V–4.5	V–4.5	V–4.5
T	FPQ2	V+100	V+100	V+100	V+100
U	FPQ1~	**NXA1**	**NXA5**	**NXA9**	**NXA13**
V	ØD	**NXA0**	**NXA4**	**NXA8**	**NXA12**
W	ØN~	**MD0**	**MD4**	**MD8**	**MD12**
X	-	**MD1**	**MD5**	**MD9**	**MD13**
Y	-	**MD2**	**MD6**	**MD10**	**MD14**
Z	-	**MD3**	**MD7**	**MD11**	**MD15**

Pin	N12	N11	N10	N09	N08	N07	N06	N05	N04	N03	N02	N01
A		-	-	-	-	-	-	-	-	-	-	
B		RK_W8	RB_W8	RA_W8	RM_W8	**RK_W8**	**RK_W8**	**RB_W8**	**RB_W8**	**RA_W8**	**RM_W8**	
C		RK_W4	RB_W4	RA_W4	RM_W4	**RK_W4**	**RK_W4**	**RB_W4**	**RB_W4**	**RA_W4**	**RM_W4**	
D		RK_W2	RB_W2	RA_W2	RM_W2	**RK_W2**	**RK_W2**	**RB_W2**	**RB_W2**	**RA_W2**	**RM_W2**	
E		RK_W1	RB_W1	RA_W1	RM_W1	**RK_W1**	**RK_W1**	**RB_W1**	**RB_W1**	**RA_W1**	**RM_W1**	
F		ØWp	ØWp	ØWp	ØWp	ØDp	RKD_WEN	RBX_WEN	RBD_WEN	RAD_WEN	RMD_WEN	
H		**RK_S8~**	**RB_S8~**	**RA_S8~**	**RM_S8~**	KN8~	RKD_PLD1~	RBX_PLD1~	RBD_PLD1~	RAD_PLD1~	RMD_PLD1~	
J		**RK_S4~**	**RB_S4~**	**RA_S4~**	**RM_S4~**	KN4~	ØDp	ØDp	ØDp	ØDp	ØDp	
K		**RK_S2~**	**RB_S2~**	**RA_S2~**	**RM_S2~**	KN2~	**RKD_ROLL**	**RBX_ROLL**	**{RBD_ROLL}**	**RAD_ROLL**	**RMD_ROLL**	
L		**RK_S1~**	**RB_S1~**	**RA_S1~**	**RM_S1~**	KN1~	ØA10	RBX_INC~	{RBD_INC~}	RA_INC~	RM_INC~	
M		ØD~	ØD~	ØD~	ØD~	RKD_PLD1~	RKD_PLD2~	RBX_PLD2~	RBD_PLD2~	RAD_PLD2~	RMD_PLD2~	
N		V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12	
P	CORE	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	
R		V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	
S		V–4.5	V–4.5	V–4.5	V–4.5	**RKX_CLR~**	**RKD_CLR~**	**RBX_CLR~**	**RBD_CLR~**	**RAD_CLR~**	**RMD_CLR~**	
T		**MRK1**	**MRB1**	**MRA1**	**MRM1**	RK_S1~	RK_S1~	RB_S1~	RB_S1~	RA_S1~	RM_S1~	
U		**MRK2**	**MRB2**	**MRA2**	**MRM2**	RK_S2~	RK_S2~	RB_S2~	RB_S2~	RA_S2~	RM_S2~	
V		**MRK4**	**MRB4**	**MRA4**	**MRM4**	RK_S4~	RK_S4~	RB_S4~	RB_S4~	RA_S4~	RM_S4~	
W		**MRK8**	**MRB8**	**MRA8**	**MRM8**	RK_S8~	RK_S8~	RB_S8~	RB_S8~	RA_S8~	RM_S8~	
X		(V–c)	-	-	-	-	-	-	-	-	-	
Y		(MTEMP)	-	-	-	-	-	-	-	-	-	
Z		-	-	-	-	-	-	-	-	-	-	

IME 84 Calculator

Section: Connectors N1 :: N17

 Rendition: Mar 29, 2026

• Bold-faced expressions are signal sources.

	N22	N21	N20	N19	N18
A	**FDK15Za~**	KC~	FDK15Z	KASD~	**OVF~**
B	**D1CINC~**	**SH0B1K**	**SYNC~**	**KCLR_RK~**	**NEG~**
C	PLEND~	**FPQ1~**	FPML~	**RSEL_K~**	ØD15
D	D1CEND~	**FPML**	FPQ2	**RSEL_B~**	ØA
E	**FPWORK~**	**FPQ2**	FPDV2~	**RSEL_A~**	FPDV2~
F	KOPDE~	**FPQ2~**	FPDV2	**RSEL_M~**	FSUB
H	**FPDV2**	PLEND~	FPWORK	FPWORK~	ØA~
J	RKWZ~	KOPME~	FPML	**RSEL_K**	ØN
K	ØD15	ØN	FPQ1~	**RSEL_B**	FSUB~
L	ØN	FPDV2	ØN	**RSEL_A**	KR~
M	RAD_ROLL	FDA15R~	FPQ2~	**RSEL_M**	RAD_ROLL
N	V–12	V–12	V–12	V–12	V–12
P	GND	GND	GND	GND	GND
R	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5
S	DA15RE	**RBX_INC~**	**RA_INC~**	KRK~	**RM_INC~**
T	**FDA15R~**	MSCINC~	RBX_ROLL	KRB~	**MF_N**
U	**FDK15Z**	MSCEND~	**A_START~**	KRA~	RM_INCa~
V	**FPDV2~**	**FPML~**	**MSCINC~**	KRM~	FSM7a~
W	**PLINC~**	**SHIFTa**	**RBX_PLD2~**	FPDV2~	FPWORK~
X	-	-	ØD0	FPQ1~	FCYIN
Y	-	-	**#33**	#33	ØD0
Z	-	-	**PLINC~**	**RBX_CLR~**	ØN~

EMPTY

EMPTY

	N32	N31	N30	N29	N28	N27	N26	N25	N24	N23
A	-	-	KMUL~	-	-	-	**TFR_RB~**	-	-	**FSUB~**
B	**NXK0**	**DDP8**	**DDP8**	RK_W4	RK_W1	KRM~	**RBD_CLR~**	**ØDp**	**RKDW,XR~**	ØD0
C	**NXK1**	**DDP4**	**DDP4**	RK_W8	RK_W2	NEG~	**TFR_RA~**	**ØRp**	**RBDW,XR~**	ØA10
D	**NXK2**	**DDP2**	**DDP2**	-	-	KCLR_RK~	**RAD_CLR~**	**ØX**	SH0B1K	A_SETADD~
E	**NXK3**	**DDP1**	**DDP1**	-	-	**TFR_RK~**	**TFR_RK~**	**ØWp**	SHIFTa	A_SETSUB~
F	**NXK4**	RSEL_K~	RSEL_K	**RKWZ~**	**RKWZ~**	FSM2	**FSM2**	ØD0	**RBXW,DR~**	**RA_INC~**
H	**NXK5**	DPINC~	**DPINC~**	-	-	**FSM8**	FSM8	A_START~	**RKDR~**	**RM_INCa~**
J	**NXK6**	DPRDR~	**DPRDR~**	-	-	**FSM1p~**	FSM1p~	FØA8	#33	FPWORK
K	**NXK7**	ØN	ØN	**PLEND~**	**D1CEND~**	KTOT~	FDK15Za~	**ØA10**	**A_START~**	ØN~
L	**NXK8**	KDIV~	KDIV~	PLINC~	D1CINC~	FSM8p~	**FSM8p~**	**ØN**	ØD~	**A_START~**
M	**NXK9**	KC~	KC~	DA15RE	-	KIM~	**RBX_CLR~**	**ØD**	KOPAS~	**FCYIN**
N	V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12	V–12
P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
R	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5	V+4.5
S	V–100	-	V+100	**FØA8**	**MSCEND~**	**RKX_CLR~**	RSEL_A~	**ØA**	KOP~	-
T	DD1	**DD1**	KP~	KC~	KC~	RSEL_K~	RSEL_K~	-	SYNC~	ØA~
U	DD2	**DD2**	KNML~	ØA10	MSCINC~	**RKD_CLR~**	KMUL~	**ØN~**	KN~	RAD_ROLL
V	DD4	**DD4**	KR~	-	-	**RMD_CLR~**	KR~	**ØA~**	**FPWORK~**	RMD_ROLL
W	DD8	**DD8**	**NXADP**	FPDV2	FDK15Z	**TFR_RM~**	RSEL_B~	**ØD~**	**FPWORK**	RKD_ROLL
X	-	-	-	-	-	**FSM7a~**	KNn~	-	**KNML~**	**FSUB**
Y	-	-	ØD	**{KC~(29)}**	**{KC~(28)}**	**KME~**	**KRK~**	-	-	MF_FCT
Z	-	-	-	-	-	FSM6p~	**FSM6p~**	-	KC~	**MF_GT**

N1

1	**RK_S1~**
2	**RB_S1~**
3	**RK_S2~**
4	**RB_S2~**
5	**RK_S4~**
6	**RB_S4~**
7	**RK_S8~**
8	**RB_S8~**
9	**DD8**
10	**DD4**
11	**DD2**
12	**DD1**
13	RSEL_B
14	RSEL_K
15	RSEL_A
16	RSEL_M
17	RK_W1
18	RB_W1
19	RA_W1
20	RM_W1
21	RK_W2
22	RB_W2
23	RA_W2
24	RM_W2
25	RK_W4
26	RB_W4
27	RA_W4
28	RM_W4
29	RK_W8
30	RB_W8
31	RA_W8
32	RM_W8
33	V–12
34	GND
35	**RM_S8~**
36	**RA_S8~**
37	**RM_S4~**
38	**RA_S4~**
39	**RM_S2~**
40	**RA_S2~**
41	**RM_S1~**
42	**RA_S1~**
43	TFR_RM~
44	TFR_RA~
45	TFR_RB~
46	TFR_RK~

NK

1	**KN1~**
2	**KN2~**
3	**KN4~**
4	**KN8~**
5	**KN~**
6	**KP~**
7	**RMD_CLR~**
8	**RBD_CLR~**
9	**RBX_CLR~**
10	**RAD_CLR~**
11	**KC~**
12	**RKD_CLR~**
13	**RKX_CLR~**
14	**KRK~**
15	**A_SETADD~**
16	FPQ1~
17	FPDV2~
18	FPQ2
19	FSM7a~
20	**KOPAS~**
21	**KOP~**
22	**KASD~**
23	**KR~**
24	**A_SETSUB~**
25	**KDIV~**
26	**TFR_RK~**
27	**TFR_RA~**
28	RSEL_A~
29	**KTOT~**
30	RSEL_K~
31	**KRA~**
32	MF_N
33	**MF_FCT**
34	MF_GT
35	**KOPDE~**
36	**KOPME~**
37	GND
38	V–12
39	**KRB~**
40	**KRM~**
41	**KMUL~**
42	**KNn~**
43	**KRM~**
44	**KIM~**
45	RSEL_M~
46	RSEL_B~

NN

1	NXADP
2	NXK6
3	NEG~
4	V–12
5	NXK5
6	NXK7
7	NXK4
8	NXK8
9	NXK3
10	NXK9
11	NXK2
12	NXK1
13	NXK0
14	NXA0
15	NXA1
16	NXA2
17	NXA3
18	NXA4
19	NXA5
20	NXA6
21	NXA7
22	NXA8
23	NXA9
24	NXA10
25	NXA11
26	NXA12
27	NXA13
28	NXA14
29	NXA15
30	OVF~
31	V–12

NP

V–12	1		
V–4.5	2	9	MTEMP
V–100	3	10	-
V+4.5	4	11	-
V+100	5	12	**GND**
V–2.6	6	13	**GND**
LINE1	7	14	LINE2
LINE1	8	15	LINE2

Board Types & Contents

Board	Type	Content	Transistors	Diodes
1	64	transfer gates, display select	0	64
2	66	RM decade counter	9	32
3	66	RA decade counter	9	32
4	66	RB decade counter	9	32
5	66	RBX decade counter	9	32
6	66	RK decade counter	9	32
7	68	RKX decade latch	10	27
8	70	RM core drive & sense	16	16
9	70	RA core drive & sense	16	16
10	70	RB core drive & sense	16	16
11	70	RK core drive & sense	16	16
12		core array	0	0
13	72	digits 0::3 core drive & nixie anode drive	20	44
14	72	digits 4::7 core drive & nixie anode drive	20	44
15	72	digits 8::11 core drive & nixie anode drive	20	44
16	72	digits 12::15 core drive & nixie anode drive	20	44
17	74	timing: digit counter ØDC	9	40
18	76	ctl: FOVF, FNEG, FNEGH, FNINC	15	29
19	78	current-register latch: FRS1,2	12	30
20	80	ctl: FBXLD, FMBXR	9	29
21	82	ctl: FPML, FPQ1,2	8	30
22	84	ctl: FPDV2, FPDV1, FDK15Z, FDA15R	12	21
23	86	arithmetic: FSUB, FCYIN, FRKR, FRACY, FRMCY	10	38
24	88	ctl: FPST, FPWORK, FPAS, FSHLF	14	31
25	90	timing: master clock ØM, FØA, FØC1,2	15	20
26	92	ctl: sequencer FSM1::5	10	33
27	94	ctl: sequencer FSM6::10	10	15
28	96	double counter: MSC DIV10, D1C DIV16	16	22
29	96	double counter: ØAC DIV10, PLC DIV16	16	22
30	98	DPK counter	13	31
31	100	DPR counter	11	39
32	102	nixie numeral decoder & cathode drivers	18	44
K	108	keyboard conditioning	0	48
KD	2-56-0030	keyboard daughter board	3	21
N	120	nixie display	0	0
P1	111	power supply	3	4
P4	114	power supply	4	3
chassis	-	power supply	1	4
			Total: 408	1045

Section	Signal	Description
Timing	ØM	Master clock.
	ØWp	Core Write pulse.
	ØRp	Core Read pulse.
	ØX	Nixie ON period.
	ØA	A period of arithmetic counting within an extended digit period.
	ØA10	Sequence of 10 pulses of ØM during ØA, for arithmetic counting.
	ØD	Digit clock.
	ØDA,B,C,D	1-of-4 Major decoding of the ØD Counter.
	ØDa,b,c,d	1-of-4 minor decoding of the ØD Counter.
	ØD0	LSD digit period.
	ØD15	MSD digit period.
	ØN	A digit cycle in-between number cycles.
Keyboard	K…	Keyboard signals.
	KN1,2,4,8	BCD-encoded numeral keys.
	KOP…	
	RSEL_*r*	Currently-selected register (per keyboard).
Control	FSM1..10	Sequencer State Machine outputs.
	FPSYNC	Processing Sync.
	FPWORK	Processing at work.
	FPAS	Performing Addition/Subtraction.
	FPML	Performing Multiplication.
	FPDV1	Performing Division, stage 1.
	FPDV2	Performing Division, stage 2.
	FPL1,2,4,8	Primary Loop counter for Multiplication & Division.
	FPQ1,2	Primary Loop Sequence Counter.
	FSHLF	Shifting Leap-Frog toggle.
	FBXLD	Special enable for core load into RBX.
	FMS1,2,4,8	MS Counter. During Multiplication, count additions of the multiplier to the product.
	FMBXR	During Multiplication, decade RBX Rolled over.
	FD11,2,4,8	D1 Counter. During Division, count stage 1 progress.
	FDK15Z	During Division, RK digit 15 is Zero.
	FDA15R	During Division, digit 15 of RA Rolled over.
	SHIFT	Enable logic for a register shift.

Section	Signal	Description
Registers	RK…	Keyboard entry register.
	RB…	Register for multiplier and quotient.
	RA…	Accumulator register.
	RM…	User memory register.
	R*r*D…	Decade counter for register.
	R*r*X…	Secondary decade for registers RK and RB.
	R*rd*_CLR	Clear register r decade.
	R*rd*_INC	Increment register decade counter.
	R*rd*_PLD	Enable loading of register decade during core read (enable receipt of sense pulses).
	R*rd*_WEN	Enable write to core from register decade.
	R*rd*_ROLL	Roll-over indication from register decade.
	TFR_Rr~	Enable register onto transfer bus.
Arithmetic	A_START~	The –edge of this signal extends the current digit period for an arithmetic cycle.
	A_SETADD~	Select addition for following arithmetic cycles.
	A_SETSUB~	Select subtraction for following arithmetic cycles.
	FSUB	Flag indicating subtract rather than add.
	FCYIN	A brief period at the beginning of a digit period during which the register counter may be incremented for carry from the prior digit, before increments from add/subract of the digit.
	FRKR	Roll-over flag for RK.
	FRACY	Carry flag for RA..
	FRMCY	Carry flag for RM.
	FNEG	Negative sign flag.
	FNEGH	Negative Hold flag.
	FOVF	Overflow flag.
	MPPAE	Multiplication Partial Product Add Enable.
Decimal Point	FDPK1,2,4,8	Decimal point position counter for entered number (K Register).
	FDPR1,2,4,8	DP counter for other registers.
	FDPKE	Enable FDPK counting.
	FDPRD	Count-up/down selector for FDPR counter.