IME 86S
Calculator

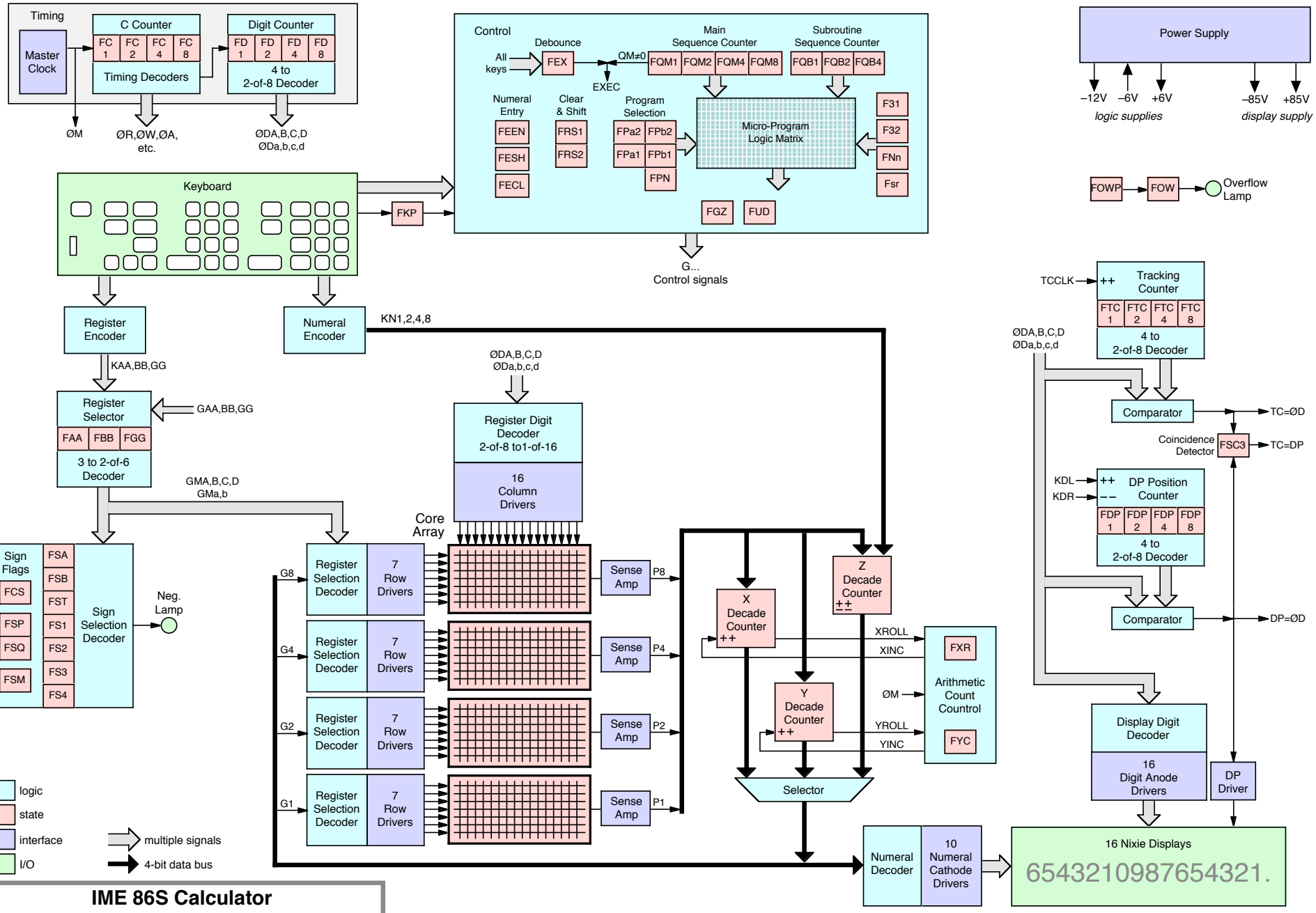
Contents

Notes

- Gate symbols and signal names are presented in accordance with:
  logic 0 = 0V, GND
  logic 1 = –12V
- The symbol N*bb,pp* denotes a physical connector pin. *bb*=board, *pp*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- Arrows indicate direction of signal or energy flow.
- The symbol with no label denotes –12V.
- The symbol with no label denotes +6V.
- These drawings are a redrawing and interpretation to logic of the original IME discrete-component schematic, with additional information from J.Ongena from examination of Unit 51409751.
- Assorted connections to the Remote Connector are not shown in these drawings.

Revision Log

- 2024 Aug: Initial drawing / bhilpert.
- TO DO: - Enumerate gates.



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Section: Block Diagram

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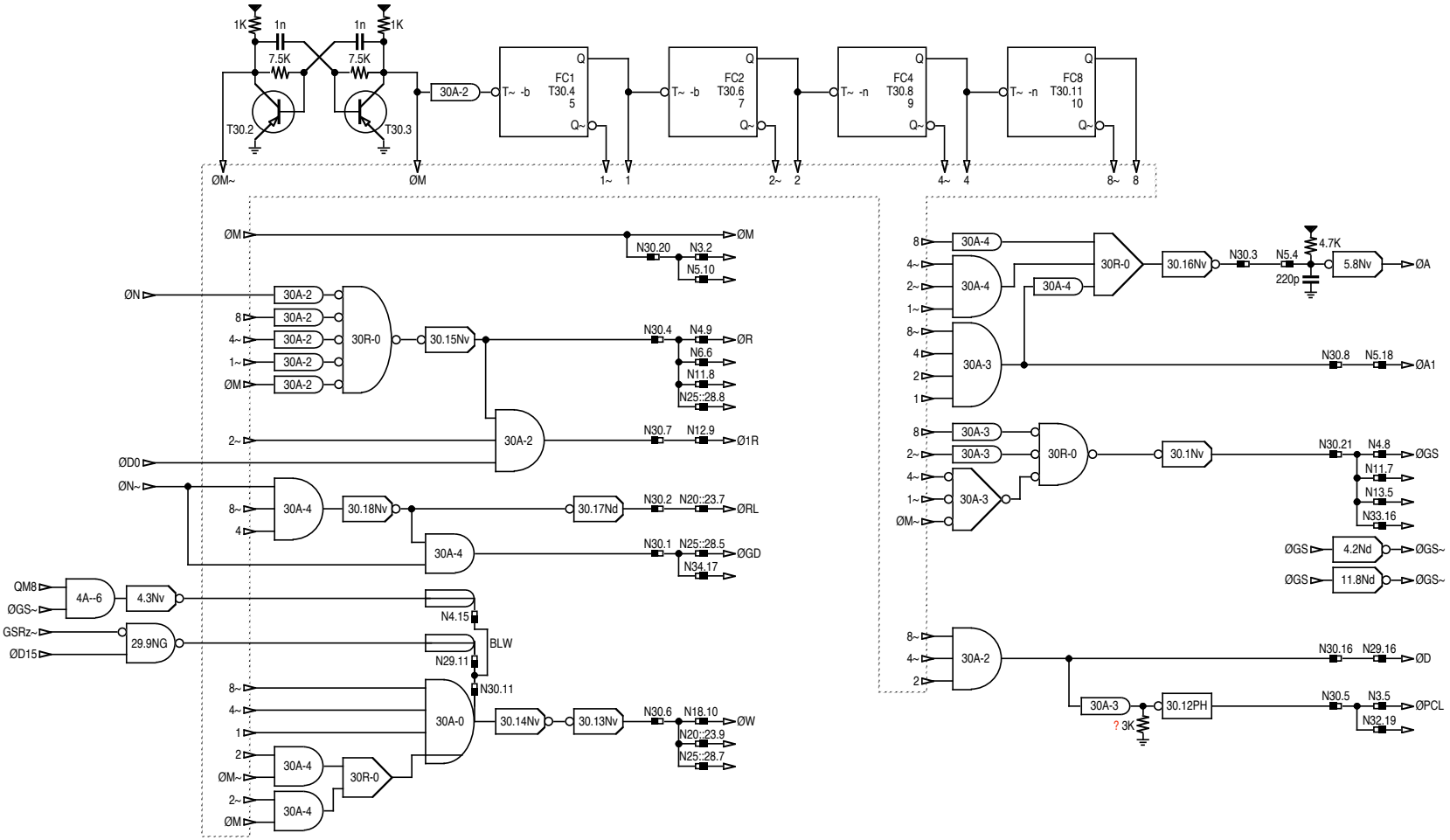

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Section: Timing

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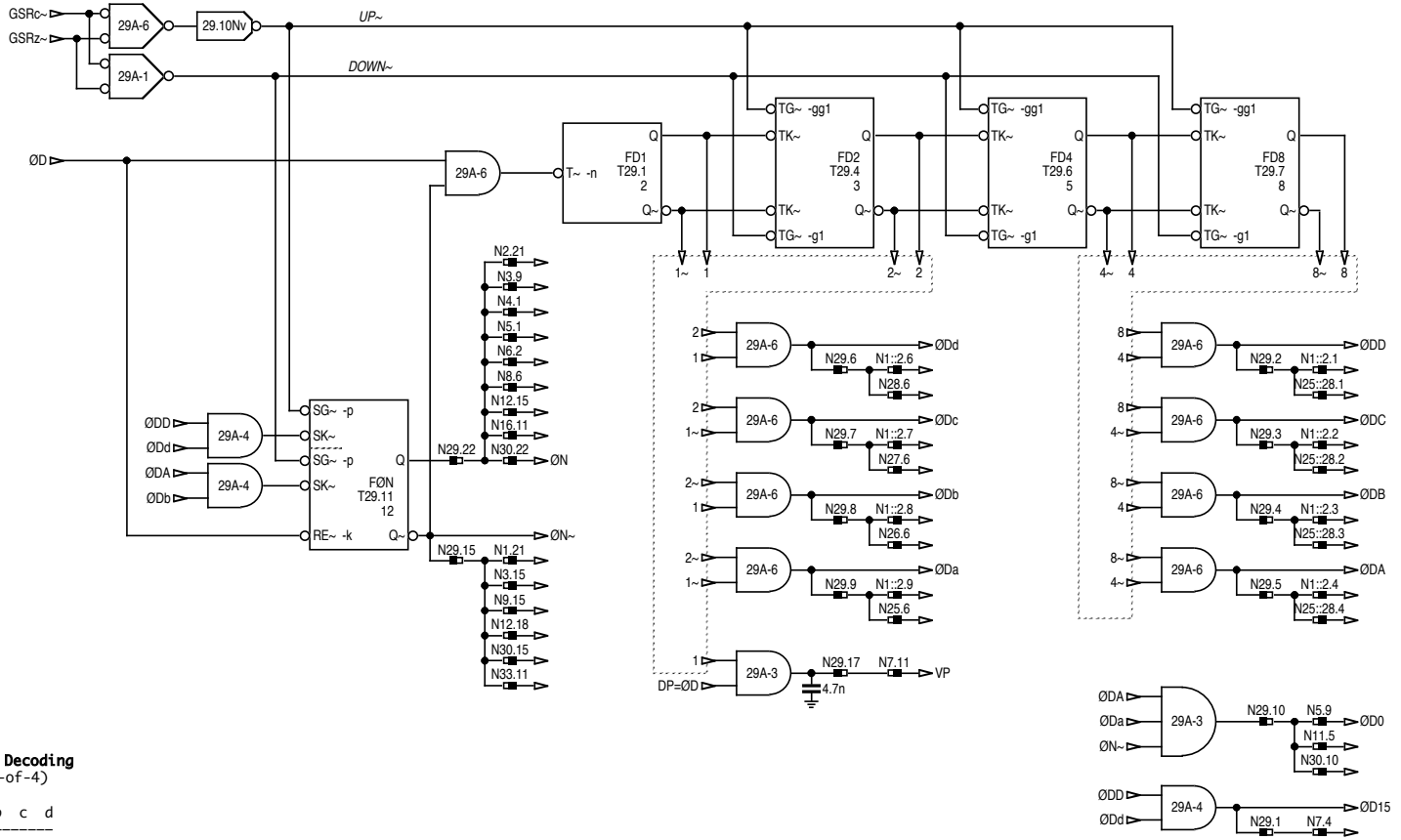
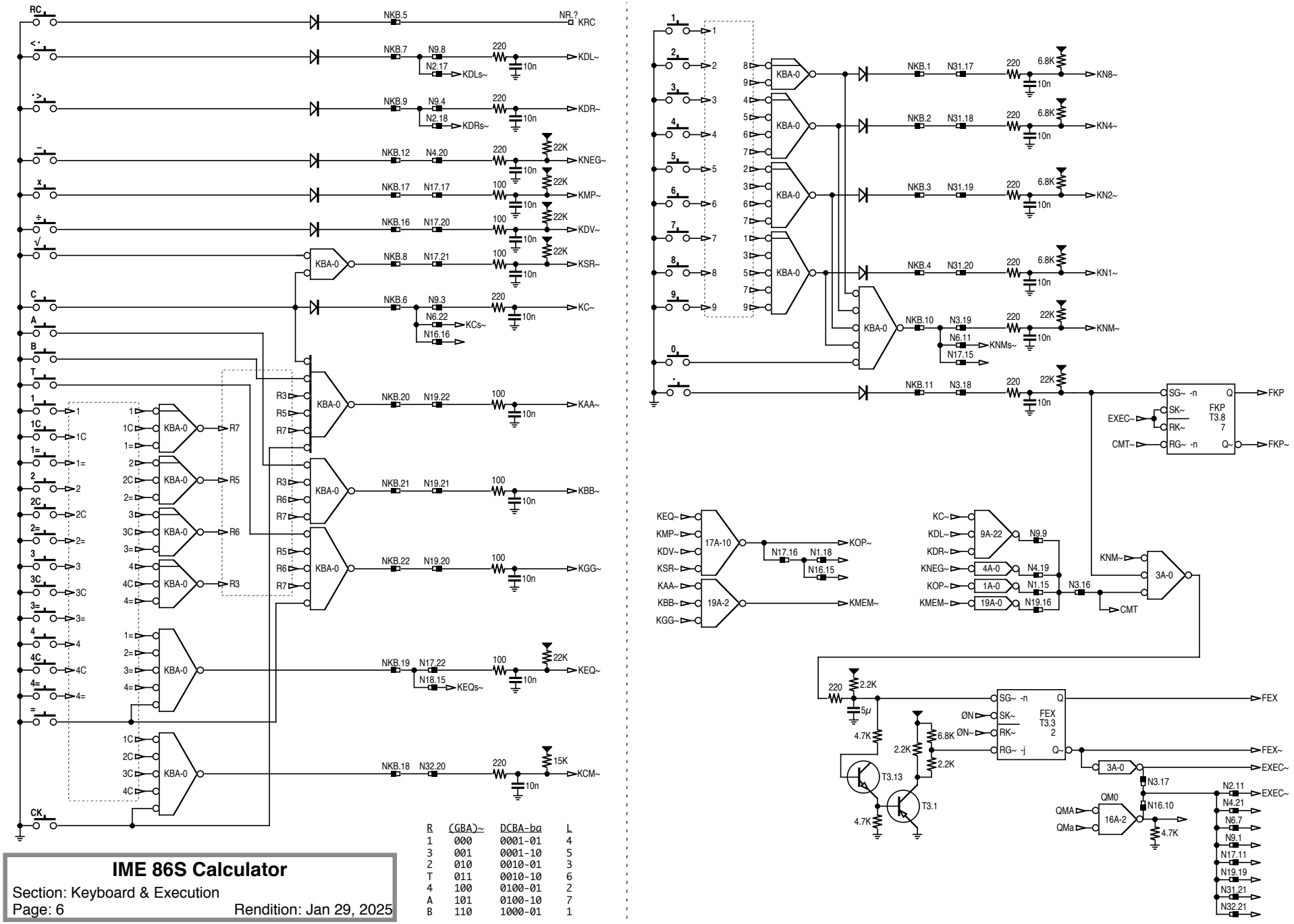


Major-minor Decoding
2 ● (1-of-4)

	a	b	c	d
A	0	1	2	3
B	4	5	6	7
C	8	9	10	11
D	12	13	14	15



R	(GBA)~	DCBA-ba	L
1	000	0001-01	4
3	001	0001-10	5
2	010	0010-01	3
T	011	0010-10	6
4	100	0100-01	2
A	101	0100-10	7
B	110	1000-01	1

IME 86S Calculator

Section: Keyboard & Execution

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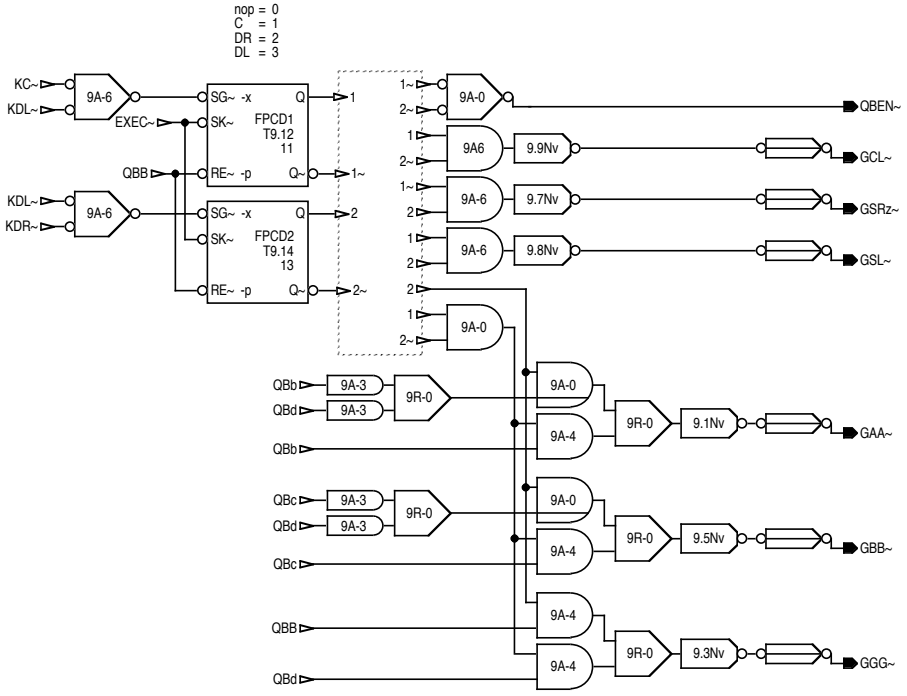
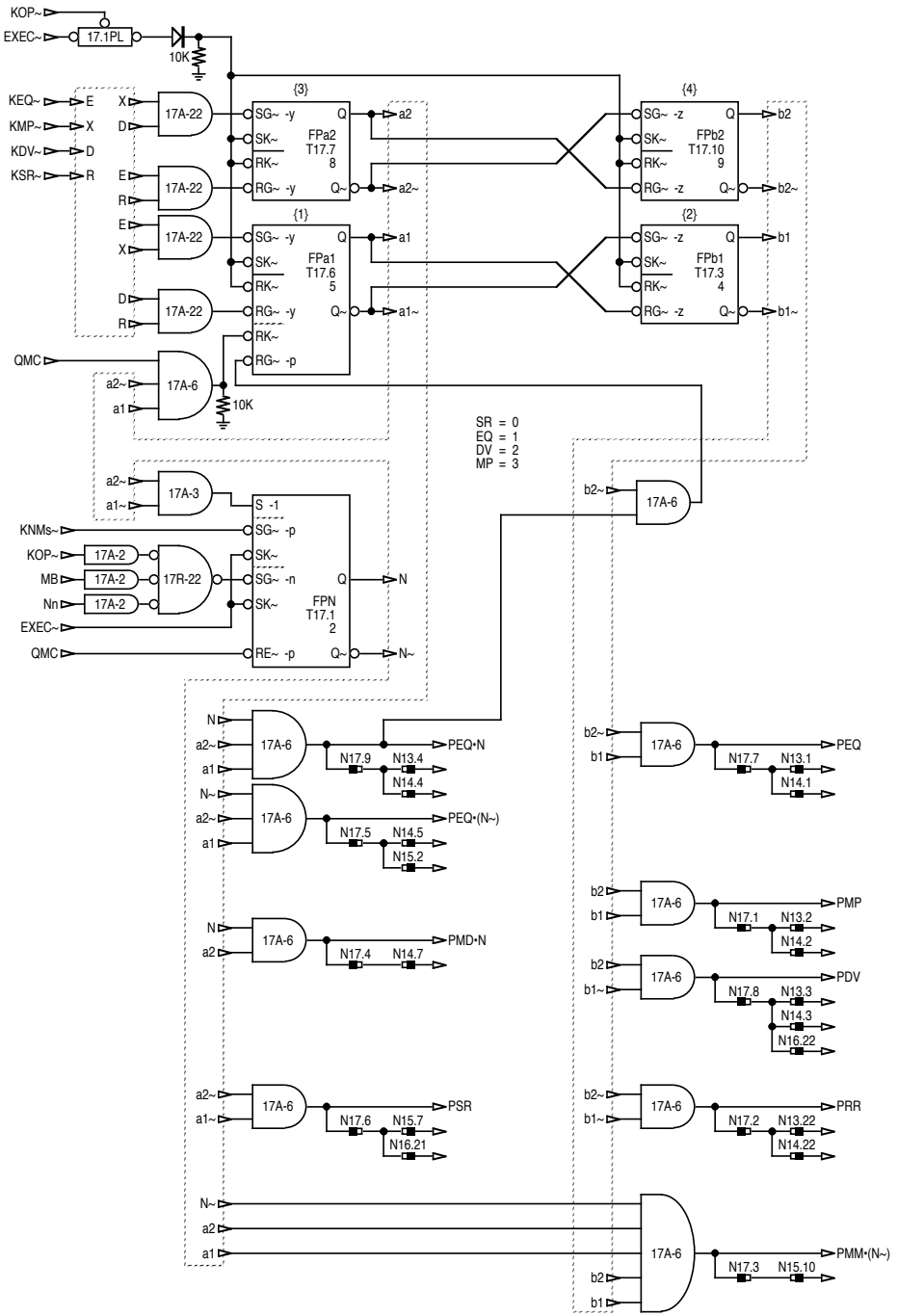
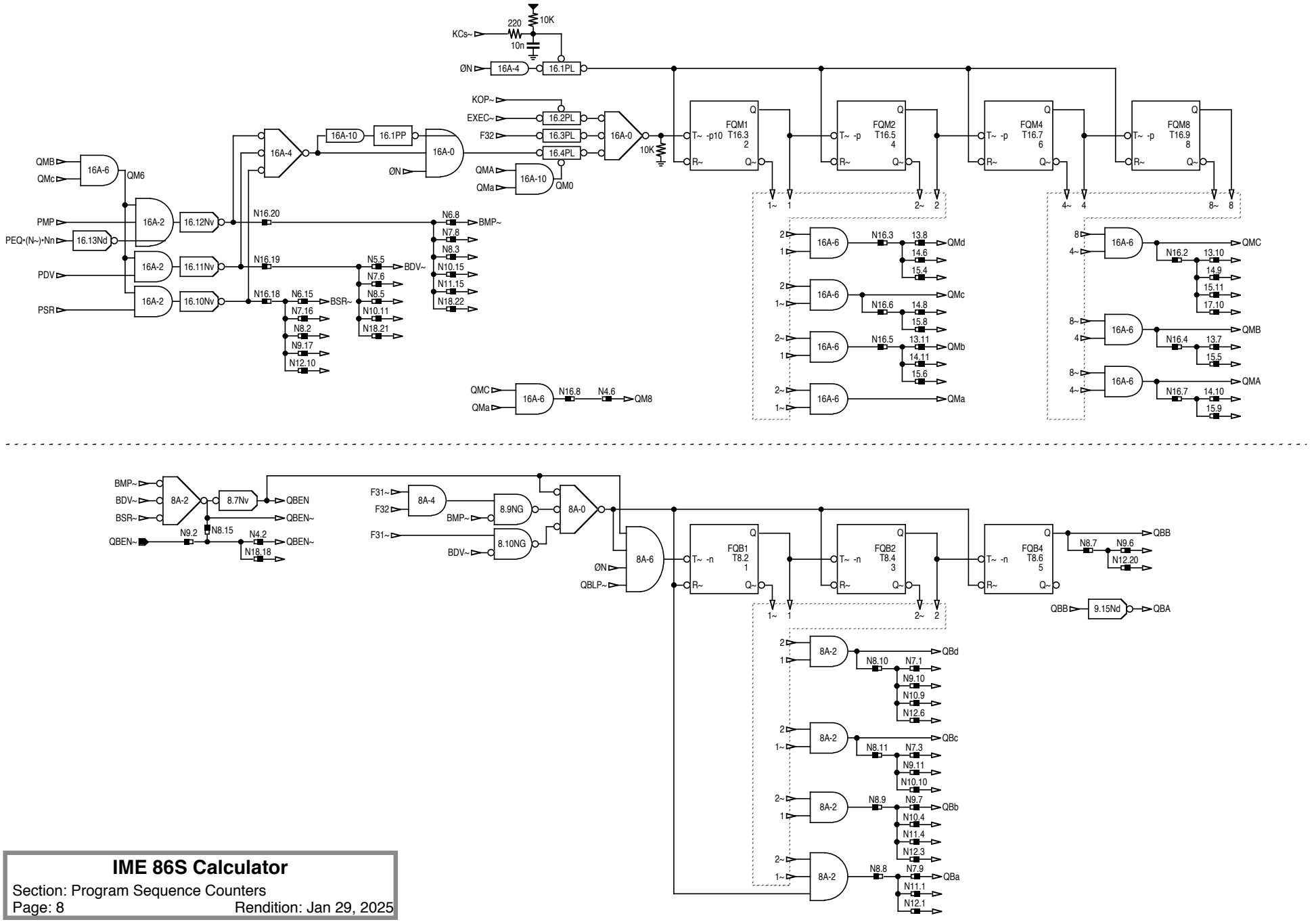

nop = 0
C = 1
DR = 2
DL = 3
KC~
KDL~
9A-6
EXEC~
SG~ -x
SK~
RE~ -p
Q
FPCD1
T9.12
11
QBB
KDL~
KDR~
9A-6
FPCD2
T9.14
13
1~
2~
9A-0
QBEN~
9A6
9.9Nv
GCL~
9.7Nv
GSRz~
9.8Nv
GSL~
QBb
QBd
9A-3
9R-0
9A-4
9.1Nv
GAA~
QBc
9.5Nv
GBB~
9.3Nv
GGG~


KOP~
EXEC~
17.1PL
10K
KEQ~
KMP~
KDV~
KSR~
17A-22
{3}
FPa2
T17.7
8
{4}
FPb2
T17.10
9
{1}
FPa1
T17.6
5
{2}
FPb1
T17.3
4
QMC
17A-6
SR = 0
EQ = 1
DV = 2
MP = 3
17A-3
KNMs~
17A-2
17R-22
Nn
FPN
T17.1
2
N17.9
N13.4
N14.4
PEQ•N
N17.5
N14.5
N15.2
PEQ•(N~)
N17.4
N14.7
PMD•N
N17.7
N13.1
N14.1
PEQ
N17.1
N13.2
N14.2
PMP
N17.8
N13.3
N14.3
N16.22
PDV
N17.6
N15.7
N16.21
PSR
N17.2
N13.22
N14.22
PRR
N17.3
N15.10
PMM•(N~)



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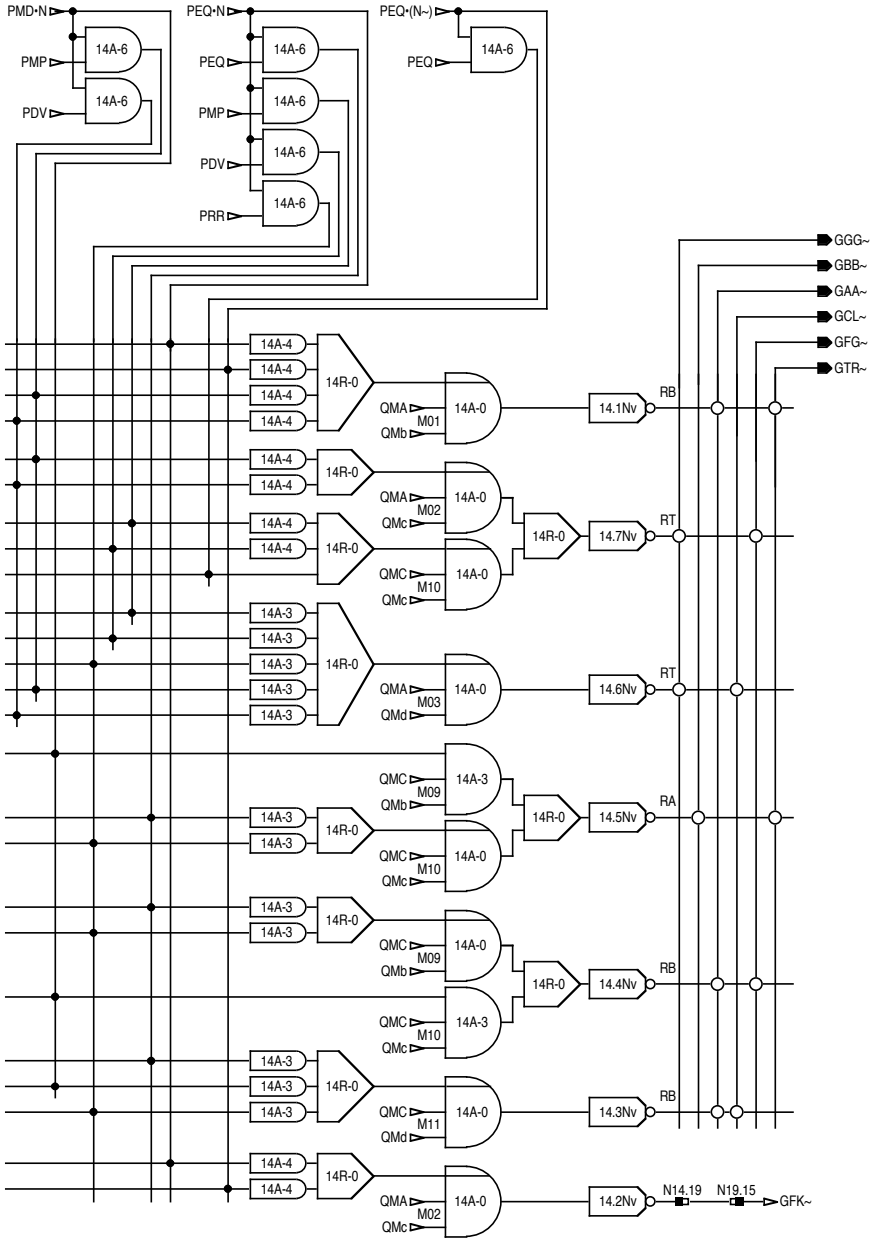
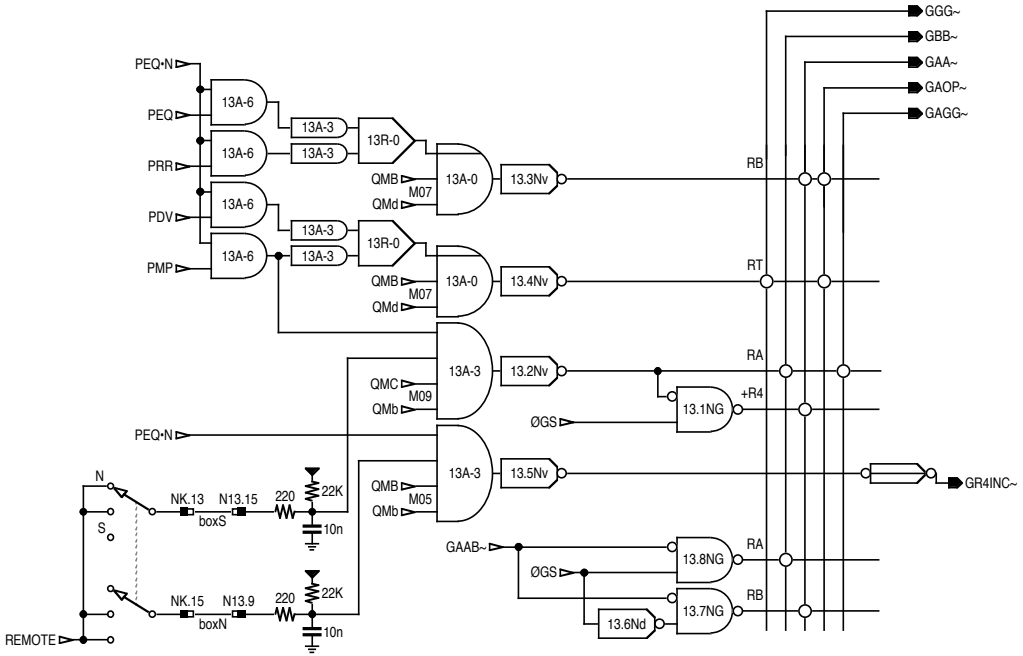
Section: Program Sequence Counters

 Rendition: Jan 29, 2025



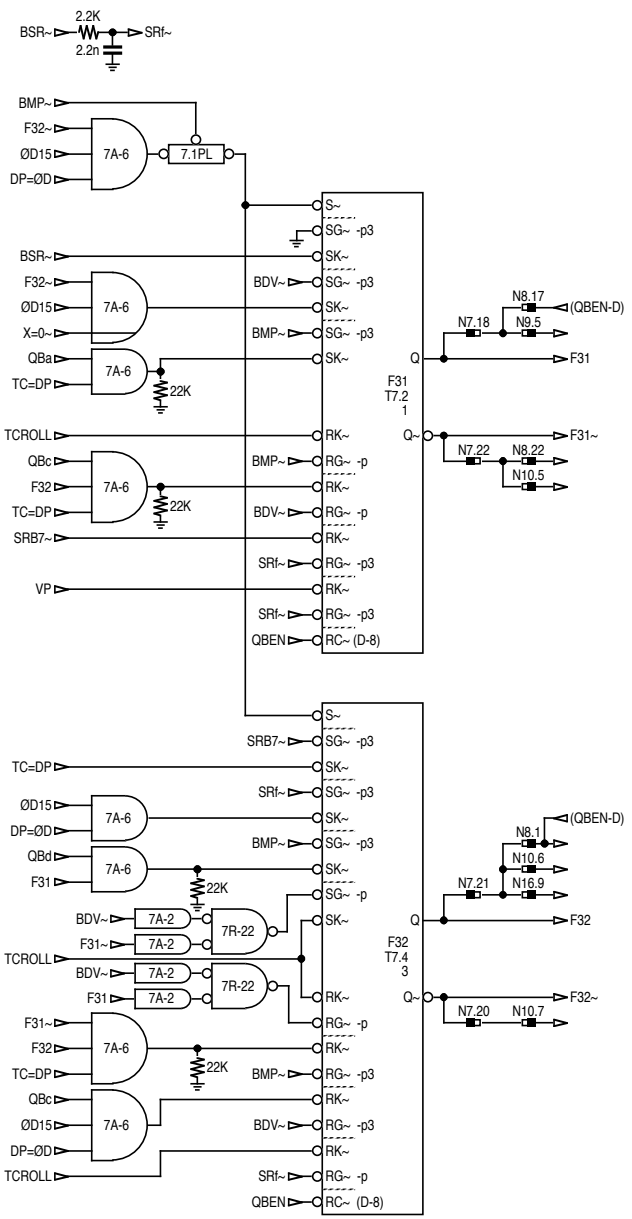


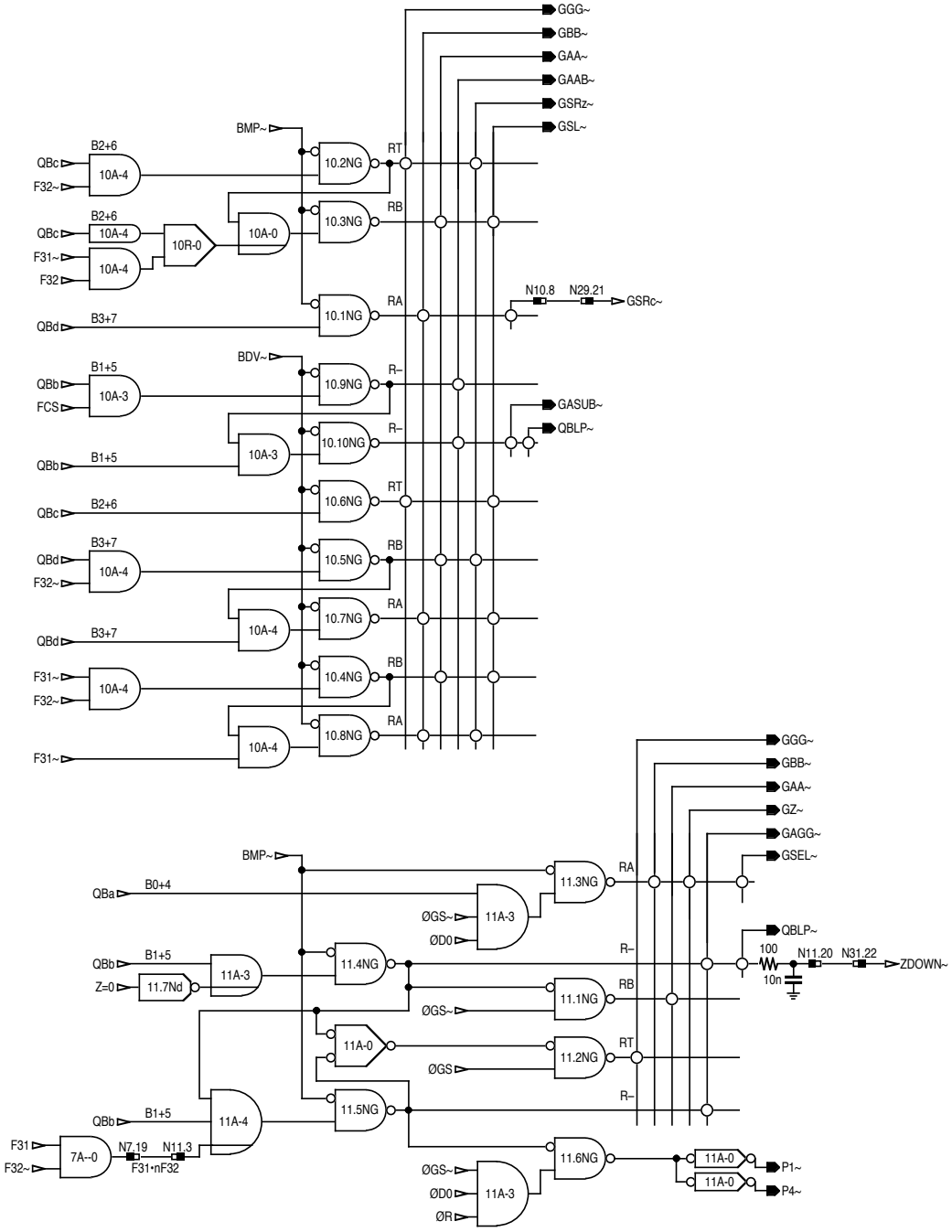
	a	b	c	d
A	0	1	2	3
B	4	5	6	7
C	8	9	10	11
D	12	13	14	15

IME 86S Calculator

Section: Programs EQ/MP/DV

Rendition: Jan 29, 2025





IME 86S Calculator

Section: F31 & F32, Sub MP/DV

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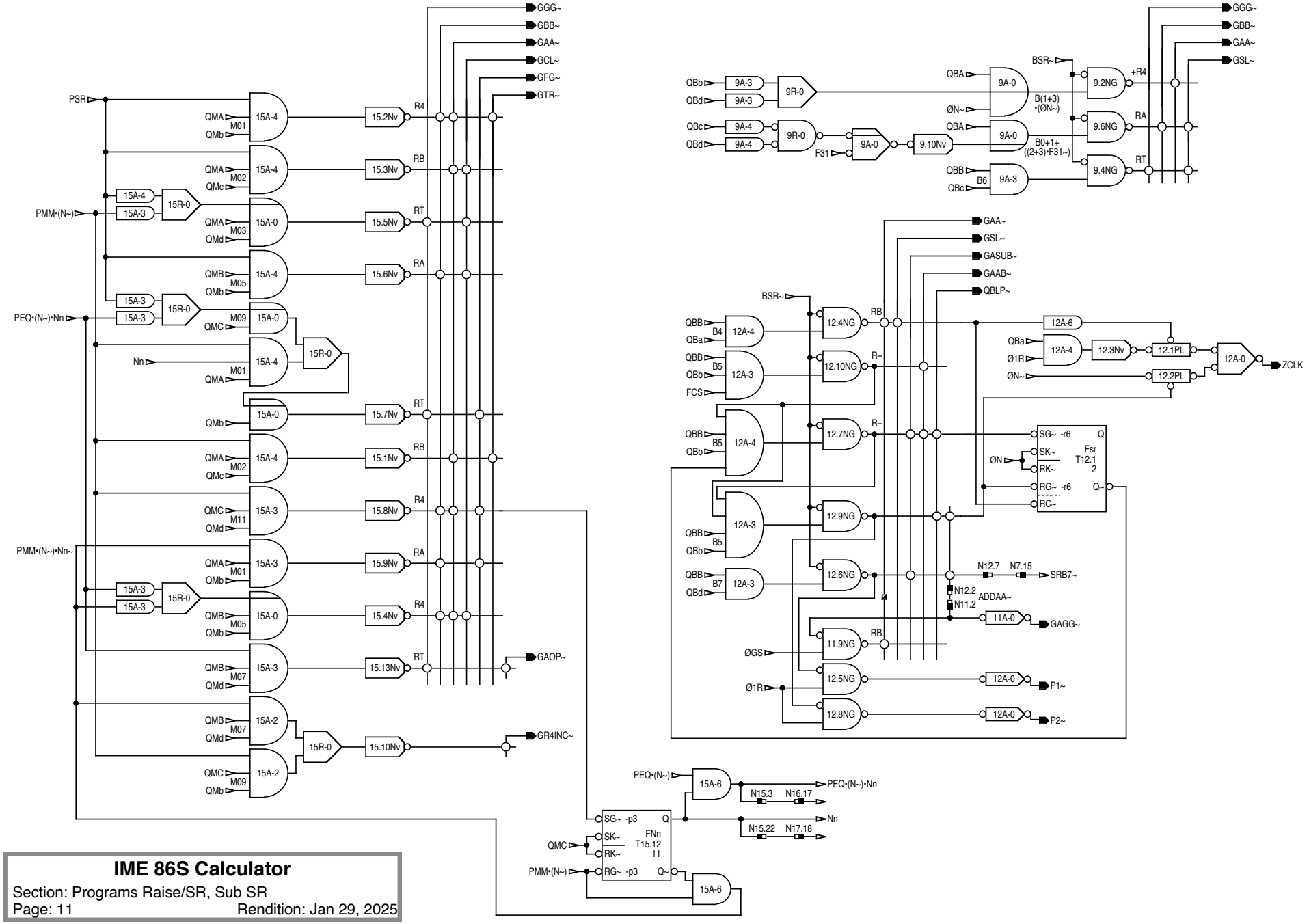

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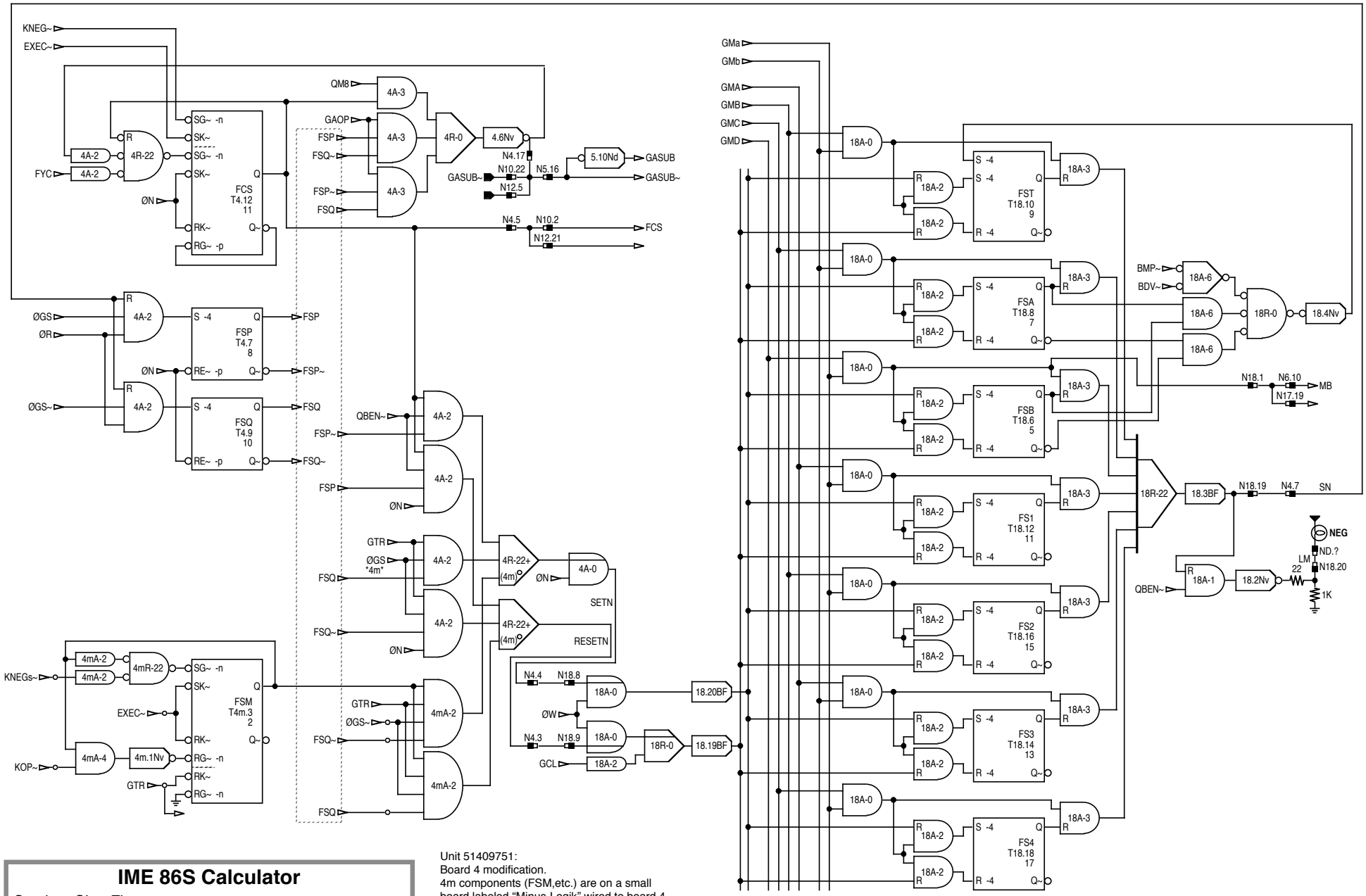
Section: Programs Raise/SR, Sub SR

 Rendition: Jan 29, 2025



Unit 51409751:
Board 4 modification.
4m components (FSM,etc.) are on a small board labeled “Minus-Logik” wired to board 4.
4m ØGS input diodes are on board 4 but are part of this modification.

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Section: Sign Flags
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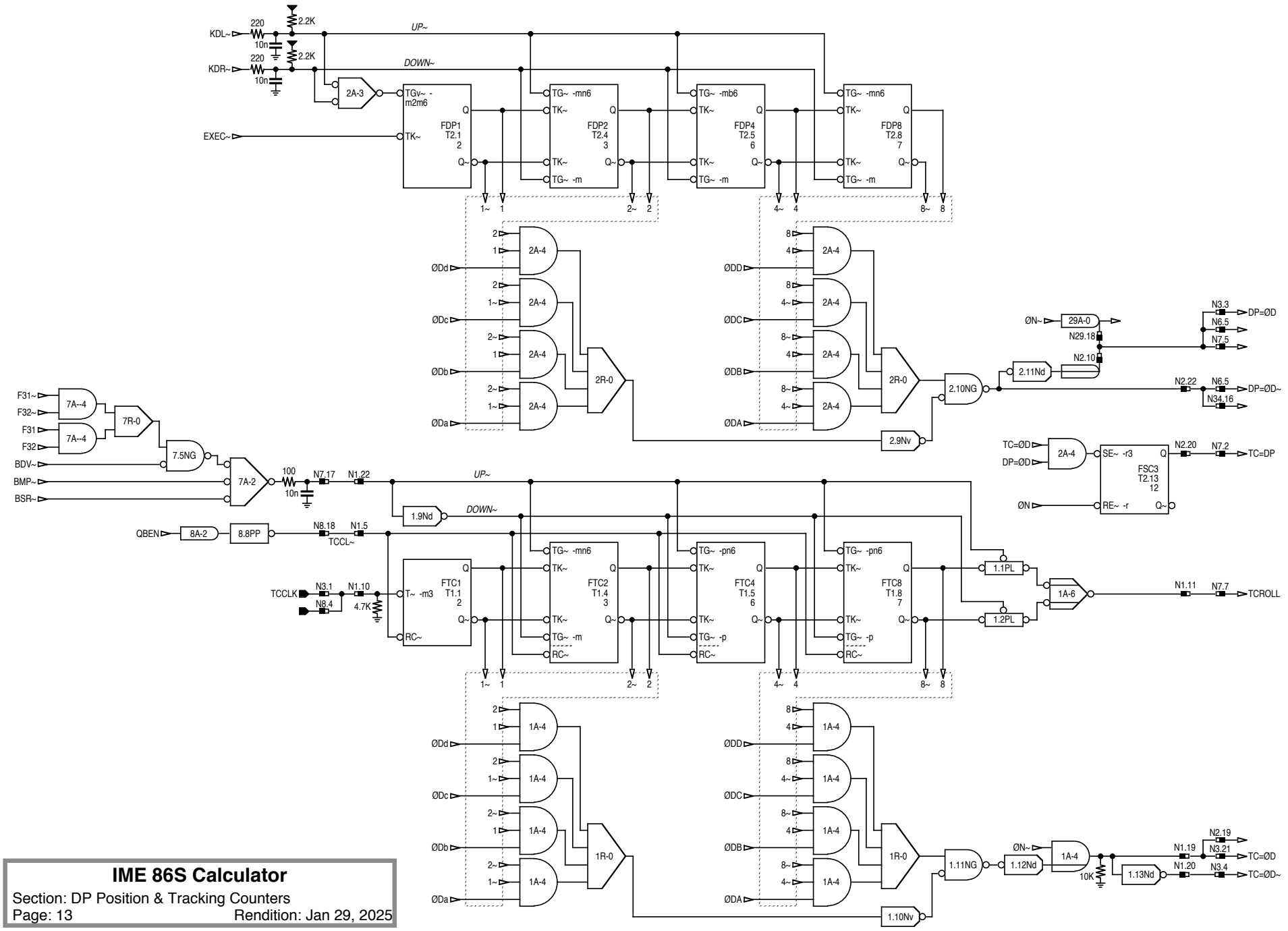

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Section: DP Position & Tracking Counters

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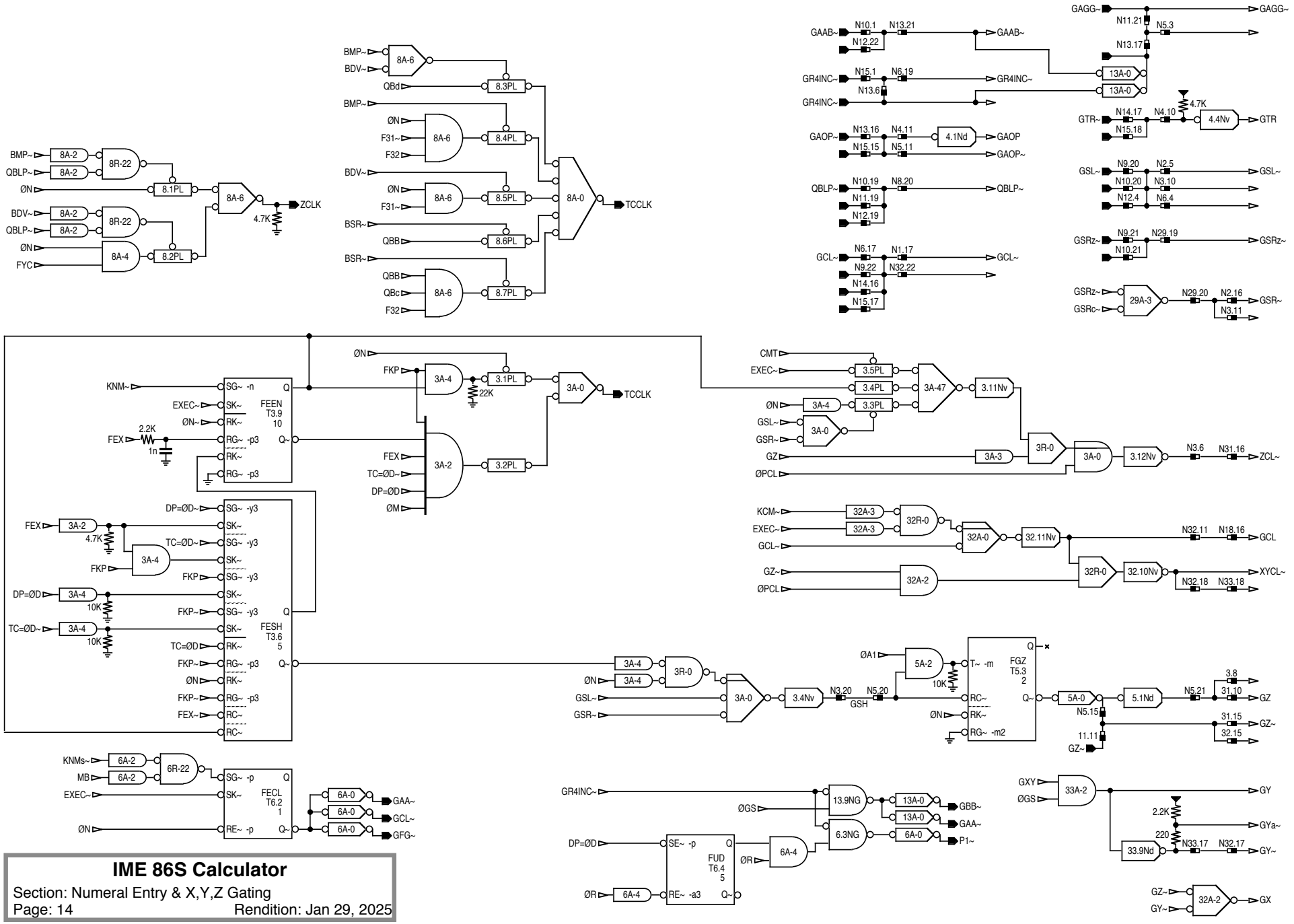
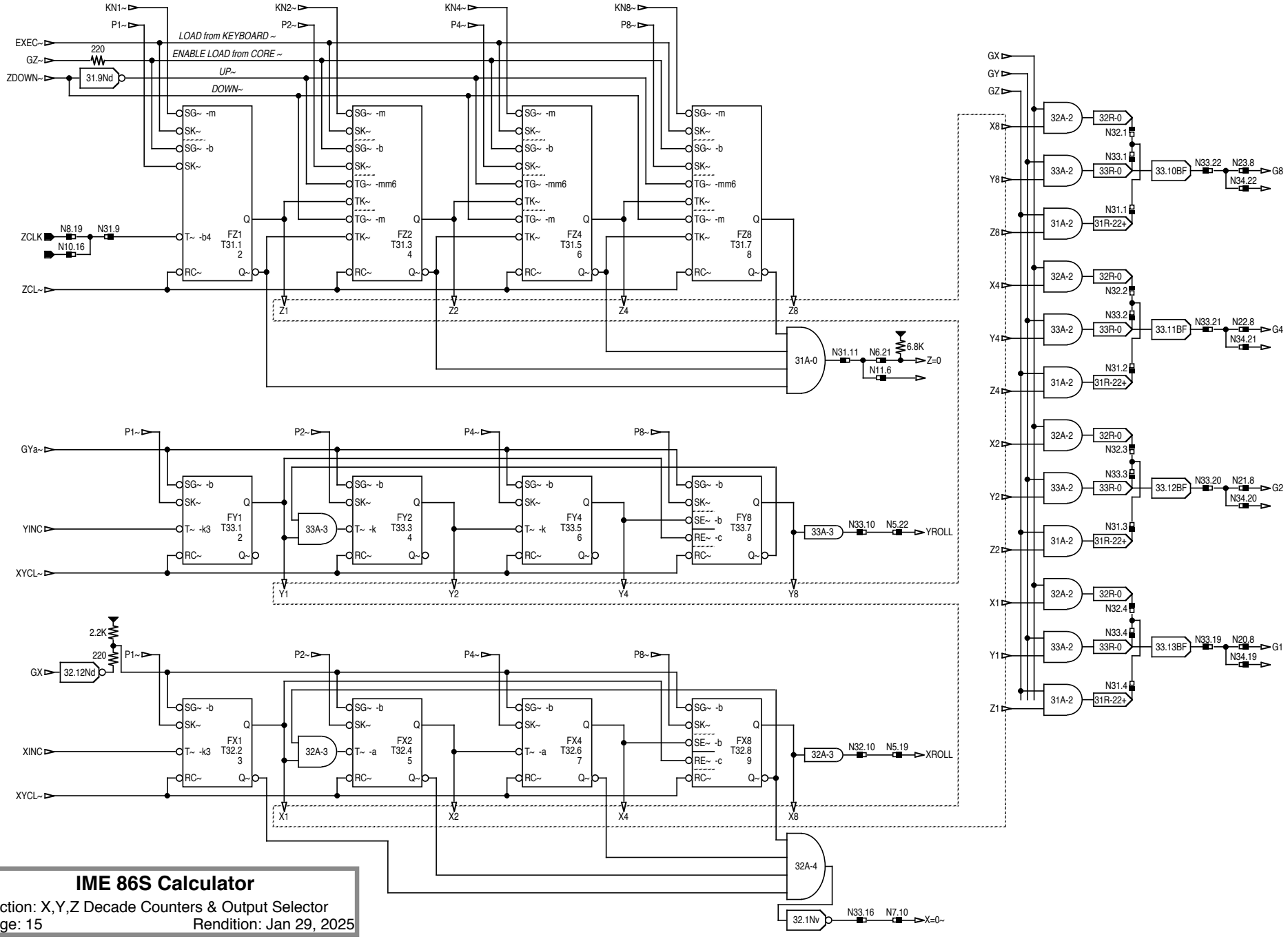


IME 86S Calculator

Section: Numeral Entry & X,Y,Z Gating

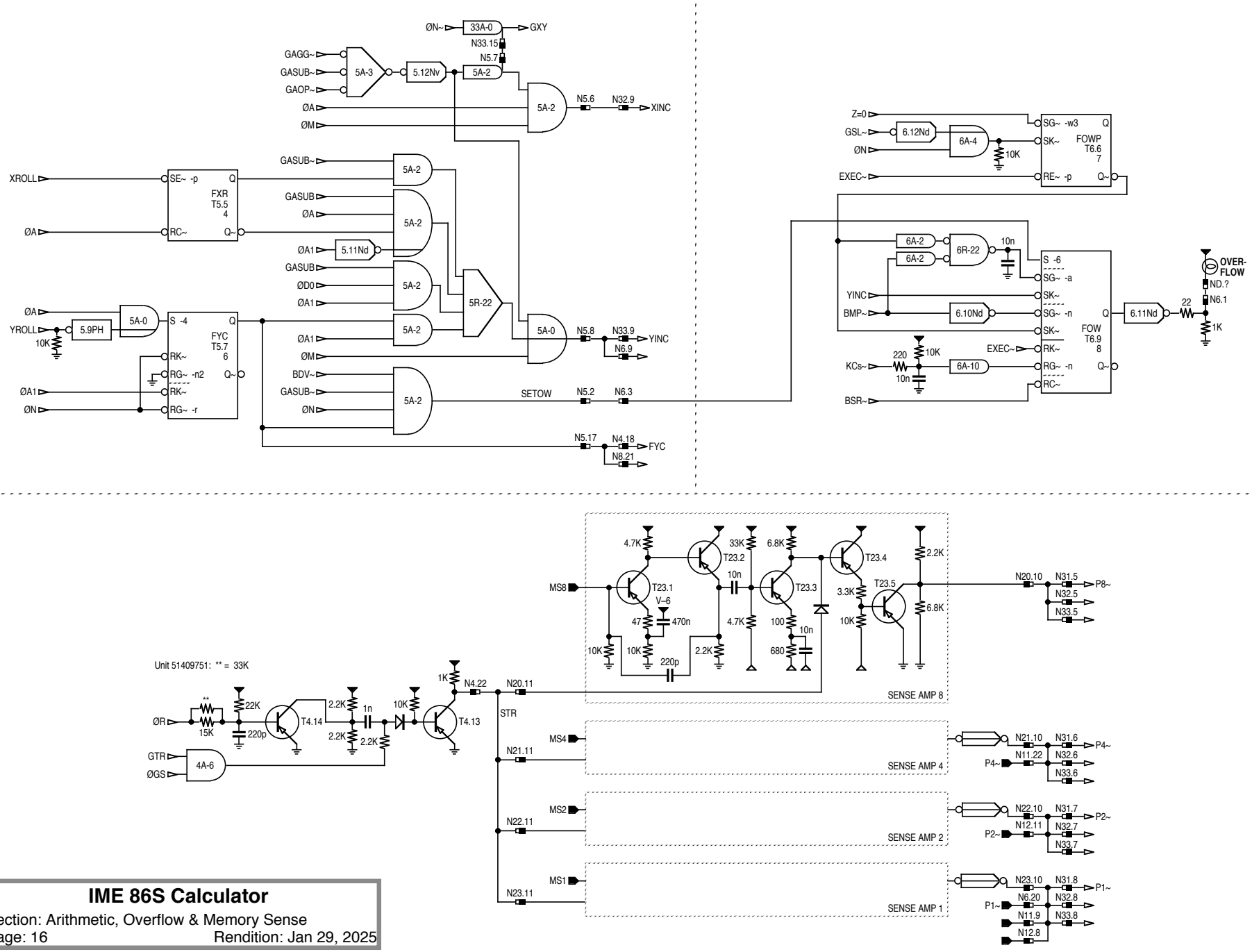
Page: 14 Rendition: Jan 29, 2025



IME 86S Calculator

Section: X,Y,Z Decade Counters & Output Selector

Page: 15 Rendition: Jan 29, 2025



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Section: Arithmetic, Overflow & Memory Sense

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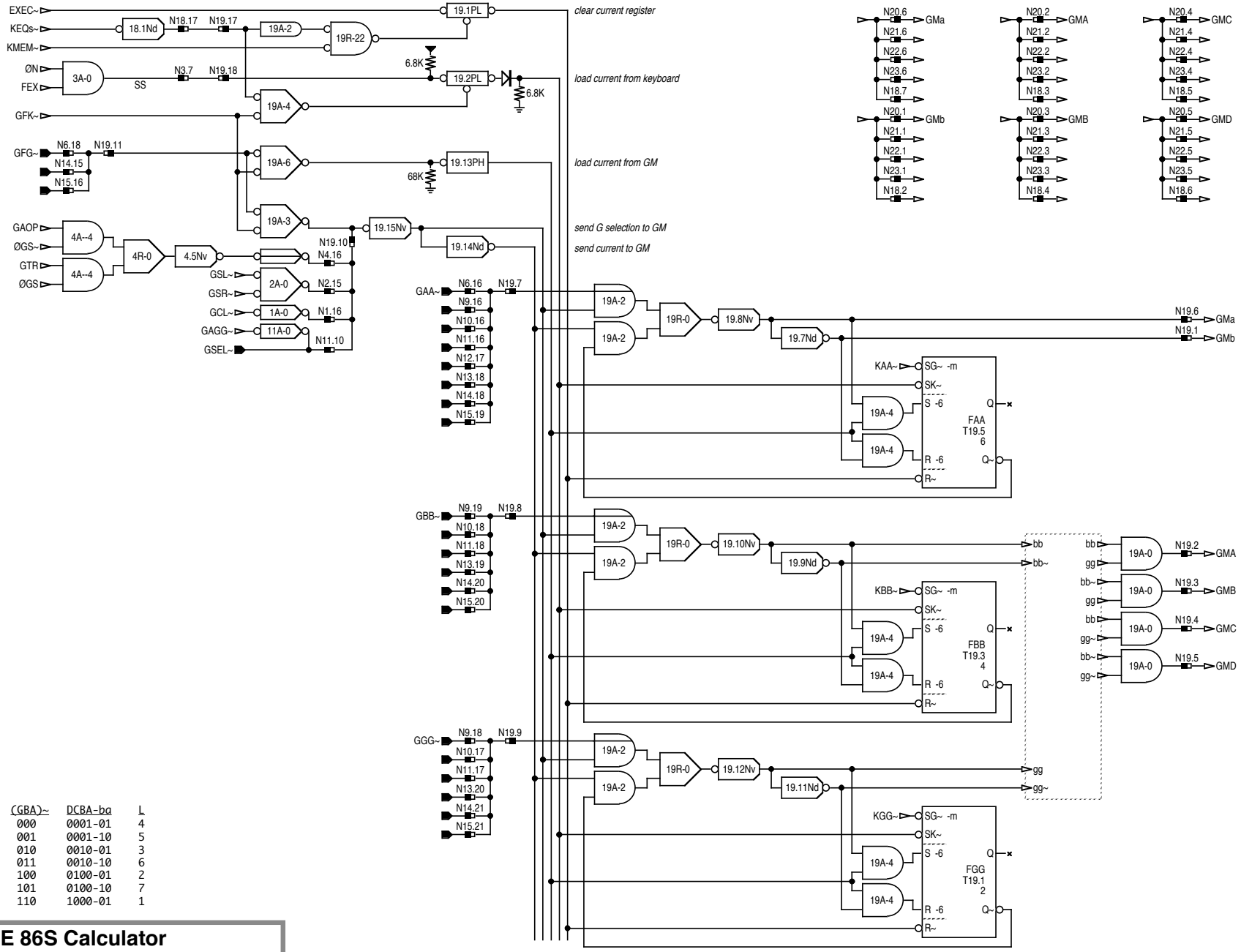

R	(GBA)~	DCBA-ba	L
1	000	0001-01	4
3	001	0001-10	5
2	010	0010-01	3
T	011	0010-10	6
4	100	0100-01	2
A	101	0100-10	7
B	110	1000-01	1

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Section: Memory Selector

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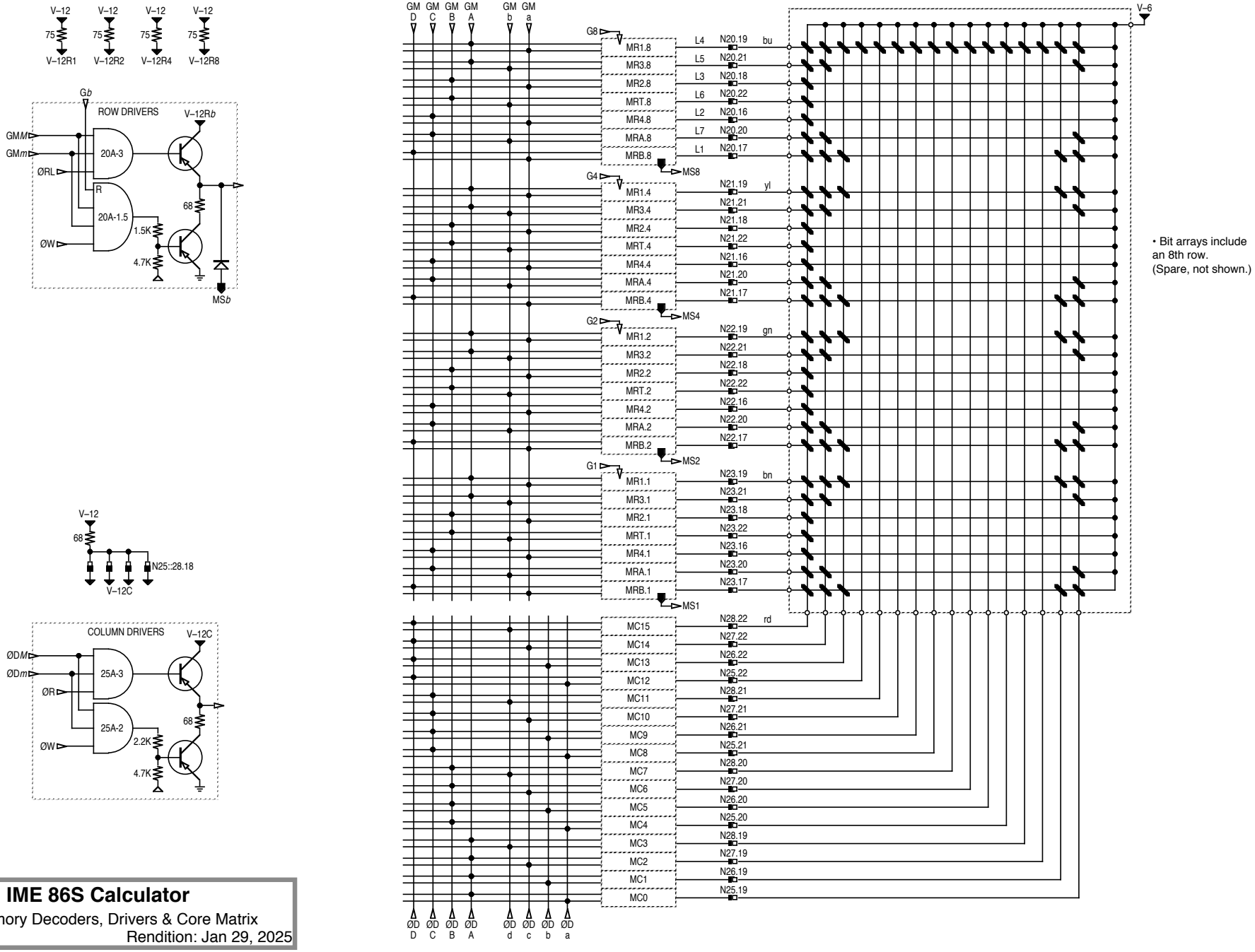
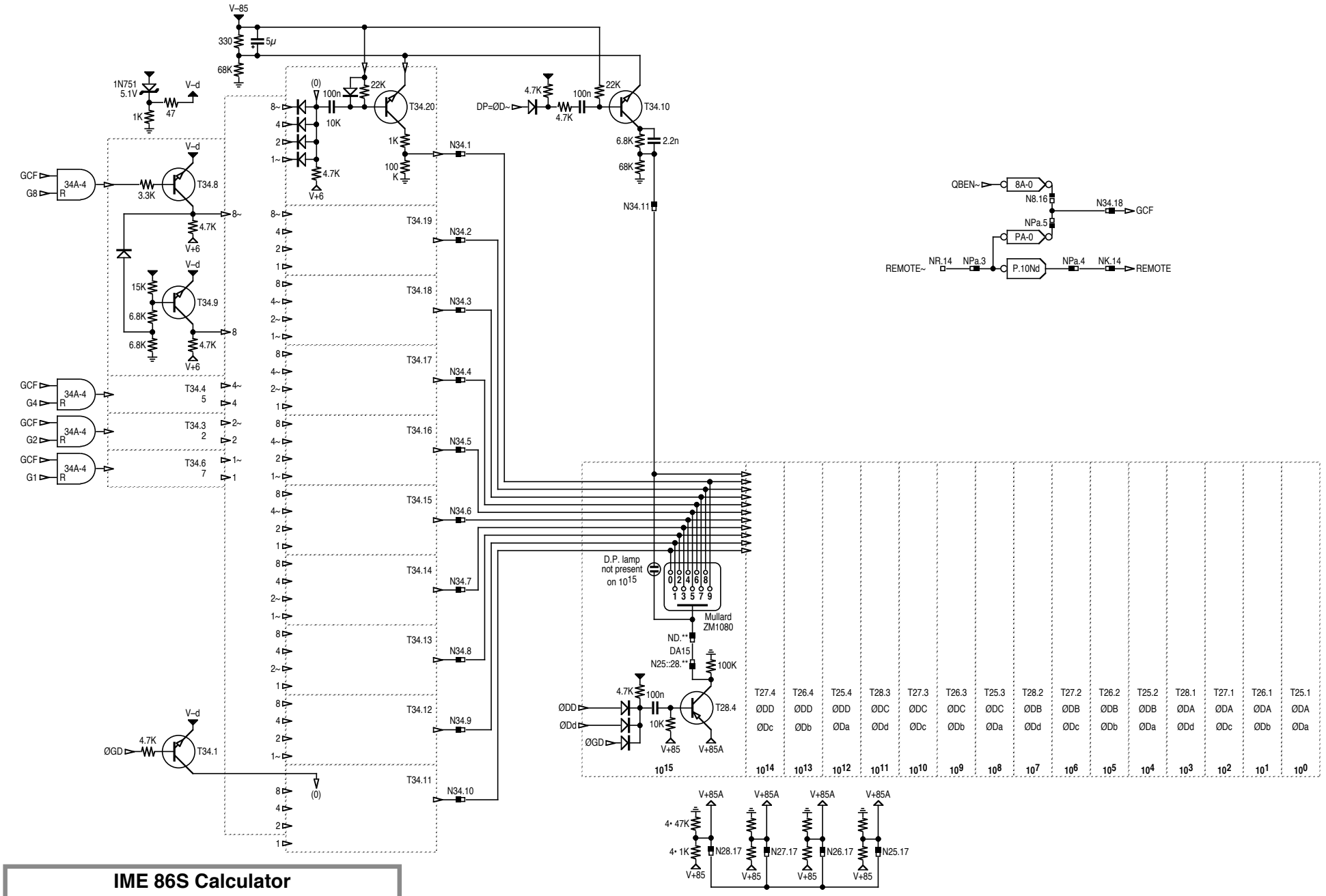


• Bit arrays include an 8th row. (Spare, not shown.)



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Section: Display

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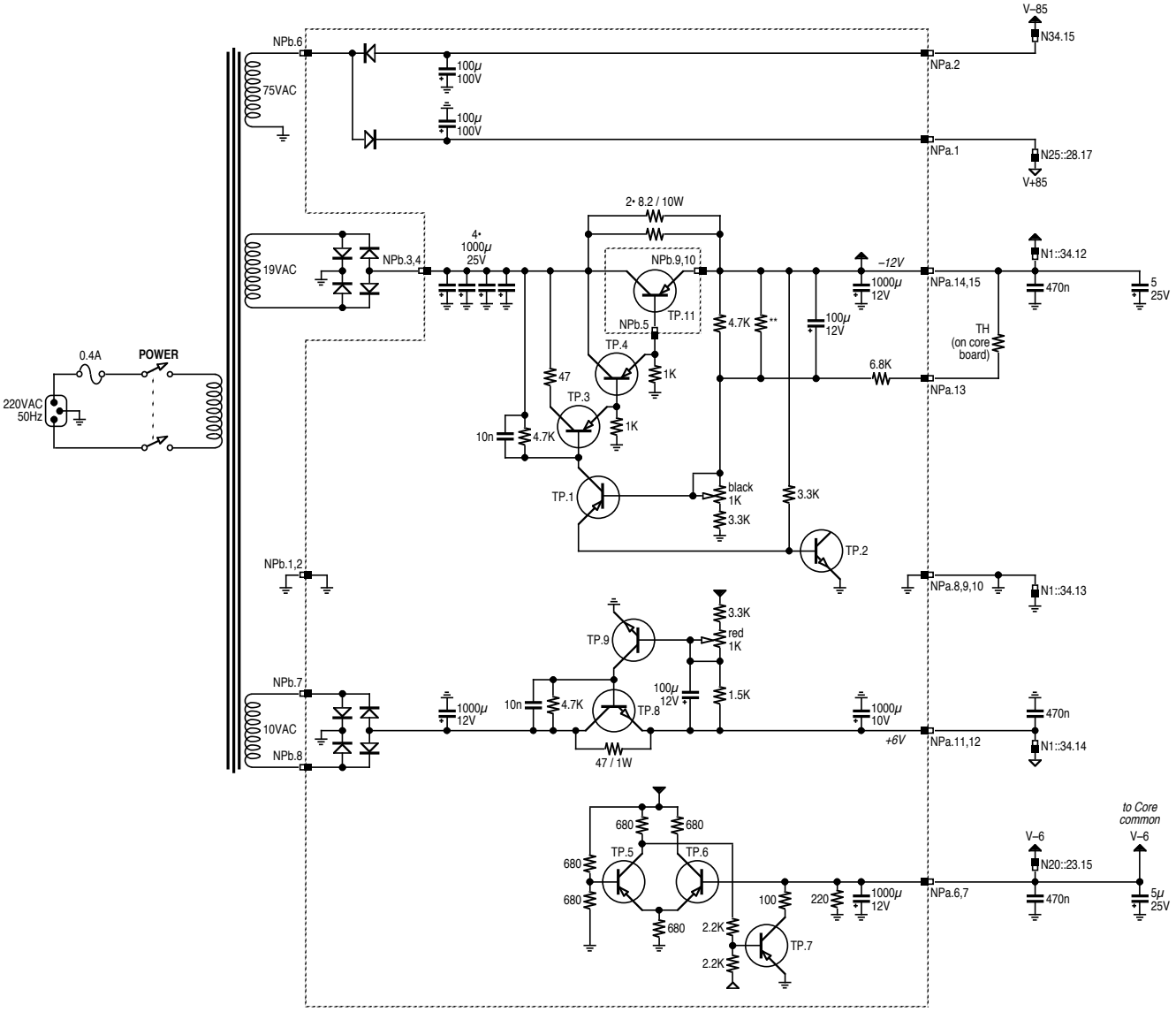

IME 86S Calculator

Section: Power Supply

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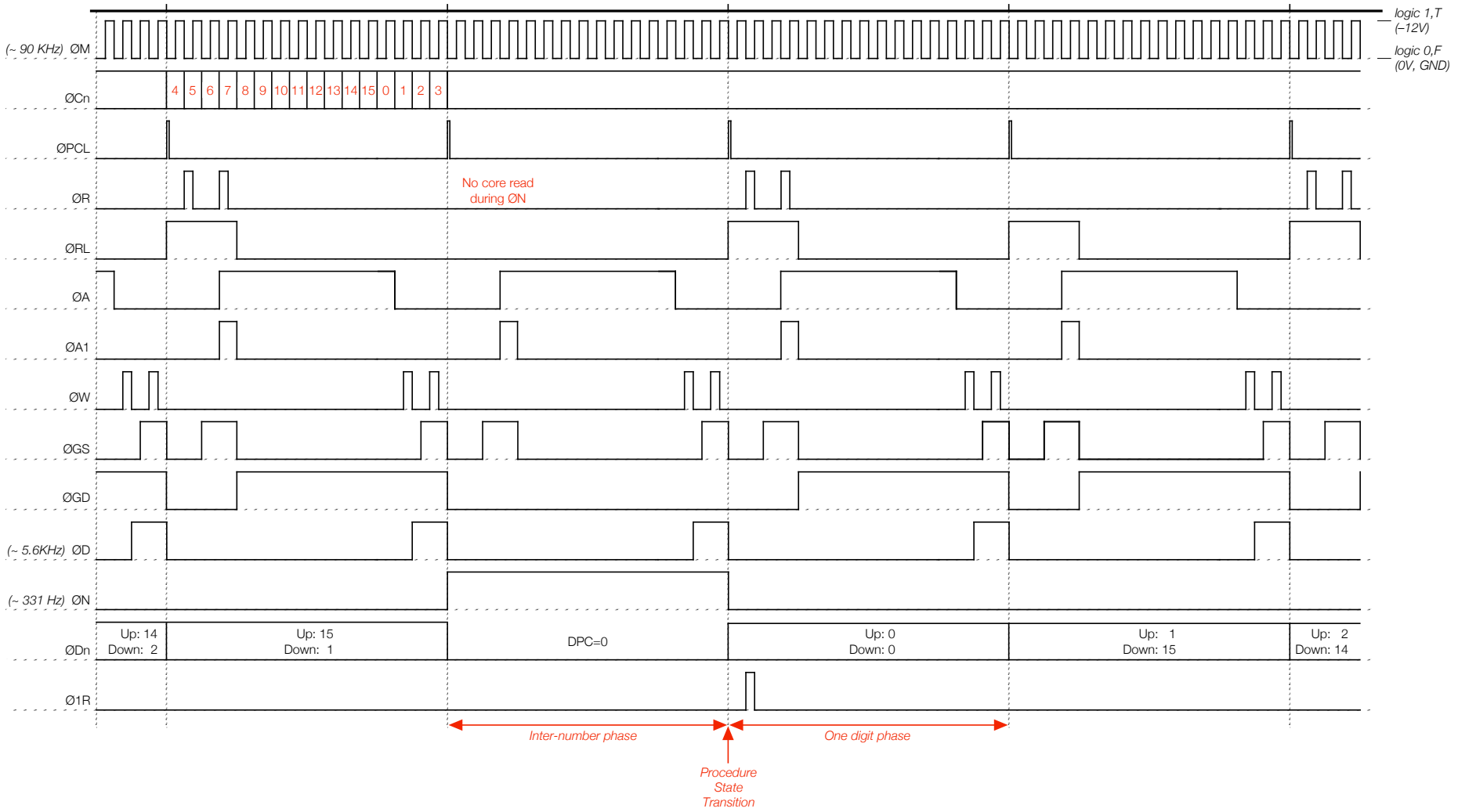
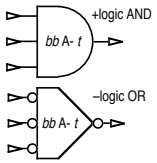
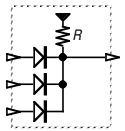


Unit 51409751: ØM = 89.3 KHz (11.2 µS)

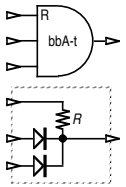
AND-Form Gates



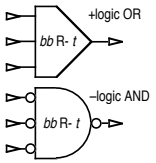


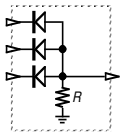
t	R
0	-
1	1K
1.5	1.5K
2	2.2K
3	3.3K
4	4.7K
6	6.8K
47	47K

AND-form with pull-up as input.



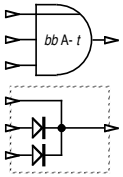
OR-Form Gates



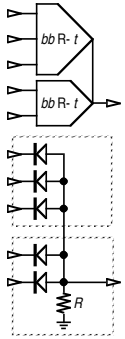


t	R
0	-
22	22K
22+	22K V+6

Wired Inputs
(AND-form example)



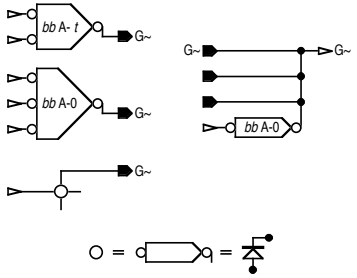
Distributed Gates
(OR-form example)



The perpendicular output line on a gate symbol indicates this is part of a distributed gate.

One of the contributors provides the load R while the others are (typically) type-0 (no load R).

Distributed Gate Separated on Pages
(–logic OR example)



This gate has 7 inputs in total.

The black tab symbol indicates this circuit electrically has multiple sources.

Gate Identification

Gates are identified with a label of the form:

bb . nn gg - t
or*bb . tt gg - t*

where:

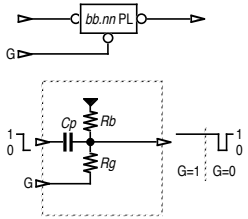
bb = board [1::34]
nn = enumeration
tt = transistor number in IME schematic
gg = gate type
t = optional type variation

gg =

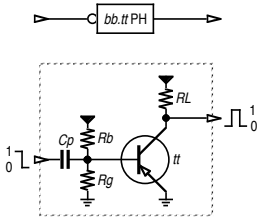
A	AND
R	OR
Nv	NOT
Nd	NOT with diode & Rh
NG	NAND with 1 inverted input (gated NOT)
BF	buffer
PL	pulse LOW on LOW-going edge
PH	pulse HIGH on LOW-going edge
PP	pulse LOW on HIGH-going edge

- Logic 0, F = 0V, GND
  Logic 1, T = –12V

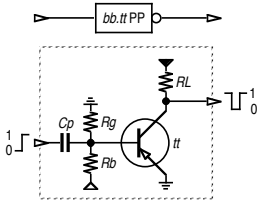
Pulsers



bb.nn	Rg	Cp	Rb
1.1	10	4.7n	
1.2	10	2.2n	
3.1	15	2.2n	
3.2	2.2g	1n	
3.3	3.3	10n	10
3.4	3.3g	10n	10
3.5	3.3	10n	
7.1	10	2.2n	33
8.1	6.8	2.2n	
8.2	6.8	2.2n	
8.3	6.8	1n	
8.4	6.8	2.2n	
8.5	6.8	2.2n	
8.6	15	1n	
8.7	15	1n	
12.1	2.2	1n	
12.2	10	1n	
16.1	10	10n	
16.2	22	4.7n	
16.3	10g	4.7n	
16.4	10	4.7n	
17.1	6.8	10n	
19.1	10	10n	
19.2	4.7	10n	

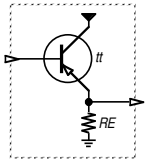


bb.tt	Rg	Cp	Rb	RL
5.9	-	2.2n	10	1.5
19.13	-	10n	10	4.7
30.12	-	2.2n	10	2.2

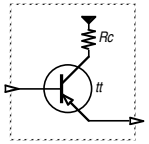


bb.tt	Rg	Cp	Rb	RL
8.8	-	4.7n	15	2.2
16.1	10	47n	22	4.7

Buffers

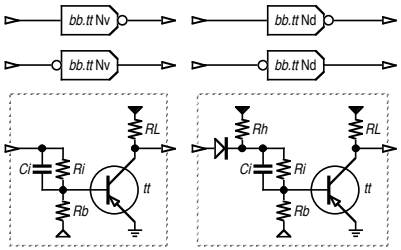


bb.tt	RE
18.3	2.2
18.19	2.2
18.20	2.2



bb.tt	Rc
33.10	100Ω
33.11	100Ω
33.12	100Ω
33.13	100Ω

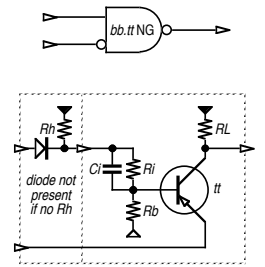
Inverters



bb.tt	Rh	Ri	Rb	RL	Ci
1.9	4.7	6.8	15	2.2	
1.10		6.8	15	10	
1.12	6.8	4.7	15	4.7	
1.13	4.7	6.8	15	2.2	
2.9		6.8	15	10	
2.11	3.3	4.7	15	4.7	
3.4		6.8	15	4.7	
3.11				3.3	
3.12		6.8	15	4.7	
4.1	4.7	6.8	15	3.3	
4.2	4.7	6.8	15	2.2	
4.3		6.8	15	xx	
4.4		4.7	15	2.2	
4.5		6.8	15	xx	
4.6		6.8	15	2.2	
5.1	3.3	6.8	15	2.2	470p
5.8		6.8	15	2.2	
5.10	4.7	6.8	15	2.2	
5.11	4.7	6.8	15	2.2	
5.12		4.7	10	4.7	
6.10	6.8	6.8	15	2.2	
6.11	2.2	3.3	10	xL	
6.12	4.7	10	15	4.7	**
8.7		6.8	15	3.3	
9.1		6.8	10	xx	
9.2		6.8	10	xx	
9.3		6.8	10	xx	
9.7		6.8	15	6.8	
9.8		6.8	15	6.8	
9.9		6.8	15	6.8	
9.10		6.8	10	3.3	
9.15	4.7	6.8	15	4.7	
11.8	4.7	6.8	15	2.2	
11.7	6.8	6.8	15	x3.3	
12.3		6.8	15	1.5	470p
13.2		6.8	10	4.7	
13.3		4.7	10	4.7	
13.4		4.7	10	4.7	
13.5		6.8	10	4.7	
13.6	4.7	4.7	15	2.2	
14.1		6.8	15	3.3	
14.2		6.8	15	xx	
14.3		6.8	10	3.3	
14.4		4.7	10	3.3	
14.5		4.7	10	3.3	
14.6		6.8	15	3.3	
14.7		4.7	10	3.3	

bb.tt	Rh	Ri	Rb	RL	Ci
15.1		6.8	15	4.7	
15.2		6.8	15	4.7	
15.3		6.8	15	4.7	
15.4		4.7	10	4.7	
15.5		4.7	10	4.7	
15.6		6.8	15	4.7	
15.7		6.8	15	4.7	
15.8		6.8	15	4.7	
15.9		6.8	10	4.7	
15.10		6.8	10	xx	
15.11		6.8	10	4.7	
16.10		3.3	6.8	4.7	
16.11		3.3	6.8	4.7	
16.12		3.3	6.8	4.7	
16.13	4.7	6.8	10	x2.2	
18.1	3.3	6.8	15	4.7	
18.2		2.2	6.8	xL	
18.4		6.8	15	2.2	
19.7	3.3	4.7	15	2.2	470p
19.8		4.7	10	2.2	470p
19.9	3.3	4.7	15	2.2	470p
19.10		4.7	10	2.2	470p
19.11	3.3	4.7	15	2.2	470p
19.12		4.7	10	2.2	470p
19.14	4.7	4.7	10	2.2	470p
19.15		6.8	10	2.2	470p
29.10		4.7	15	2.2	
30.1		4.7	15	2.2	**
30.13		1.5	6.8	2.2	
30.14		4.7	15	2.2	
30.15		2.2	4.7	xx	
30.16		6.8	15	xx	
30.17	3.3	3.3	10	2.2	
30.18		4.7	15	3.3	**
31.9	4.7	6.8	15	2.2	
32.1		6.8	15	xx	
32.10		4.7	15	2.2	
32.11		6.8	10	2.2	
32.12	4.7	6.8	15	x	**
33.9	4.7	6.8	15	x	**
P.10	1.5	3.3	6.8	1	**
4m.1		6.8	10	3.3	

Active Gates



bb.tt	Rh	Ri	Rb	RL	Ci
1.11		6.8	15	4.7	
2.10		6.8	15	4.7	
6.3		4.7	15	2.2	470p
7.5		6.8	15	2.2	
8.9		4.7	15	2.2	
8.10	4.7	4.7	15	2.2	
9.2		6.8	10	3.3	
9.4		6.8	15	3.3	
9.6		4.7	15	3.3	
10.1	3.3	6.8	15	3.3	
10.2		6.8	15	3.3	
10.3		6.8	15	3.3	
10.4		6.8	15	3.3	
10.5		6.8	15	3.3	
10.6	4.7	6.8	15	3.3	
10.7		6.8	15	3.3	
10.8		6.8	15	3.3	
10.9		6.8	15	3.3	
10.10		6.8	15	2.2	
11.1	6.8	6.8	15	3.3	
11.2	6.8	6.8	15	3.3	
11.3		6.8	15	3.3	
11.4		6.8	15	3.3	
11.5		6.8	15	3.3	
11.6		6.8	15	3.3	470p
11.9	6.8	6.8	15	3.3	
12.4		6.8	15	3.3	
12.5	3.3	6.8	10	3.3	470p
12.6		6.8	15	xx	
12.7		6.8	15	3.3	
12.8	3.3	6.8	10	3.3	470p
12.9		6.8	15	3.3	
12.10		6.8	15	3.3	
13.1	4.7	6.8	15	3.3	
13.7	4.7	6.8	15	3.3	
13.8	4.7	6.8	15	3.3	
13.9	4.7	4.7	15	3.3	
29.9	4.7	10	15	xx	

- R in KΩ.

- x = no RL, load R is external to module.
- xx = no RL, load R is on other board.
- xL = lamp driver.

Capacitor Color Code

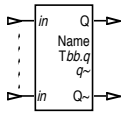
wh	220p
yl	470p
og	1n
rd	2.2n
gn	4.7n
bu	10n

**** Special**:

- 6.12Nd: additional trim R parallel to Ri.
- 30.1Nv: 470p C from base to GND.
- 30.18Nv: 1n C from base to GND.
- 32.12Nd: external 220+2.2K load R.
- 33.9Nd: external 220+2.2K load R.
- P.10Nd: 10n C from base to GND.

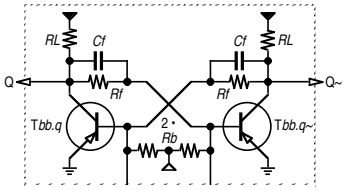
Flip-Flops

Flip-Flop Base

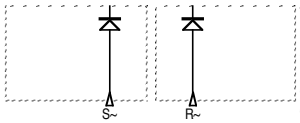


in are input options.

q & *q~* are transistor numbers in IME schematic.



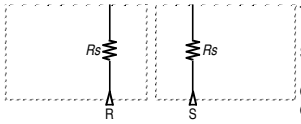
Input Options Immediate



Types S~ and R~

Set & Reset, assert 0.

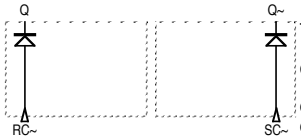
Q goes 1 if SS~ = 0.
Q goes 0 if RG~ = 0.



Types S and R

Set & Reset, assert 1.

Q goes 1 if S = 1.
Q goes 0 if R = 1.

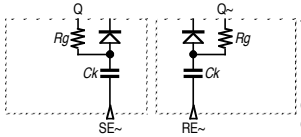


Types SC~ and RC~

Collector Set & Reset.

Q goes 1 if SC~ = 0.
Q goes 0 if RC~ = 0.

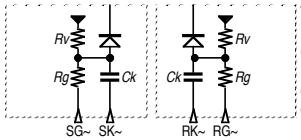
Input Options Edge-Triggered



Types SE~ and RE~

Edge-triggered Set & Reset.

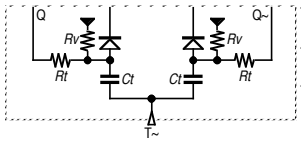
Q goes 1 on 1-to-0 edge of SE~.
Q goes 0 on 1-to-0 edge of RE~.



Types SG~ and RG~

Gated Edge-triggered Set & Reset.

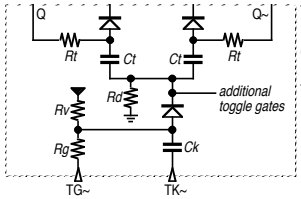
Q goes 1 if SG~=0 on 1-to-0 edge of SK~.
Q goes 0 if RG~=0 on 1-to-0 edge of RK~.



Type T

Toggle.

Toggle Q on 1-to-0 edge of T~.



Type TG

Gated Toggle.

Toggle Q if TG~=0 on 1-to-0 edge of TK~.

Base Component Values

Flip-Flop	RL	Rf	Cf	Rb		Flip-Flop	RL	Rf	Cf	Rb	
FC1	2.2	6.8	220	22	2622	FDP1	2.2	10	470	22	2142
FC2	2.2	6.8	470	22	2642	FDP2,8	2.2	10	470	22	2142
FC4,8	2.2	6.8	470	22	2642	FDP4	2.2	10	470	22	2142
						FTC1	2.2	10	220	15	2125
FD1	1	4.7	1	22	1412	FTC2	2.2	10	470	22	2142
FD2,4,8	1	4.7	1	22	1412	FTC4,8	2.2	10	470	22	2142
FØN	2.2	4.7	470	15	2445	FSC3	3.3	10	470	22	3142
FKP	3.3	10	-	22	3102	FSA,B	*	6.8	-	10	
FEX	2.2	6.8	1	22	2612	FST	*	6.8	-	10	
						FS1,2,3,4	*	6.8	-	10	
FEEN	3.3	10	470	22	3142	FSP,Q	2.2	6.8	-	10	2601
FESH	3.3	10	470	15	3145	FSM	2.2	6.8	-	10	2601
FECL	2.2	6.8	470	22	2642	FCS	2.2	6.8	470	22	2642
F25,26	2.2	10	-	22	2102	FX1,Y1	2.2	10	470	22	2142
						FX2,4	2.2	10	470	22	2142
FPa1	2.2	6.8	470	22	2642	FY2,4	2.2	10	470	22	2142
FPa2	2.2	6.8	470	22	2642	FX8,Y8	2.2	10	470	22	2142
FPb1,b2	2.2	6.8	470	22	2642						
FPN	2.2	6.8	-	22	2602	FZ1	2.2	10	220	22	2122
						FZ2,4,8	2.2	10	470	22	2142
FQM1,2,4,8	2.2	6.8	470	22	2642						
FQB1,2,4	2.2	6.8	470	15	2645	FXR	2.2	6.8	470	22	2642
						FYC	2.2	6.8	-	10	2601
F31	2.2	6.8	470	15	2645						
F32	2.2	6.8	470	15	2645						
FNn	2.2	6.8	470	22	2642						
Fsr	2.2	10	470	22	2142						
FGZ	2.2	6.8	470	22	2642	**Special:**					
FUD	2.2	6.8	470	22	2642	FSA,B,T,1,2,3,4	RL(Q)=1.5K, RL(Q~)=2.2K				
FOWP	2.2	10	470	22	2142	FX8,Y8	No Cf from Q~.C to Q.B				
FOW	2.2	10	-	15	2105						

Input Component Value Codes

SG,RG,SE,RE	:	- *cRC cRv*	*cRC* –> Ck,Rg
T	:	- *cRC cRv*	*cRC* –> Ct,Rt
TG	:	- *gcRC cRv tcRC cRd*	*gcRC* –> Ck,Rg; *tcRC* –> Ct,Rt
S, R	:	- *cRs*	

cRC	R	C	cRv	Rv	cRd	Rd	cRs	Rs
a	3.3K	470p	3	33K	4	4.7K	4	4.7K
b	4.7K	470p	4	47K	6	6.8K	6	6.8K
c	6.8K	470p	10	100K	1	10K	1	10K
j	0	1n						
k	3.3K	1n						
m	4.7K	1n						
n	6.8K	1n						
p	10K	1n						
r	15K	1n						
w	4.7K	2.2n						
x	6.8K	2.2n						
y	10K	2.2n						
z	15K	2.2n						
g	6.8K	4.7n						

N17

1	**PMP**
2	**PRR**
3	**PMM·(N~)**
4	**PMD·N**
5	**PEQ·(N~)**
6	**PSR**
7	**PEQ**
8	**PDV**
9	**PEQ·N**
10	QMC
11	EXEC~
12	V–12
13	GND
14	V+6
15	KNMs~
16	**KOP~**
17	KMPs~
18	Nn
19	MB
20	KDVs~
21	KSRs~
22	KEQs~

N16

1	PMP
2	**QMC**
3	**QMd**
4	**QMB**
5	**QMb**
6	**QMc**
7	**QMA**
8	**QM8**
9	F32
10	**EXEC~**
11	ØN
12	V–12
13	GND
14	V+6
15	KOP~
16	KCs~
17	PEQ·(N~)·Nn
18	**BSR~**
19	**BDV~**
20	**BMP~**
21	PSR
22	PDV

N15

1	**GR4INC~**
2	PEQ·(N~)
3	**PEQ·(N~)·Nn**
4	QMd
5	QMB
6	QMb
7	PSR
8	QMc
9	QMA
10	PMM·(N~)
11	QMC
12	V–12
13	GND
14	V+6
15	**GAOP~**
16	**GFG~**
17	**GCL~**
18	**GTR~**
19	**GAA~**
20	**GBB~**
21	**GGG~**
22	**Nn**

N14

1	PEQ
2	PMP
3	PDV
4	PEQ·N
5	PEQ·(N~)
6	QMd
7	PMD·N
8	QMc
9	QMC
10	QMA
11	QMb
12	V–12
13	GND
14	V+6
15	**GFG~**
16	**GCL~**
17	**GTR~**
18	**GAA~**
19	**GFK~**
20	**GBB~**
21	**GGG~**
22	PRR

N13

1	PEQ
2	PMP
3	PDV
4	PEQ·N
5	ØGS
6	**GR4INC~**
7	QMB
8	QMd
9	boxn
10	QMC
11	QMb
12	V–12
13	GND
14	V+6
15	boxS
16	**GAOP~**
17	**GAGG~**
18	**GAA~**
19	**GBB~**
20	**GGG~**
21	GAAB~
22	PRR

N12

1	QBa
2	**ADDAA~**
3	QBb
4	**GSL~**
5	**GASUB~**
6	QBd
7	**SRB7~**
8	**P1~**
9	Ø1R
10	BSR~
11	**P2~**
12	V–12
13	GND
14	V+6
15	ØN
16	**ZCLK**
17	**GAA~**
18	ØN~
19	**QBLP~**
20	QBB
21	FCS
22	**GAAB~**

N11

1	QBa
2	ADDAA~
3	F31·nF32
4	QBb
5	ØD0
6	Z=0
7	ØGS
8	ØR
9	**P1~**
10	**GSEL~**
11	**GZ~**
12	V–12
13	GND
14	V+6
15	BMP~
16	**GAA~**
17	**GGG~**
18	**GBB~**
19	**QBLP~**
20	**ZDOWN~**
21	**GAGG~**
22	**P4~**

NK

1	**K8s~**
2	**K4s~**
3	**K2s~**
4	**K1s~**
5	**TRC**
6	**KCs~**
7	**KDLs~**
8	**KSRs~**
9	**KDRs~**
10	**KNMs~**
11	**KDPs~**
12	**KNEGs~**
13	**S**
14	REMOTE
15	**N**
16	**KDVs~**
17	**KMPs~**
18	**TCM**
19	**KEQs~**
20	**KAAs~**
21	**KBBs~**
22	**KGGs~**

NPa

1	**V+85**
2	**V–85**
3	REMOTE~
4	REMOTE
5	GCF
6	**V–6**
7	**V–6**
8	GND
9	GND
10	GND
11	**V+6**
12	**V+6**
13	thermistor
14	**V–12**
15	**V–12**

NPb

1	GND
2	GND
3	C
4	C
5	B
6	75VAC
7	10VAC
8	10VAC
9	V–12
10	V–12

N10

1	**GAAB~**
2	FCS
3	-
4	QBb
5	F31~
6	F32
7	F32~
8	**GSRc~**
9	QBd
10	QBc
11	BDV~
12	V–12
13	GND
14	V+6
15	BMP~
16	**GAA~**
17	**GGG~**
18	**GBB~**
19	**QBLP~**
20	**GSL~**
21	**GSRz~**
22	**GASUB~**

N09

1	EXEC~
2	**QBEN~**
3	KCs~
4	KDRs~
5	F31
6	QBB
7	QBb
8	KDLs~
9	**CMT**
10	QBd
11	QBc
12	V–12
13	GND
14	V+6
15	ØN~
16	**GAA~**
17	BSR~
18	**GGG~**
19	**GBB~**
20	**GSL~**
21	**GSRz~**
22	**GCL~**

N08

1	F32
2	BSR~
3	BMP~
4	TCCLK
5	BDV~
6	ØN
7	**QBB**
8	**QBa**
9	**QBb**
10	**QBd**
11	**QBc**
12	V–12
13	GND
14	V+6
15	**QBEN~**
16	GCF
17	F31
18	**TCCL~**
19	**ZCLK**
20	QBLP~
21	FYC
22	F31~

N07

1	QBd
2	TC=DP
3	QBc
4	ØD15
5	DP=ØD
6	BDV~
7	TCROLL
8	BMP~
9	QBa
10	X=0~
11	VP
12	V–12
13	GND
14	V+6
15	SRB7~
16	BSR~
17	**REVCND**
18	**F31**
19	**F31·nF32**
20	**F32~**
21	**F32**
22	**F31~**

N06

1	**LOW**
2	ØN
3	SETOW
4	GSL~
5	DP=ØD
6	ØR
7	EXEC~
8	BMP~
9	YINC
10	MB
11	KNMs~
12	V–12
13	GND
14	V+6
15	BSR~
16	**GAA~**
17	**GCL~**
18	**GFG~**
19	GR4INC~
20	**P1~**
21	Z=0
22	KCs~

N05

1	ØN
2	**SETOW**
3	GAGG~
4	ØA~
5	BDV~
6	**XINC**
7	**GXY**
8	**YINC**
9	ØD0
10	ØM
11	GAOP~
12	V–12
13	GND
14	V+6
15	**GZ~**
16	GASUB~
17	**FYC**
18	ØA1
19	XROLL
20	GSH
21	**GZ**
22	YROLL

N04

1	ØN
2	QBEN~
3	**RESETN**
4	**SETN**
5	**FCS**
6	QM8
7	SN
8	ØGS
9	ØR
10	GTR~
11	GAOP~
12	V–12
13	GND
14	V+6
15	**BLW**
16	**GSEL~**
17	**GASUB~**
18	FYC
19	CMT
20	KNEGs~
21	EXEC~
22	**STR**

N03

1	**TCCLK**
2	ØM
3	DP=ØD
4	TC=ØD~
5	ØPCL
6	**ZCL~**
7	**SS**
8	GZ
9	ØN
10	GSL~
11	GSR~
12	V–12
13	GND
14	V+6
15	ØN~
16	CMT
17	**EXEC~**
18	TV
19	KNMs~
20	**GSH**
21	TC=ØD
22	DP=ØD~

N02

1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	GSL~
6	ØDd
7	ØDc
8	ØDb
9	ØDa
10	**DP=ØD**
11	EXEC~
12	V–12
13	GND
14	V+6
15	**GSEL~**
16	GSR~
17	KDLs~
18	KDRs~
19	TC=ØD
20	**TC=DP**
21	ØN
22	**DP=ØD~**

N01

1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	TCCL~
6	ØDd
7	ØDc
8	ØDb
9	ØDa
10	TCCLK
11	**TCROLL**
12	V–12
13	GND
14	V+6
15	CMT
16	**GSEL~**
17	GCL~
18	KOP~
19	**TC=ØD**
20	**TC=ØD~**
21	ØN~
22	REVCND

• Bold-faced expressions are signal sources.

ND
1
2
3
4
5
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CORE

24

N23	
1	GMb
2	GMA
3	GMB
4	GMC
5	GMD
6	GMa
7	ØRL
8	G1
9	ØW
10	**P1~**
11	STR
12	V–12R
13	GND
14	V+6
15	V–6
16	**MR4.1**
17	**MRB.1**
18	**MR2.1**
19	**MR1.1**
20	**MRA.1**
21	**MR3.1**
22	**MRT.1**

N22	
1	GMb
2	GMA
3	GMB
4	GMC
5	GMD
6	GMa
7	ØRL
8	G2
9	ØW
10	**P2~**
11	STR
12	V–12R
13	GND
14	V+6
15	V–6
16	**MR4.2**
17	**MRB.2**
18	**MR2.2**
19	**MR1.2**
20	**MRA.2**
21	**MR3.2**
22	**MRT.2**

N21	
1	GMb
2	GMA
3	GMB
4	GMC
5	GMD
6	GMa
7	ØRL
8	G4
9	ØW
10	**P4~**
11	STR
12	V–12R
13	GND
14	V+6
15	V–6
16	**MR4.4**
17	**MRB.4**
18	**MR2.4**
19	**MR1.4**
20	**MRA.4**
21	**MR3.4**
22	**MRT.4**

N20	
1	GMb
2	GMA
3	GMB
4	GMC
5	GMD
6	GMa
7	ØRL
8	G8
9	ØW
10	**P8~**
11	STR
12	V–12R
13	GND
14	V+6
15	V–6
16	**MR4.8**
17	**MRB.8**
18	**MR2.8**
19	**MR1.8**
20	**MRA.8**
21	**MR3.8**
22	**MRT.8**

N19	
1	**GMb**
2	**GMA**
3	**GMB**
4	**GMC**
5	**GMD**
6	**GMa**
7	GAA~
8	GBB~
9	GGG~
10	GSEL~
11	GFG~
12	V–12
13	GND
14	V+6
15	GFK~
16	CMT
17	KEQs
18	SS
19	EXEC~
20	KGGs~
21	KBBs~
22	KAAs~

N18	
1	**MB**
2	GMb
3	GMA
4	GMB
5	GMC
6	GMD
7	GMa
8	SETN
9	RESETN
10	ØW
11	-
12	V–12
13	GND
14	V+6
15	T+
16	GCL
17	**KEQs**
18	QBEN~
19	**SN**
20	**LM**
21	BDV~
22	BMP~

N34	
1	NK9
2	NK8
3	NK7
4	NK6
5	NK5
6	NK4
7	NK3
8	NK2
9	NK1
10	NK0
11	NKP
12	V–12
13	GND
14	V+6
15	V–85
16	DP=ØD~
17	ØGD
18	GCF
19	G1
20	G2
21	G4
22	G8

N33	
1	U8
2	U4
3	U2
4	U1
5	P8~
6	P4~
7	P2~
8	P1~
9	YINC
10	**YROLL**
11	ØN~
12	V–12
13	GND
14	V+6
15	**GXY**
16	ØGS
17	**GY~**
18	XYCL~
19	**G1**
20	**G2**
21	**G4**
22	**G8**

N32	
1	**U8**
2	**U4**
3	**U2**
4	**U1**
5	P8~
6	P4~
7	P2~
8	P1~
9	XINC
10	**XROLL**
11	**GCL**
12	V–12
13	GND
14	V+6
15	GZ~
16	**X=0~**
17	GY~
18	**XYCL~**
19	ØPCL
20	TCM
21	EXEC~
22	GCL~

N31	
1	**U8**
2	**U4**
3	**U2**
4	**U1**
5	P8~
6	P4~
7	P2~
8	P1~
9	ZCLK
10	GZ
11	Z=0
12	V–12
13	GND
14	V+6
15	GZ~
16	ZCL~
17	K8s~
18	K4s~
19	K2s~
20	K1s~
21	EXEC~
22	ZDOWN~

N30	
1	**ØGD**
2	**ØRL**
3	**ØA~**
4	**ØR**
5	**ØPCL**
6	**ØW**
7	**Ø1R**
8	**ØA1**
9	-
10	ØD0
11	BLW
12	V–12
13	GND
14	V+6
15	ØN~
16	**ØD**
17	-
18	-
19	-
20	**ØM**
21	**ØGS**
22	ØN

N29	
1	**ØD15**
2	**ØDD**
3	**ØDC**
4	**ØDB**
5	**ØDA**
6	**ØDd**
7	**ØDc**
8	**ØDb**
9	**ØDa**
10	**ØD0**
11	**BLW**
12	V–12
13	GND
14	V+6
15	**ØN~**
16	ØD
17	**VP**
18	**DP=ØD**
19	GSRz~
20	**GSR~**
21	GSRc~
22	**ØN**

N28	
1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	ØGD
6	ØDd
7	ØW
8	ØR
9	**DA12**
10	**DA8**
11	**DA4**
12	V–12
13	GND
14	V+6
15	V+85
16	**DA0**
17	V+85A
18	V–12C
19	**MC3**
20	**MC7**
21	**MC11**
22	**MC15**

N27	
1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	ØGD
6	ØDc
7	ØW
8	ØR
9	**DA13**
10	**DA9**
11	**DA5**
12	V–12
13	GND
14	V+6
15	V+85
16	**DA1**
17	V+85A
18	V–12C
19	**MC2**
20	**MC6**
21	**MC10**
22	**MC14**

N26	
1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	ØGD
6	ØDb
7	ØW
8	ØR
9	**DA14**
10	**DA10**
11	**DA6**
12	V–12
13	GND
14	V+6
15	V+85
16	**DA2**
17	V+85A
18	V–12C
19	**MC1**
20	**MC5**
21	**MC9**
22	**MC13**

N25	
1	ØDD
2	ØDC
3	ØDB
4	ØDA
5	ØGD
6	ØDa
7	ØW
8	ØR
9	**DA15**
10	**DA11**
11	**DA7**
12	V–12
13	GND
14	V+6
15	V+85
16	**DA3**
17	V+85A
18	V–12C
19	**MC0**
20	**MC4**
21	**MC8**
22	**MC12**

Section	Old	Signal	Description
Timing	AST	ØM	Master clock.
	R	ØR	Core Read pulse for column lines.
	RL	ØRL	Core Read pulse for register lines.
	W	ØW	Core Write pulse.
	10P	ØA	Span of 10 pulses for arithmetic counting.
	FP	ØA1	First pulse of the ØA span.
	INSC	ØD	Digit clock.
	1P	ØD0	Digit 0 of the number cycle (LSD).
	16P	ØD15	Digit 15 of the number cycle (MSD).
	1R	Ø1R	A single read pulse at the beginning of a number (ØD0).
	12	ØN	A digit cycle in-between number cycles, for control-state changes.
	GS	ØGS	Switches source of register access code.
	PCL	ØPCL	Pulse to clear X & Y.
Keyboard	T…	K…	Keyboard signals.
	T1,2,4,8	KN1,2,4,8	BCD-encoded numeral keys.
	T0	KNM~	Numeral key pressed.
	SETSC	KOP~	Operation key pressed.
Control		FEX	Debounce and execution control flag.
	7~	EXEC~	Machine is busy executing a procedure (assert=0).
	11	FKP	Flag indicating DP key has been pressed.
	-	FEEN	Flag to enable numeral entry.
	-	FESH	Flag to shift digits during numeral entry.
	-	FECL	Flag to select & clear B on entry of first digit of number.
	25	FRS1	Clear & Shift (register sequence) procedure-select flags.
	26	FRS2	
	-	FPa1,2,b1,2	Program-select flags.
	-	FPN	Program-select modifier for N operand.
	-	P…	Program-select signals.
	MP,DV,SR	BMP,BDV,BSR	Subroutine-select signals.
		QM...	Main Sequence Counter.
	A'…C'	QMA,B,C	QM major.
	a'…d'	QMa,b,c,d	QM minor.
	-	QB...	Subroutine Sequence Counter.
	PR	QBEN	QB enabled (subroutine executing).
	-	QBA	QB major=0.
	16	QBB	QB major=1.
	S1…S4	QBa,b,c,d	QB minor.
	BLP	QBLP	Loop at current step of QB (stop QB incrementing).
	31	F31	MP/DV/SR utility flag.
	32	F32	MP/DV/SR utility flag.
	IØ	REMOTE	
	-	FUD	Flag set for the 1st read pulse of the units digit.
	I8	SRB7	QB=7 during BSR.

Section	Old	Signal	Description
Gating Signals		G…	Control signals to gate data-processing elements.
	GSel	GSEL~	Selects source of register access code, 0:GGBA, 1:FGBA.
	GSA	GFG	Set FGBA = GGBA.
	RMS	GFK	Set FGBA = KGG,BB,AA (register from keypress).
	SSR	GSL	Shift register left.
	SH	GSR	Shift register right.
	SDN	GSRz	Shift register rIght, zero-fill.
	SDR	GSRc	Shift register right, circulate digit.
	GTR	GTR	Transfer Register. R(GGBA) <= R(FGBA).
	ADD	GAGG	Enable arithmetic, use GGBA for both operands.
	SOTT	GASUB	Enable arithmetic, perform subtraction.
	ADDDV	GAAB	Enable arithmetic, perform A <+/–= B.
	OP	GAOP	Enable arithmetic, signed add/subtract.
	GOP	GXY	Enable ØGS switching of X/Y selection for arithmetic cycle.
	OPn	GR4INC	Add 1 to Register 4.
Sign Flags	-	FSA,B,T,1,2,3,4	Sign of number in respective register.
	-	FSP, FSQ,	Signs of operands during an operation.
	-	FSM	
	-	FCS	Change-sign flag, indicates the sign flag of a register needs to be flipped.
DP Counter	-	DP	User-set Decimal PointPosition adjusted by L & R keys.
	SC2	DP=ØD	
Tracking Counter	CND	TC	Tracks digit to receive numeral during entry, & progress during MP/DV/SR.
	INCND	TCCLK	Increment or decrement TC.
	OUTCND	TCROLL	Rollover/carry from TC.
	SC1	TC=ØD	The current digit being processed matches TC.
	SC3	TC=DP	Strictly: ØD>TC=DP.
X Decade		X	BCD counter for addend digit for arithmetic.
	INX	XINC	
	OUTX	XROLL	
	CLXY	XYCL	Clear X & Y.
Y Decade		Y	BCD counter for summing digit for arithmetic counts.
	INY	YINC	
	OUTY	YROLL	
Z Decade		Z	4-bit counter for keypress numeral, shifting & digit construction.
	INZ	ZCLK	
	CLZ	ZCL	Clear Z.
Arithmetic	XC	FXR	Roll-over flag from X digit to control counting into Y digit.
	10	FYC	Carry flag from Y digit.
Register Address	Galpha	GAA	3 together indicate register selection in binary code, GGBA.
	Gbeta	GBB	
	Ggamma	GGG	
	-	FGA	Current-Register flags, FGBA.
	-	FGB	
	-	FGG	
Memory		GMA,B,C,D	Register memory address, Major.
		GMa,b	Register memory address, Minor.
	MB		Register B selected.