Sharp Compet 17 Calculator

Contents

Notes

- Gate symbols and signal names are presented in accordance with:
  logic 1 = GND
  logic 0 = V–24
- The symol Ncp denotes a physical connector pin, where *c*=connector and *p*=pin. Solid black end is the male side of the connector. White end is the female side of the connector.
- ⟶► ◄⟵ connection between different sections.
  ⟶▷ ▷⟵ connection limited to same section.
  Arrows indicate direction of signal or energy flow.
- The symbol ▲ without an additional label denotes VDD (–24V).
- Capacitance in microfarads unless otherwise indicated.
- This schematic includes the user memory which is not present in the Compet 17 model. Components marked with "§" are not present in the Compet 17.
- These drawings based on a Model CS-17C unit with Serial No. 810591T.

Log

- 2000 Jul: Initial drawing / bhilpert.
- 2004 Oct: Signals on the remote connector (NR) elaborated further.
  Switches and notes about single-cycle control of P added.
- 2017 May: Format updates. Question of pins on IC 5-6 noted.

Gate Identification

Gates and logic elements are identified by symbols of the following form:

Gate ID	Description	
1-*n*	inverter	in μPD1 IC
2-*n*	2 by 2 AND–OR gate	in μPD2 IC
3-*n*	4-input AND gate	in μPD3 IC
4-*n*	flip-flop	in μPD4 IC
5-*n*	4-bit shift register	in μPD5 IC
6-*n*	8-bit shift register	in μPD6 IC
7-*n*	MOSFET	in μPD7 IC
M-*n*	MOSFET	discrete

Discrete gates have no distinguishing identifier but their inputs are identified with a label indicating the location of the diode which implements it:

Label	Description
g.p	diode in TDA001 or TDA002 package *g* at pin *p*
d*n*	discrete diode

See the IC Pinouts and Gate Construction page for more about the integrated circuits.

See the Physical Layout and Connectors page for more about IC and gate location.

Signal Names

Section	Signal	Description
Timing	Ø…	Master timing.
	Ø1	Master clock, data capture phase.
	Ø2	Master clock, output transition phase.
	Ø3	Master clock, a third phase used by some flip-flops.
	ØB…	Bit timing.
	ØD…	Digit timing (4 bits constitutes a digit).
	ØnB1+3	Used for triggering digit timing and display latch.
	Øn(D16•B8•1)	Capture pulse at the end of each full number cycle.
Keyboard	K…	The keyboard and numeral encoder.
	P	Indicates a number cycle during which processing occurs.
Control	S…, C…	The state machine.
	C	Multiply or divide operation pending.
	D	Divide operation pending.
	F, G, J, M, S	Assorted state flags.
	S…	Assorted internal state signals.
	IDLE	1 during display and simple operations, 0 during multi-cycle operations.
	CX…	Outputs from control to the X register.
	CW…	" W register.
	CM…	" M register.
	CPX…	" PX decimal point counter.
	CPW…	" PW decimal point counter.
	CPY…	" PY digit counter.
X Register	X…	The operand being displayed. Arithmetic is also incorporated in this register.
	XC1,2,4,8	BCD numerals on their way to the display.
	CARRY	Carry indication to control.
W Register	W	The second operand.
M Register	M	The user memory.
PX Counter	PX	Ring counter to hold the place of the decimal point for the X operand.
	PXI	Signal to the display to turn on the decimal point at the appropriate time.
PW Counter	PW	Ring counter to hold the place of the decimal point for the W operand.
PY Counter	PY	Ring counter used during multiply and divide operations.

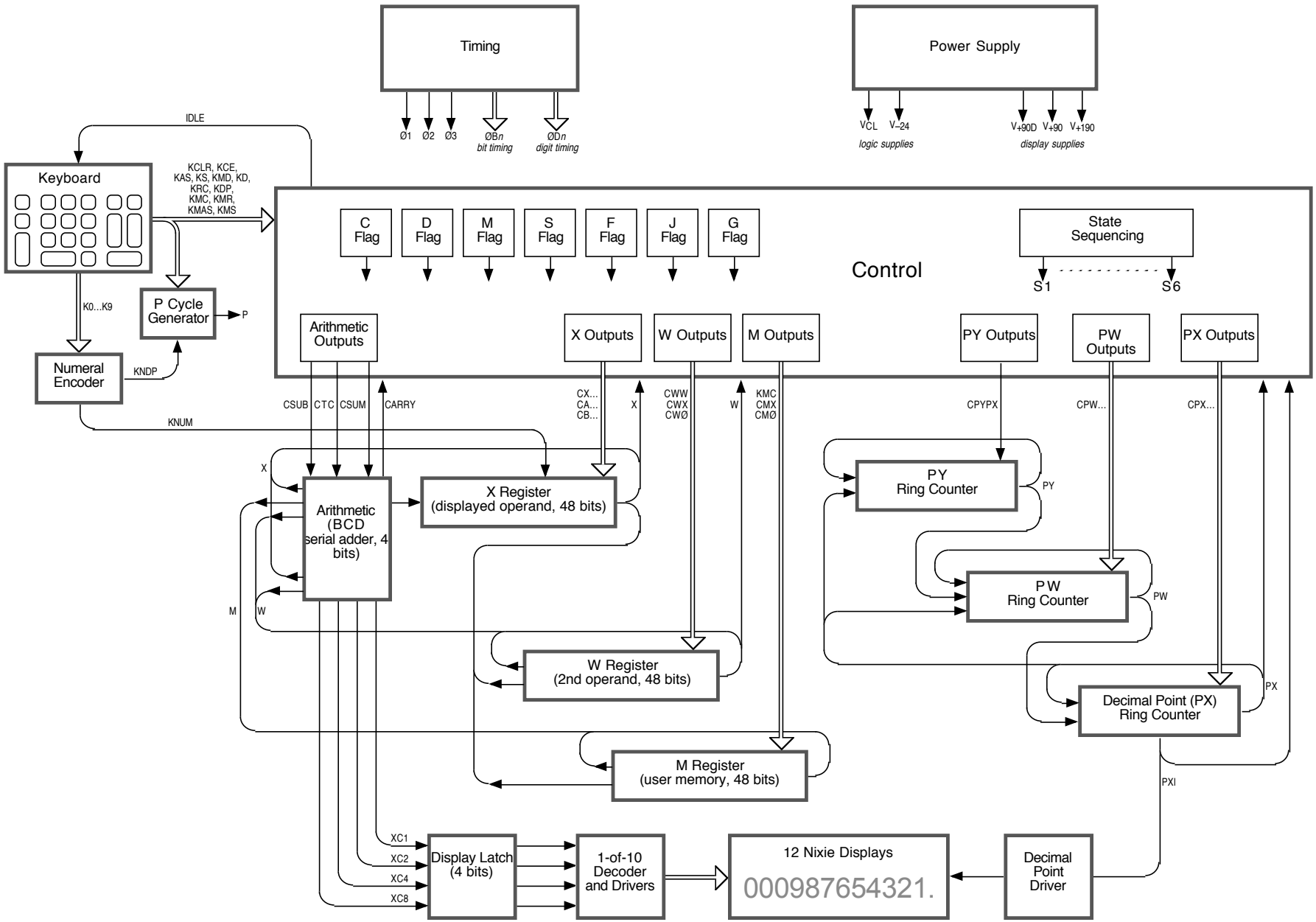
- A lowercase "n" in a symbol name indicates the logical NOT operation.
- The character "•" in a symbol name indicates the logical AND operation.
- The character "+" in a symbol name indicates the logical OR operation.

P-Cycles and Manual Control of Operations

Two switches can be plugged into the remote connector (NR) to provide the ability to single-step through the major state cycles of an operation. See the Keyboard page for wiring of the switches.

A P-cycle is a full number cycle during which processing occurs and is indicated by the P signal. Major state transitions occur at the end of a P-cycle. Simple user operations such as numeral entry generate a single P-cycle without sending IDLE to 0. More complex operations requiring multiple number cycles generate a first P-cycle and send IDLE to 0. Multiple P-cycles are subsequently generated until the operation is complete, at which time IDLE returns to 1.

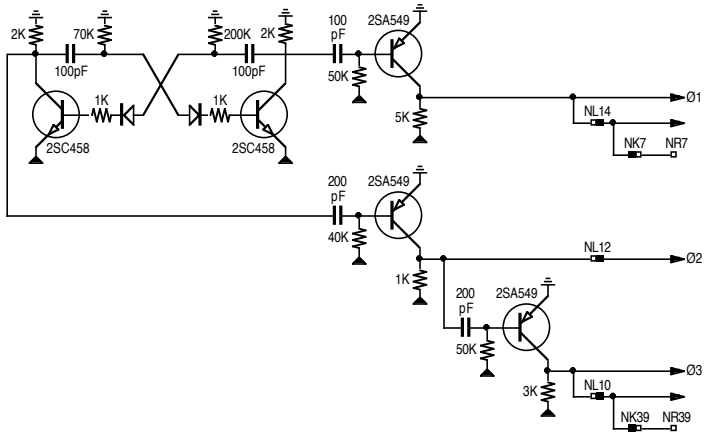
Enabling the MANUAL switch disables the automatic generation of P-cycles for multi-cycle operations. In this mode, once a multi-cycle operation has been initiated, each press of the STEP pushbutton generates a single P-cycle, so the operation can be stepped through one P-cycle at a time.

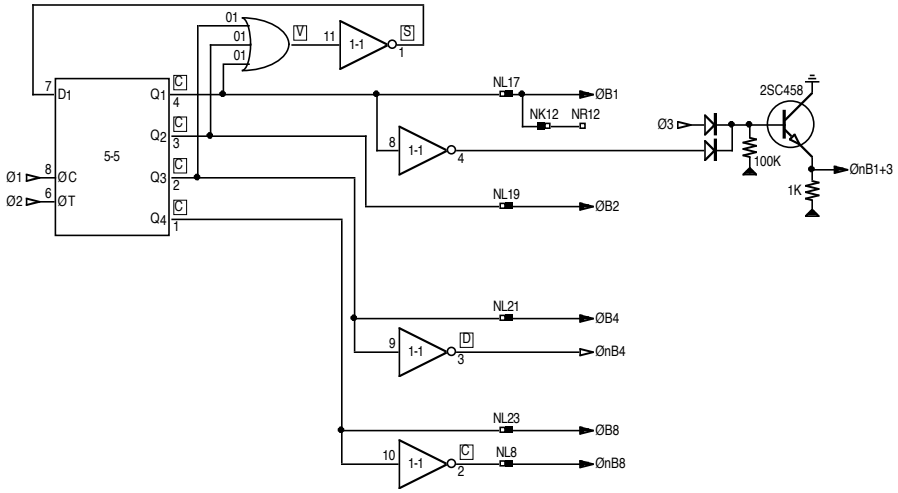


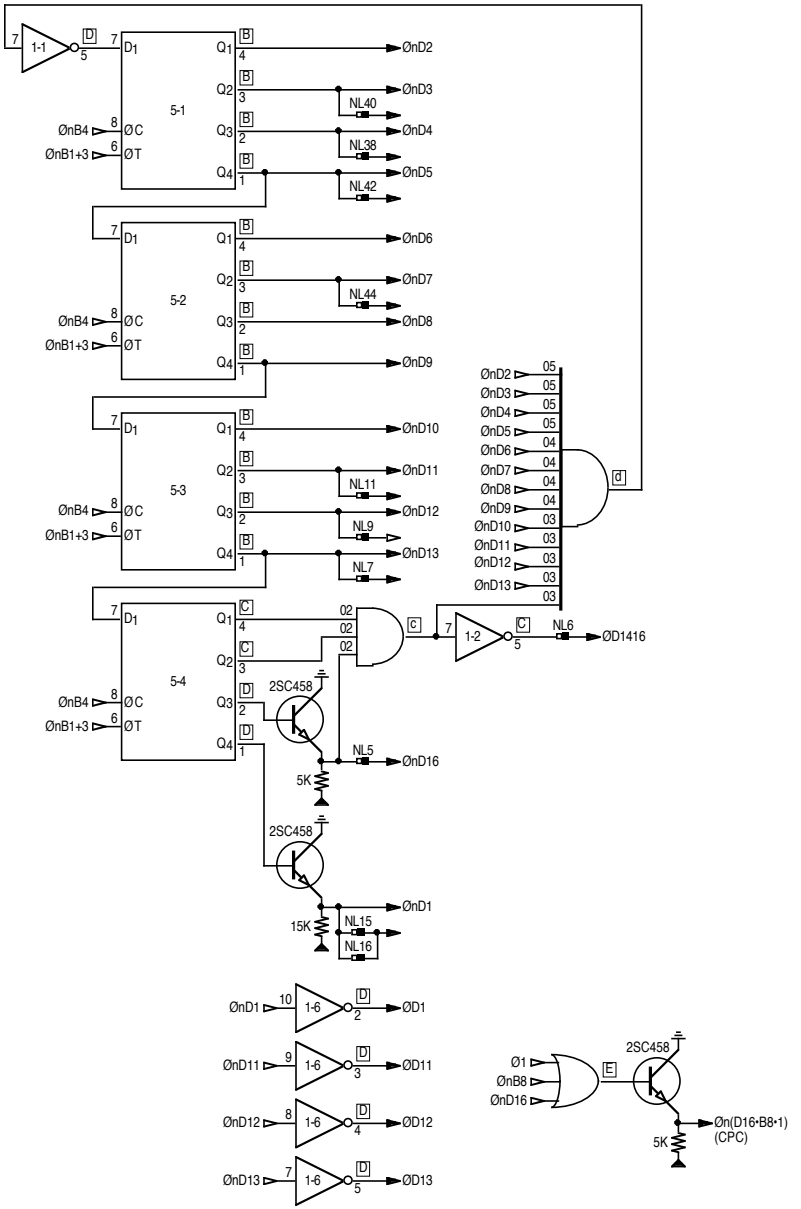
Sharp Compet 17 Calculator

Section: Block Diagram

Rendition: 2020 May 20







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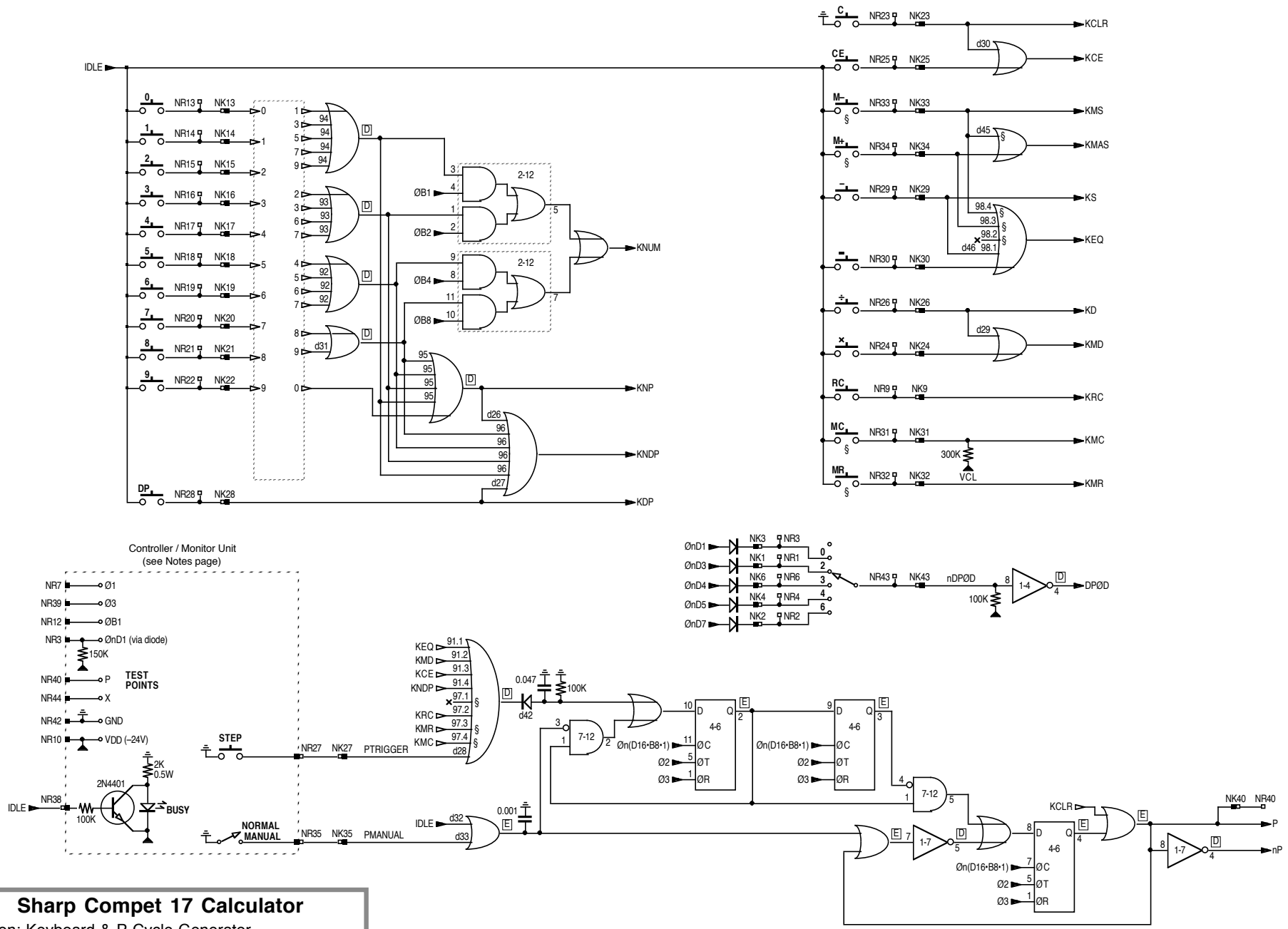
Section: Timing

Rendition: 2020 May 20



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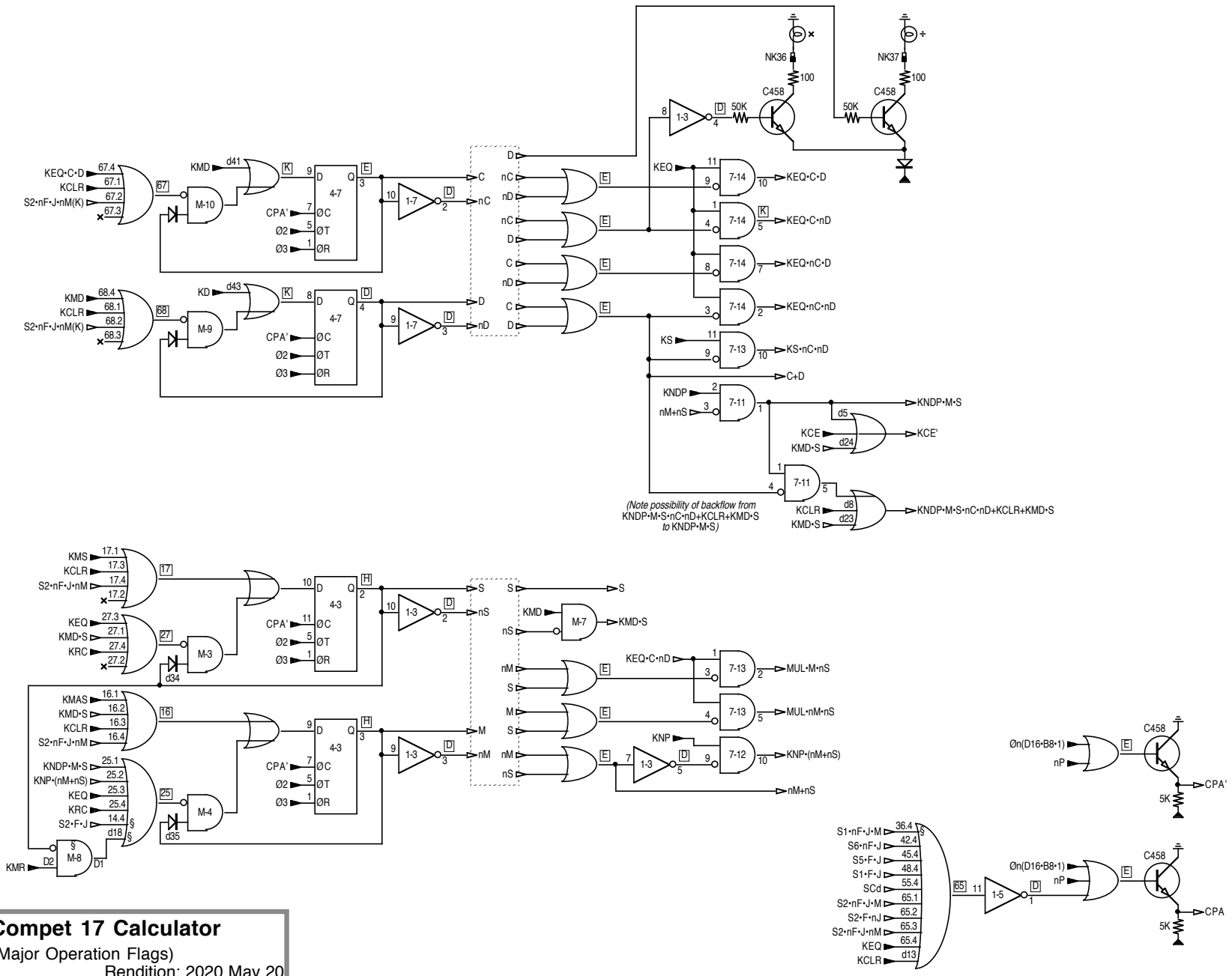
Section: Keyboard & P-Cycle Generator

Page: 5 Rendition: 2020 May 20



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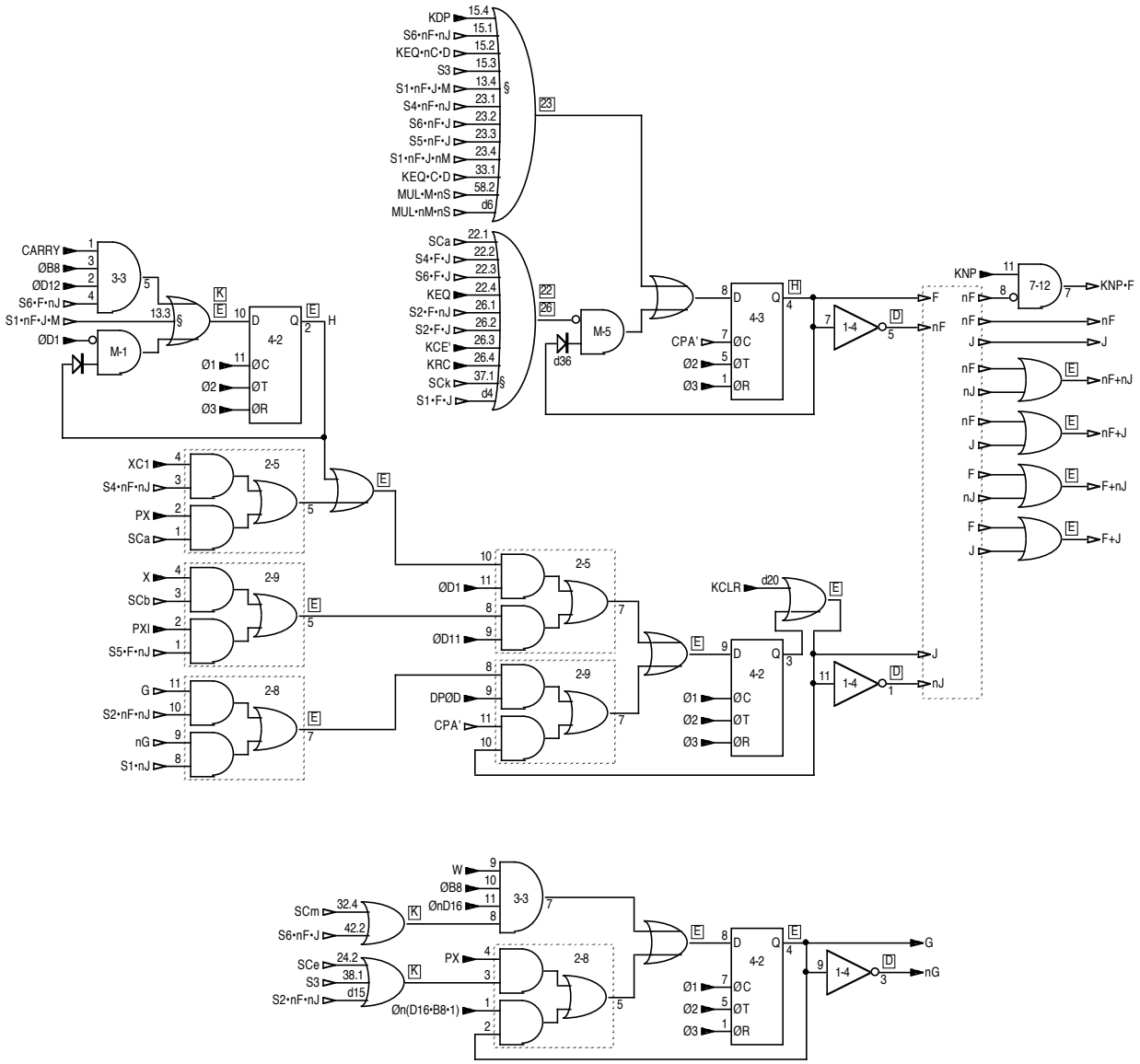
Section: Control (Major Operation Flags)

Page: 6 Rendition: 2020 May 20



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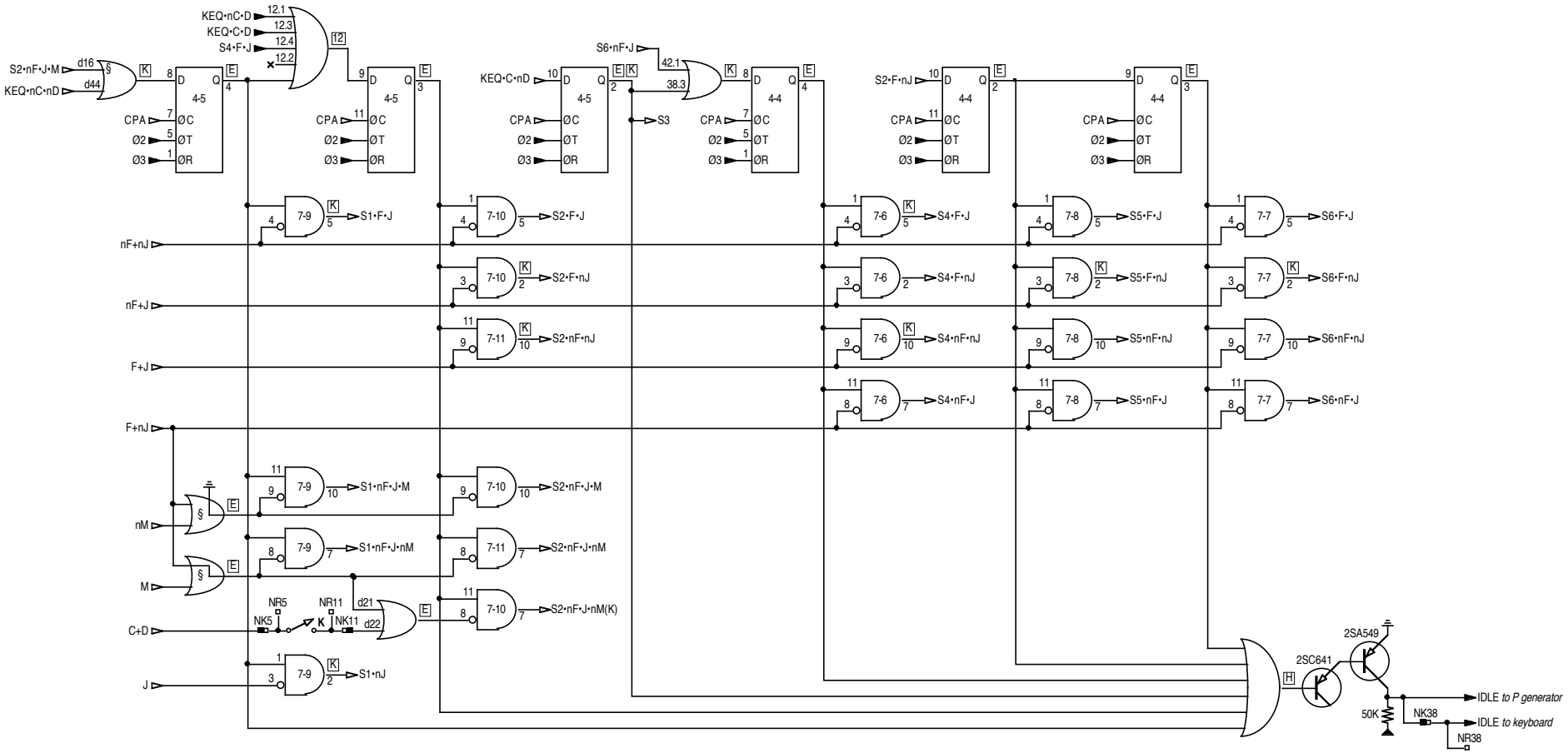
Section: Control (F, J & G Flags)

Page: 7 Rendition: 2020 May 20



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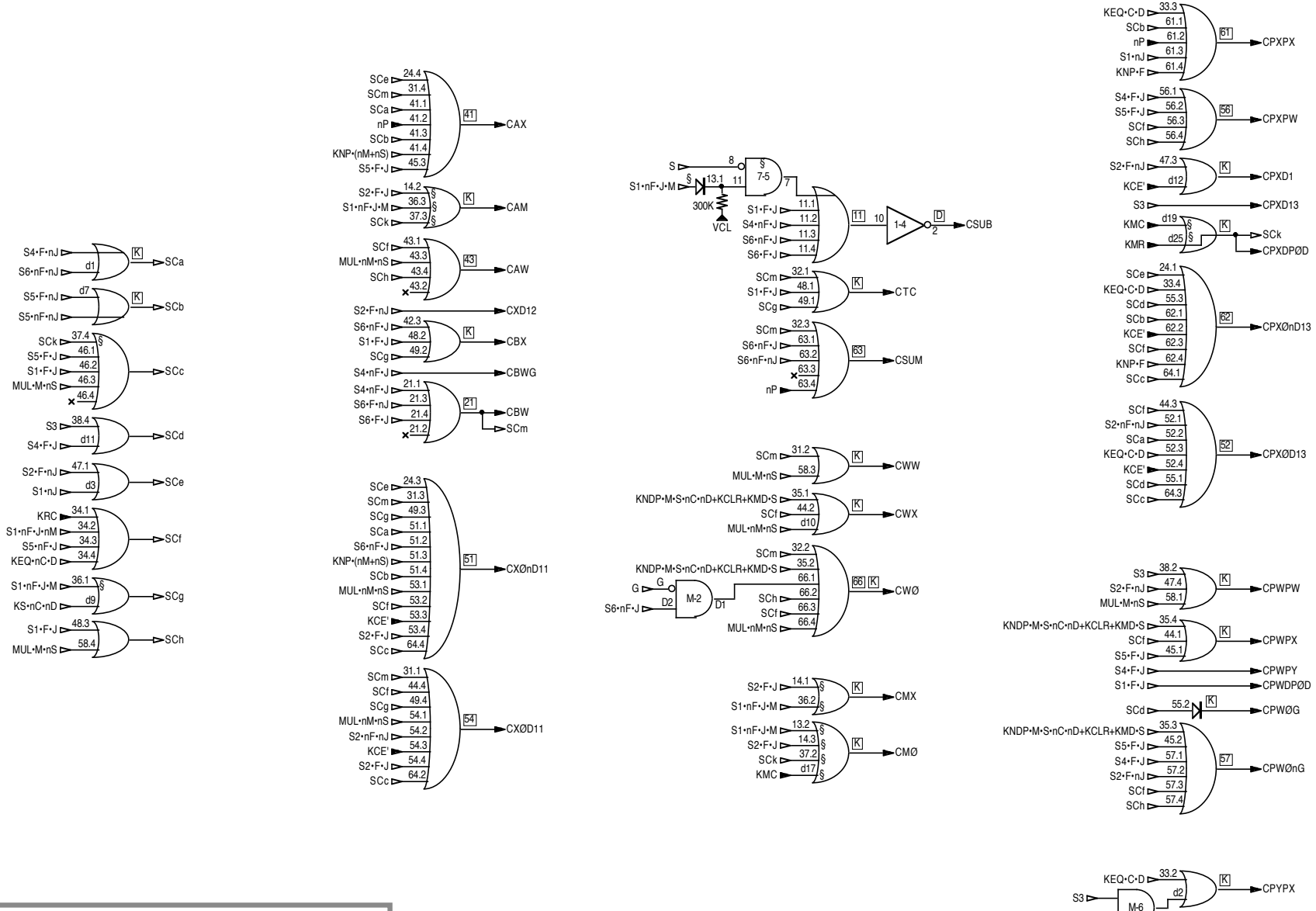
Section: Control (State Matrix)

Page: 8 Rendition: 2020 May 20



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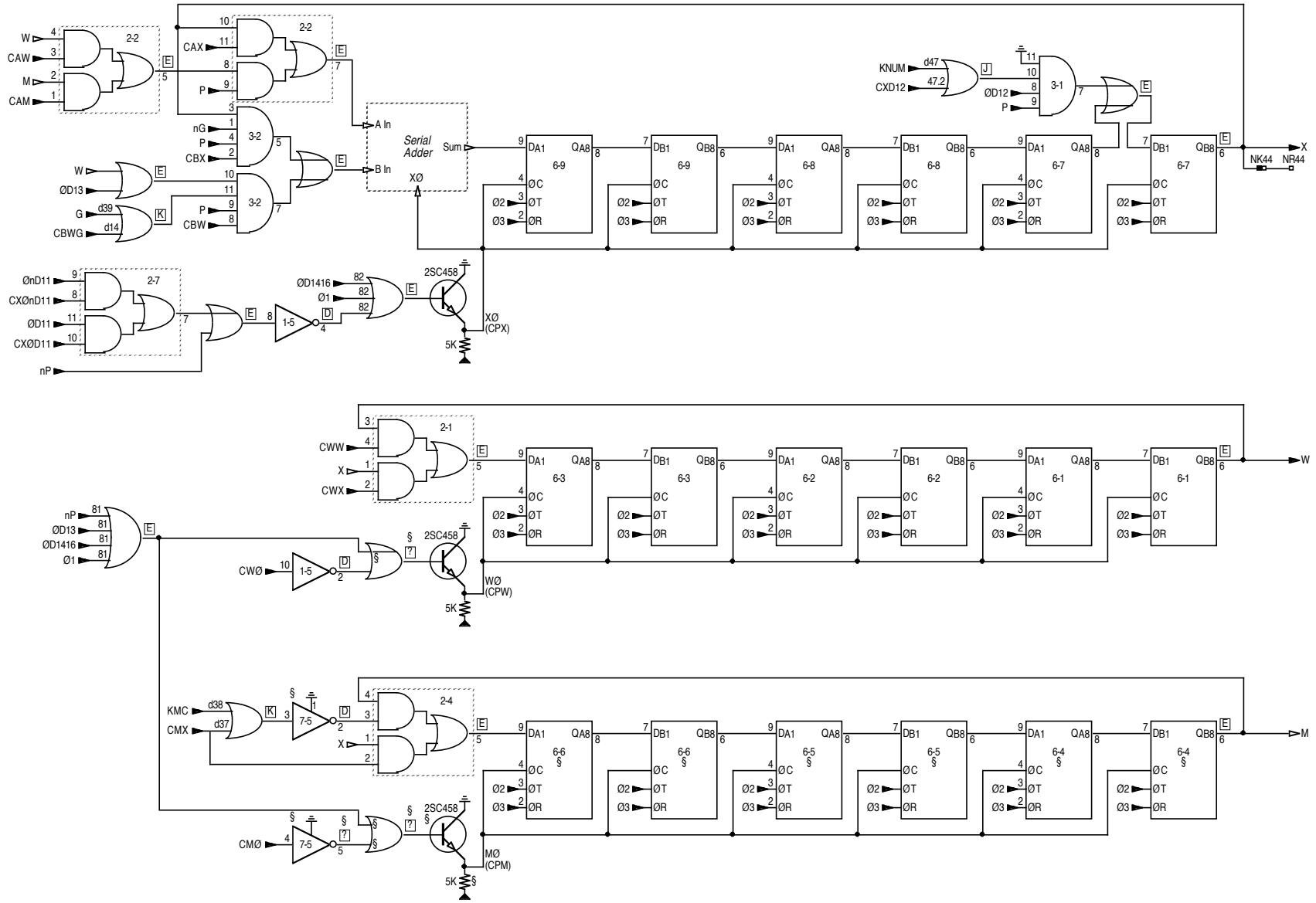
Section: Control (Outputs)

Page: 9 Rendition: 2020 May 20



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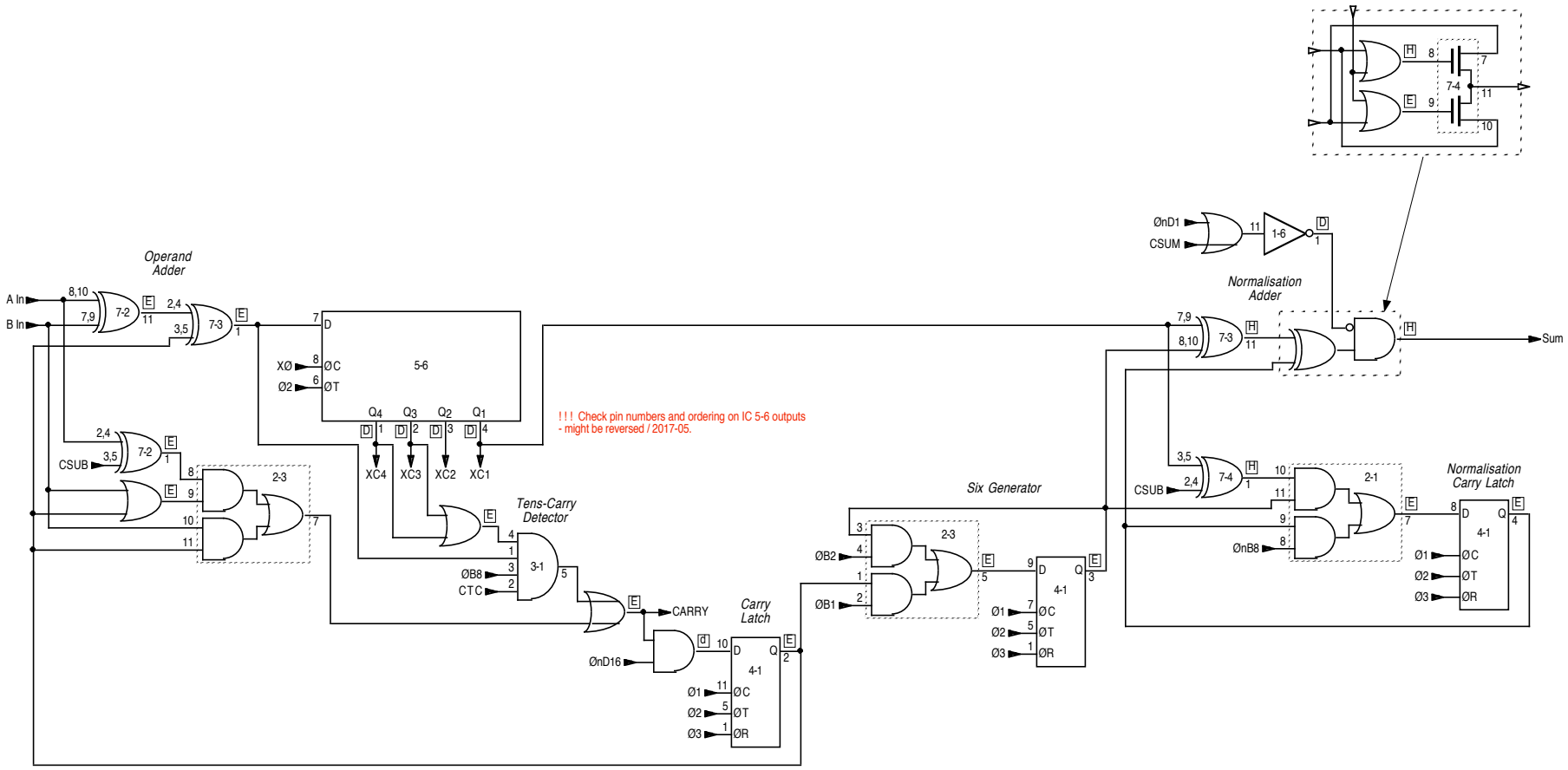
Section: Registers

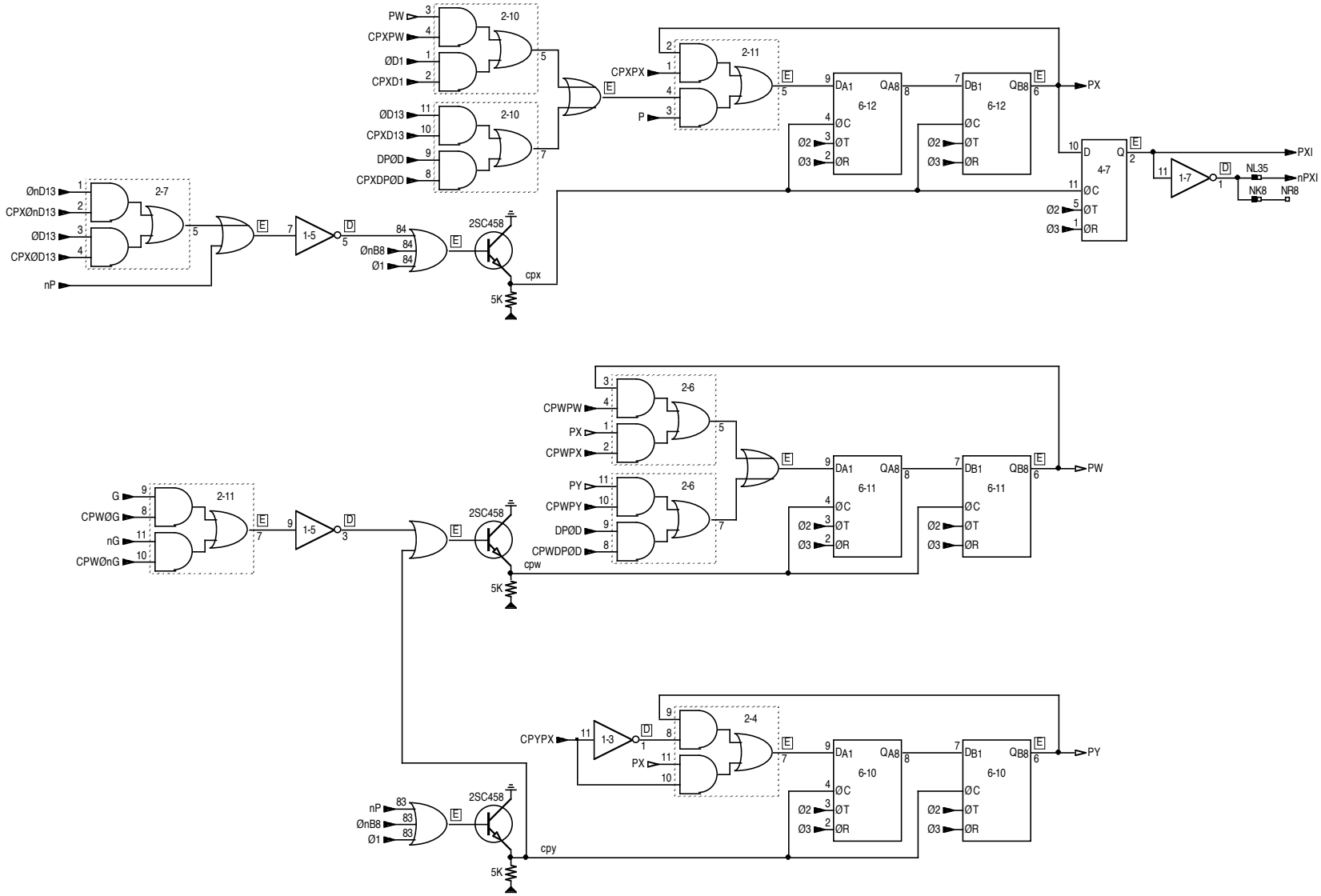
Page: 10 Rendition: 2020 May 20

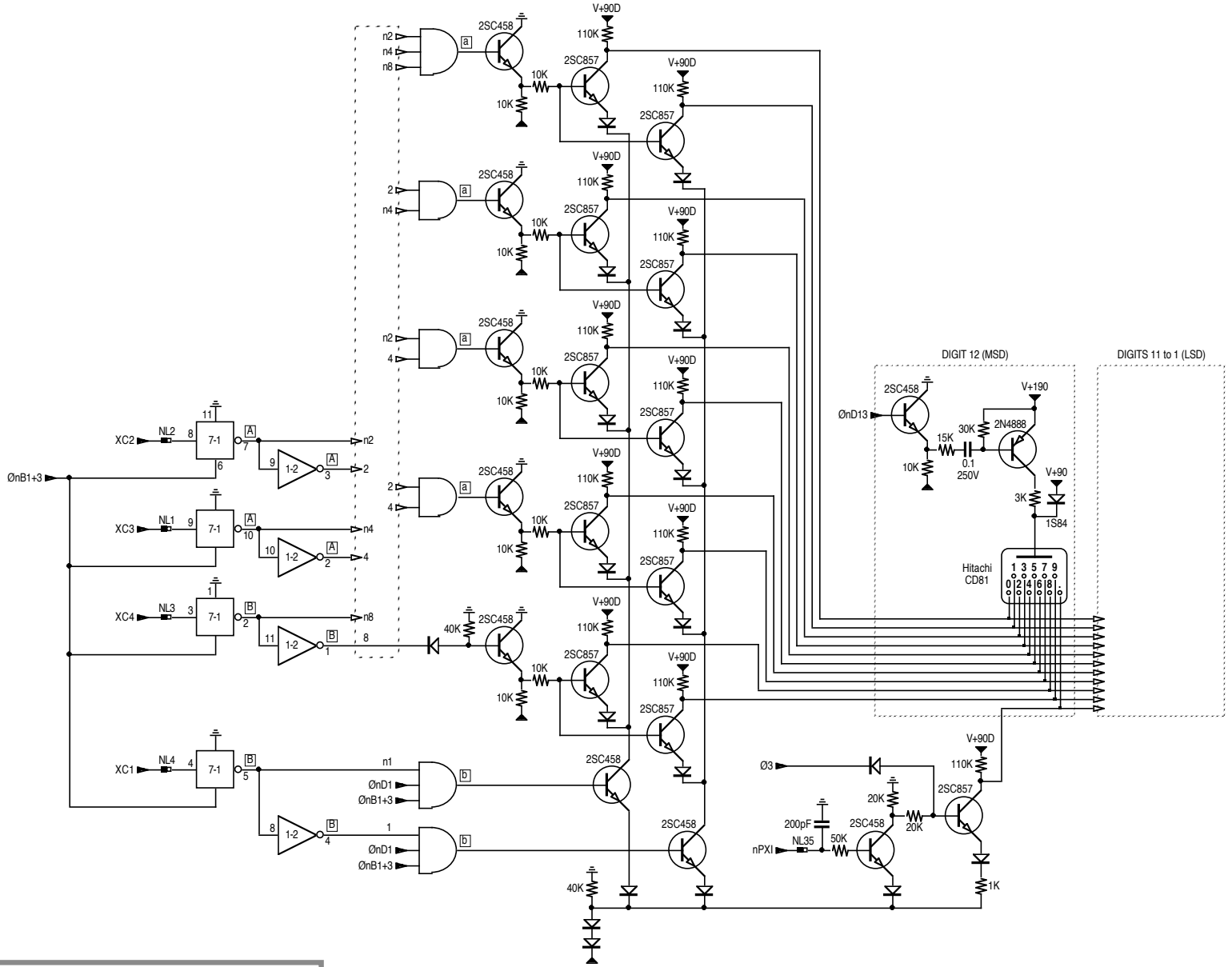


Sharp Compet 17 Calculator

Section: Arithmetic

Page: 11 Rendition: 2020 May 20

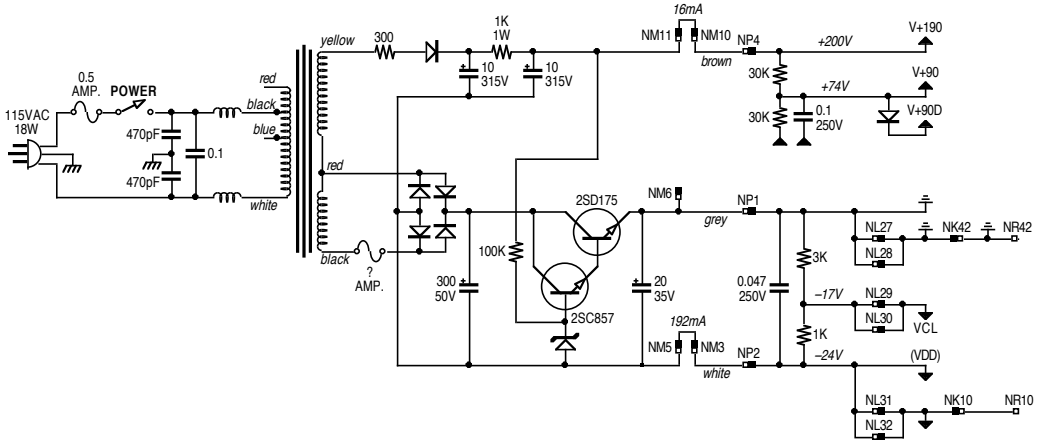

PW
CPXPW
ØD1
CPXD1
ØD13
CPXD13
DPØD
CPXDPØD
2-10
2-10
CPXPX
P
2-11
6-12
6-12
PX
4-7
PXI
nPXI
NL35
NK8
NR8
1-7
ØnD13
CPXØnD13
ØD13
CPXØD13
nP
2-7
1-5
ØnB8
Ø1
2SC458
cpx
5K
CPWPW
PX
CPWPX
PY
CPWPY
DPØD
CPWDPØD
2-6
2-6
6-11
6-11
PW
G
CPWØG
nG
CPWØnG
2-11
1-5
cpw
5K
CPYPX
PX
2-4
6-10
6-10
PY
nP
ØnB8
Ø1
2SC458
cpy
5K

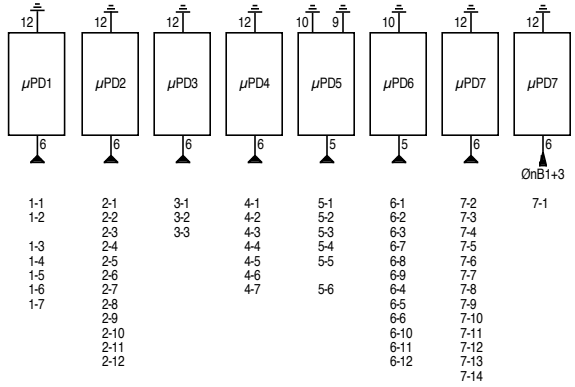


Sharp Compet 17 Calculator

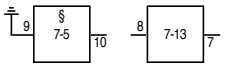
Section: Display

Page: 13 Rendition: 2020 May 20





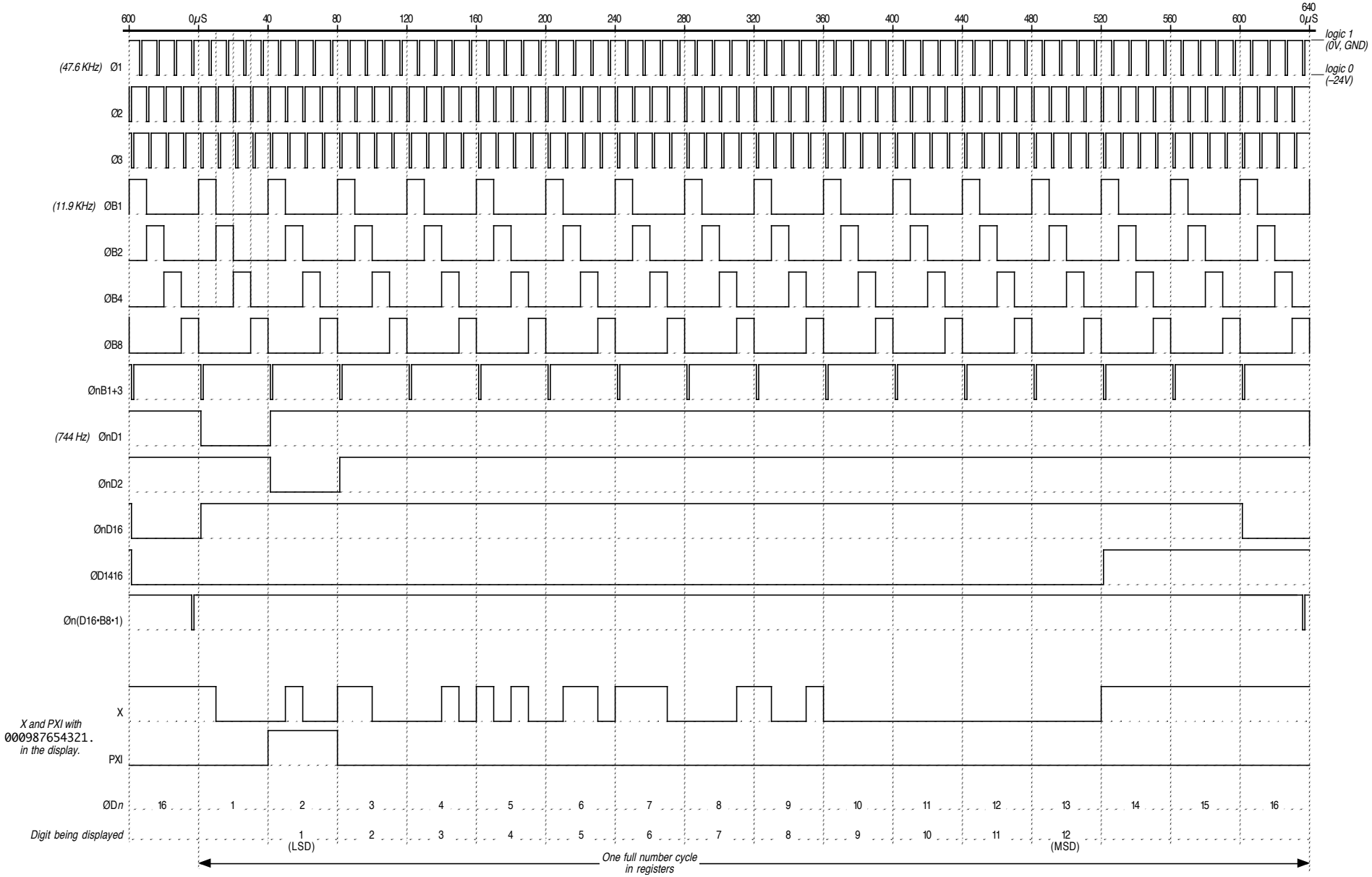
Unused Elements



Sharp Compet 17 Calculator

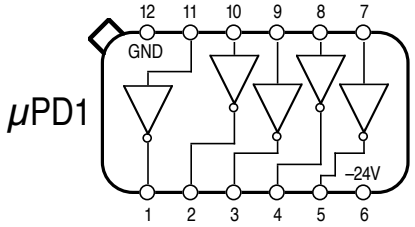
Section: Power Supply

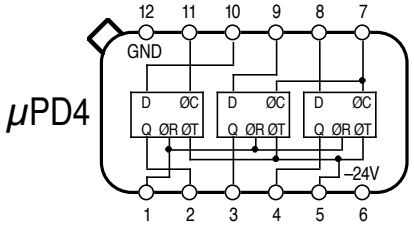
Rendition: 2020 May 20

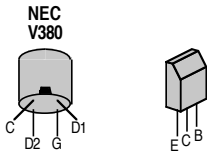

600
0μS
40
80
120
160
200
240
280
320
360
400
440
480
520
560
600
640
0μS
logic 1
(0V, GND)
logic 0
(–24V)
(47.6 KHz) Ø1
Ø2
Ø3
(11.9 KHz) ØB1
ØB2
ØB4
ØB8
ØnB1+3
(744 Hz) ØnD1
ØnD2
ØnD16
ØD1416
Øn(D16•B8•1)
X and PXI with
000987654321.
in the display.
X
PXI
ØDn
16 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
Digit being displayed
1 2 3 4 5 6 7 8 9 10 11 12
(LSD)
(MSD)
One full number cycle
in registers

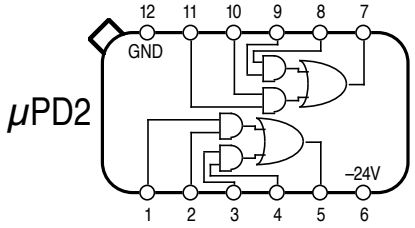
The μPD Integrated Circuit Family

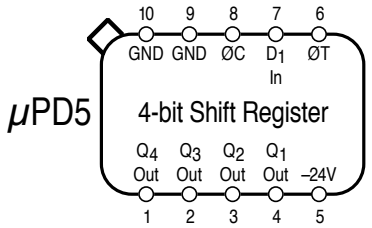
- Based on supply voltage, circuit impedances and logic density, IC technology is presumed to be early MOS.
- Gate symbols are presented in accordance with:
  logic 1 = 0V, GND
  logic 0 = –24V
- Outputs are open-collector, closing to GND (logic 1) and requiring external pull-down resistor to –24V (logic 0).
- Inferred for flip-flops:
  The flip-flops in this logic family appear to be Master/Slave D-type flip-flops with the clocks for the master and slave sections kept separate. This permits a system design where data capture is done in accordance with the requirements of the logic while all outputs are changed synchronously by a single clock signal.
  ØC = Capture Input (master section clock)
  ØT = Transition Input (slave section clock)
  The state of the D input is captured when ØC is logic 0 (–24V).
  The Q output is set in accordance with the captured state when ØT goes to logic 0.

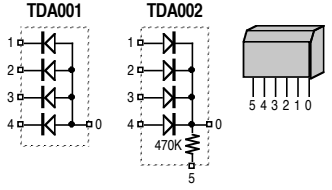


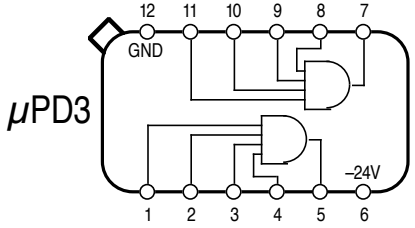


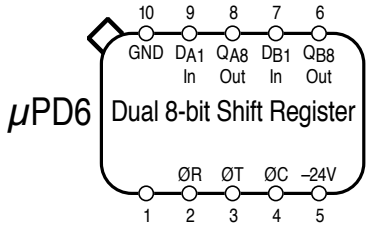


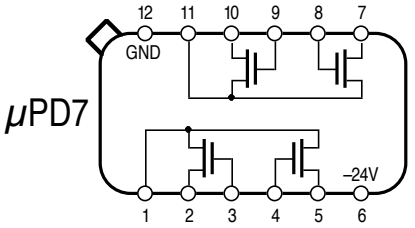






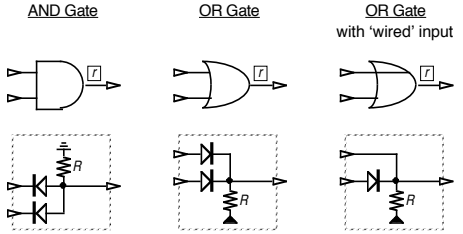






Discrete Gate Construction

Most OR and some AND gates are constructed from discrete diodes and resistors. More complex logic elements are contained in integrated circuits. The internal construction of discrete gates is shown in the following diagrams. A wire–OR or wire–AND construction is indicated by the input line traversing the width of the gate.

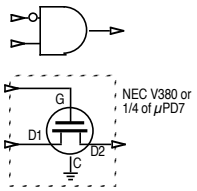


The diodes and resistors may be individual components or contained in TDA001 and TDA002 packages.

Most gate outputs have load resistors (*R*) connected from the output to one side of the power supply. To reduce clutter these resistors are indicated in the schematic by one of the following letters (*r*) in a box near the output.

Symbol (*r*)	Resistance (*R*)
A	15K to VDD
B	20K to VDD
C	30K to VDD
D	50K to VDD
E	100K to VDD
H	150K to VDD
J	300K to VDD
K	300K to VCL
nn	470K to VCL, internal to TDA002 unit *nn*
a	40K to GND
b	60K to GND
c	100K to GND
d	300K to GND

Occasionally individual MOSFET transistors or MOSFETs contained in μPD7 ICs are used as AND gates. The gate of these transistors functions as an inverted input. Because the MOSFET is a bidirectional device, a diode is usually required on the other input or the output to prevent 'backflow' of the signal.



Special mention must be made of the unusual use of a μPD7 for the 4-bit display latch. Controlling pin 6 allows it to function as a sample-and-hold latch, presumably relying on inter-electrode capacitance to hold the state between digit updates (see Display).

NR

1	ØnD3	17	*key 4*	30	KEQ
2	ØnD7			31	KMC §
3	ØnD1	18	*key 5*	32	KMR §
4	ØnD5	19	*key 6*	33	KMS §
5	*K*	20	*key 7*	34	KMAS §
6	ØnD4	21	*key 8*	35	PMANUAL
7	Ø1	22	*key 9*	36	—
8	nPXI	23	KCLR	37	—
9	*key RC*	24	KMD	38	IDLE
10	VDD	25	KCE	39	Ø3
11	*K*	26	KD	40	P
12	ØB1	27	PTRIGGER	41	—
13	*key 0*	28	KDP	42	GND
14	*key 1*			43	nDPØD
15	*key 2*	29	KS	44	X
16	*key 3*			45	—

• Italicised expressions are connections with no signal name in the schematic.

• ØnDx signals on the NK and NR connectors have a diode between the connector and the actual signal. See the Keyboard page.

• The NK and NR connector pins are numerically correlated.

NL

XC3	1	2	XC2
XC4	3	4	XC1
ØnD16	5	6	T
ØnD13	7	8	ØnB8
ØnD12	9	10	Ø3
ØnD11	11	12	Ø2
—	13	14	Ø1
ØnD1	15	16	ØnD1
ØB1	17	18	—
ØB2	19	20	—
ØB4	21	22	—
ØB8	23	24	—
—	25	26	—
GND	27	28	GND
VCL	29	30	VCL
VDD	31	32	VDD
—	33	34	—
nPXI	35	36	—
—	37	38	ØnD4
—	39	40	ØnD3
—	41	42	ØnD5
—	43	44	ØnD7

NK

ØnD3	1	2	ØnD7
ØnD1	3	4	ØnD5
K	5	6	ØnD4
Ø1	7	8	nPXI
KRC	9	10	VDD
K	11	12	ØB1
key 0	13	14	*key 1*
key 2	15	16	*key 3*
key 4	17	18	*key 5*
key 6	19	20	*key 7*
key 8	21	22	*key 9*
KCLR	23	24	KMD
KCE	25	26	KD
PTRIGGER	27	28	KDP
KS	29	30	KEQ
§ KMC	31	32	KMR §
§ KMS	33	34	KMAS §
PMANUAL	35	36	*lamp **
lamp ÷	37	38	IDLE
Ø3	39	40	P
—	41	42	GND
nDPØD	43	44	X