

Sony SOBAX 2500 Calculator

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Notes

- The symbol ▼ denotes V+4.
- —▶ connection between different sections.
—▶ connection limited to same section.
Arrows indicate direction of signal or energy flow.
- A lowercase 'n' at the beginning of a symbol name indicates the logical NOT operation.
- Resistance in ohms unless otherwise indicated.
- Capacitance in microfarads unless otherwise indicated.
- The Acoustic Delay Line is based on magnetostrictive principles.
See the article "Magnetostrictive Delay Lines" in "Electronics World", Jan. 1964.
- These drawings based on unit with Serial No. 620173 which contains a Board F marked with 1-539-224-12. Component values marked with "*" are the values for Board F marked with 1-539-224-11.

Log

- 1999 Sep-Nov: Initial drawing / bhilpert.
- 2005 Feb 19: MSYNC source corrected, comes from Q7 rather than Q8. Corrections to labels on flip-flops in display page.
- 2005 Feb 20: Some additional labeling of "*" components for board F.
- 2014 May: Backplane connectors correction for V+4/GND, numeric key coupling distinguished, other minor reorganisation.

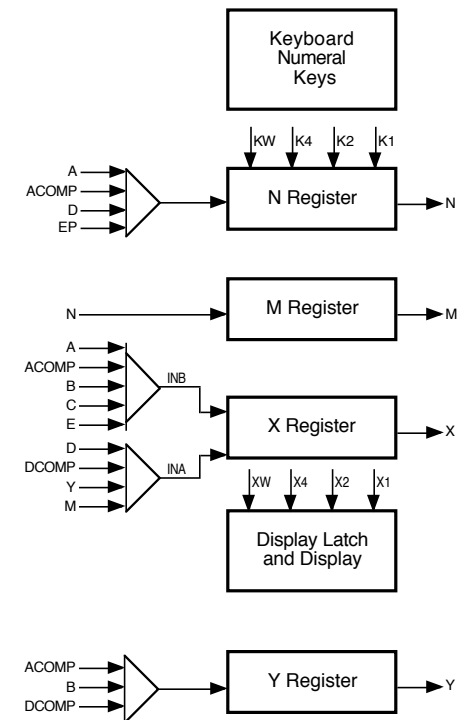
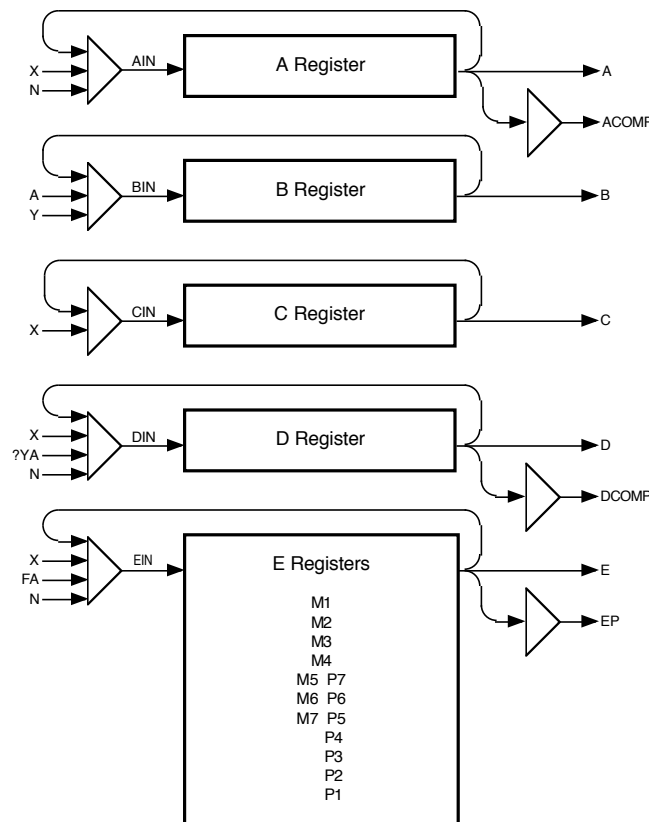
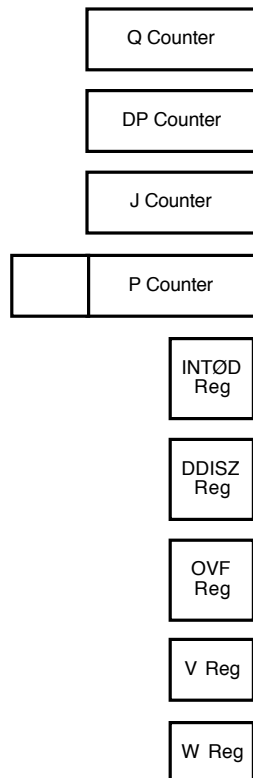
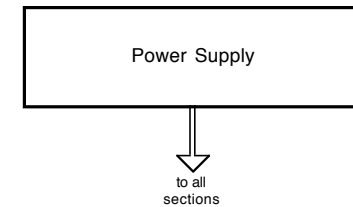
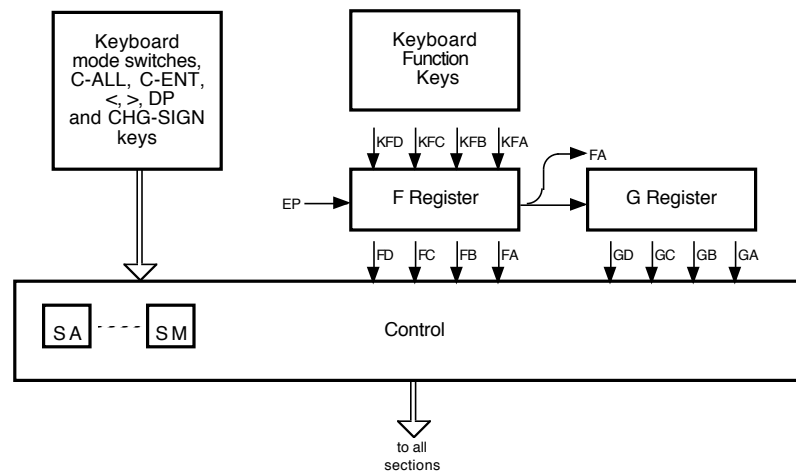
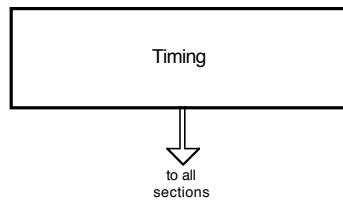
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Section: Title & Contents

Page: 1

Rendition: 2014 May 7

This schematic has been derived through reverse engineering.
This is not the manufacturer's schematic, nor is it based on the manufacturer's schematic.



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Section: Block Diagram
Page: 2

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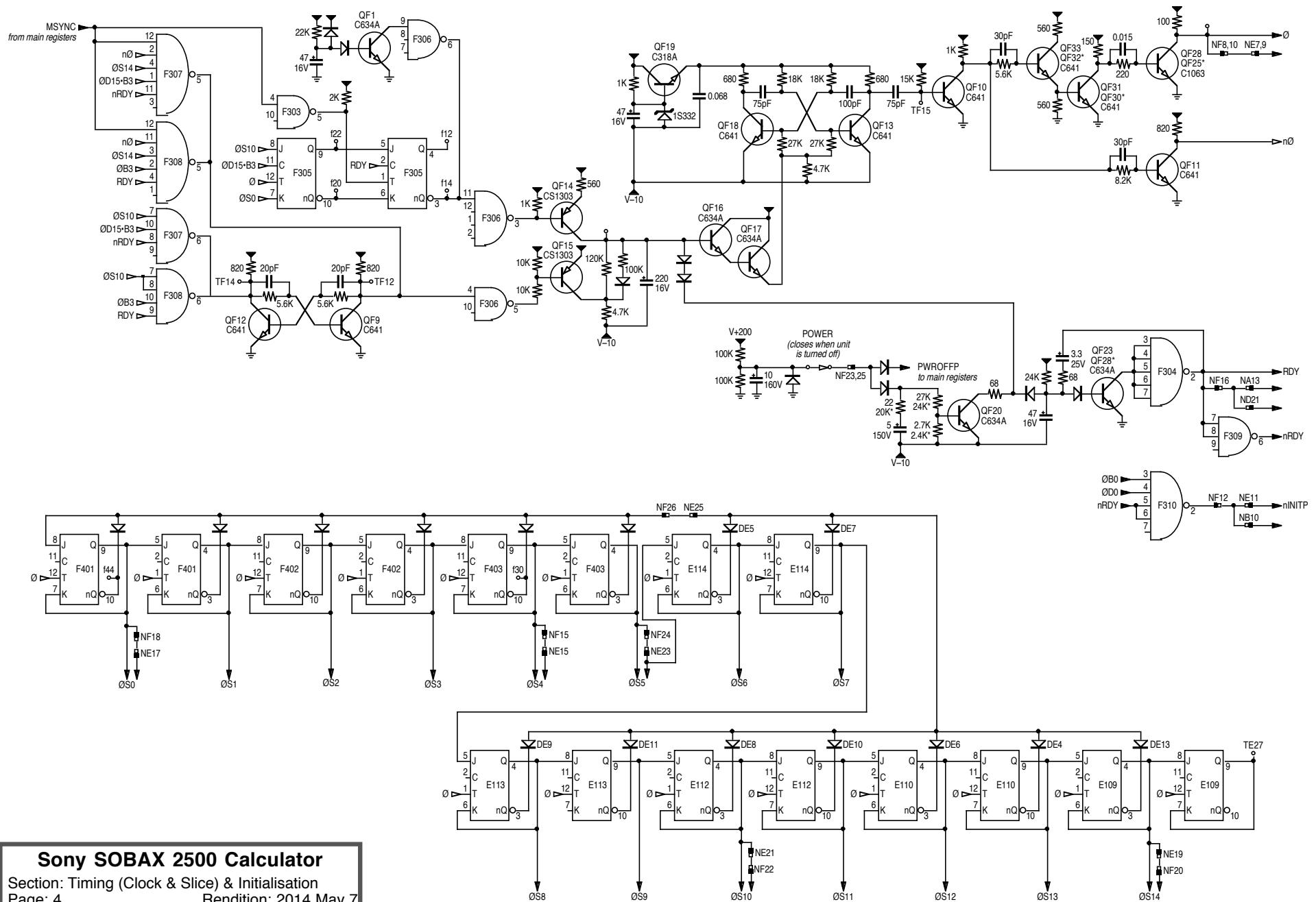
Section	Signal	Description
Timing		Master timing and power-on initialisation.
	Ø	Master clock.
	ØS...	Sliced bit timing. The bits of the 15 main registers are interleaved in the Acoustic Delay Line by slicing each 'major' bit into 16 parts. The remaining slice is used for synchronizing the frequency of the master clock to the cycle time of the delay line.
	ØB...	'Major' bit timing.
	ØD...	Digit timing (4 major bits constitutes a digit).
	ØDINS	During some calculation phases, the 16-digit cycle is extended one digit period by inserting another 'digit' between ØD11 and ØD12. The inserted period is ØDINS.
	RDY	Ready. Low when power is turned on, goes high after initialisation is complete.
	INITP	Initialisation pulses. A stream of pulses during initialisation (not-ready).
	PWROFFP	Power Off Pulse.
Keyboard		The keyboard and encoders for numerals and functions.
	KMAN	Manual mode.
	KAUTO	Execute program mode.
	KLEARN	Learn program mode.
	KOPER	Operate mode.
	KCHECK	Check program mode.
	KMAO	Manual / Auto / Operate.
	KTON	Tally mode on.
	KTREAD	Tally read.
	KR54	5 up / 4 down rounding mode.
	KRDWN	Round down mode (truncate).
	KRØD	Selected digit pulse for rounding.
	KCA	Clear all.
	KCE	Clear entry.
	KSL	Shift left.
	KSR	Shift right.
	KSCS	Shift or change sign.
	KDP	Decimal point.
	KPS	Program step (S key).
	KFA,KFB,KFC,KFD	Encoded function keys. These are the same as FA, FB, FC, FD.
	K1,K2,K4,KW	Encoded numeral keys.
Control		Control registers & logic.
	F...	4 bit register for function keystrokes and program instructions to be executed.
	G...	Secondary function register loaded from the F register.
	S...	Assorted state registers.
		All these registers clock on a 16-digit cycle (17 when ØDINS active).
	T...	Misc control logic. These are combinations of the state registers.
	U...	More control logic. These are combinations of the function register and state registers.
	AISNEG	Indicates the number in the A register is negative. (Appears to also be used for other purposes).
	DISNEG	Indicates the number in the D register is negative.
	ANEGJ	
Q Counter		16 squared counter. Counter for 16 cycles of 16 or 17 digits.
	Q QA	
DP Counter		Decimal point timing counter.
	DP	Signal to the display to turn on the decimal point at the appropriate times.
	UNITØD CHGSGN	Pulses during the digit which is currently the units digit. Change Sign.
J Counter		Multi-use counter for fraction fill count, digit position to start zero blanking and more.
	J JA, JB, JC	

Section	Signal	Description
P Counter		The program counter. This must select one of the 7 program registers in the E group as well as track a position within the selected register.
	PØS	Timing slice for selecting 1 of 7 program registers in the E register group.
	P1ST	Program at beginning.
	PEXP	Program memory expended.
	POVF PA	
N Register		4-bit register for numeric keystrokes.
	N	Bit stream from the N register.
	NPRESS NPRESSA	Numeric key has been pressed.
M Register		4-bit register to indicate which memory is currently selected.
	M	Bit stream from the M register.
	MØS	Timing slice for selecting 1 of 7 memory registers in the E register group.
	MEM1	Memory 1 is selected.
Main Data Switches		Data switches to select inputs to the Main Registers.
	AIN	Bit stream into the A register.
	BIN	
	CIN	
	DIN	
	EIN	
	EIN_ENB	Enable the input to the currently selected register in the E register group.
	ACOMP	Complementary form of bit stream from the A register in accordance with AISNEG.
	DCOMP	Complementary form of bit stream from the D register in accordance with DISNEG.
	EP	Bit stream from the E register for program instruction purposes.
Main Registers		15 16-digit registers for the operands and program instructions.
	A	Bit stream from the A register. The A register mimics the D register but with zeroes (1000) mapped to 0000.
	B	Bit stream from the B register.
	C	Bit stream from the C register.
	D	Bit stream from the D register. The D register contains the number being displayed. Displayed zeroes are encoded as 1000 and blanked zeroes as 0000.
	E	11 16-digit registers shared between the 7 memories and program instructions. 4 of these registers are reserved for memories 1,2,3 and 4. 4 are reserved for program instructions. The remaining 3 are shared by memories 5,6,7 and program instructions in reverse overlapping order. Thus a long program will cut into memory 7, then memory 6 then 5.
	MSYNC	The maximum length of a program is (4+3)*16=112 instructions (functions). Signal from the delay line to automatic frequency control circuit for the master clock.
X Register		4-bit register for arithmetic and transferring numerals on their way from the D register to the display.
	X	Bit stream from the X register.
	X1,X2,X4,XW	Numerals on their way to the display.
	XOVF CA	Carry Flag.
Y Register		4-bit register.
	Y	
	YR54 YA,YB,YC	
Misc. Registers		Goes high during digits which are part of the integral portion of the number.
	INTØD RNDØD	
	DDISZ	Output from a register which assesses whether the current register D digit is zero.
	OVF	Overflow latch.
	V	1-bit register.
	VA,VB,VC	
	W	1-bit register.

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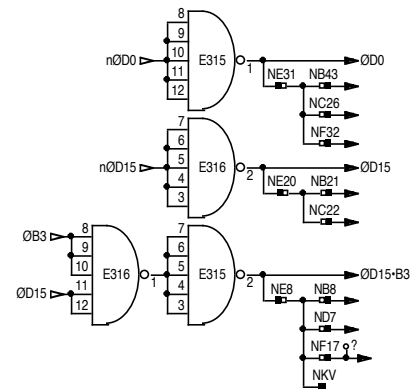
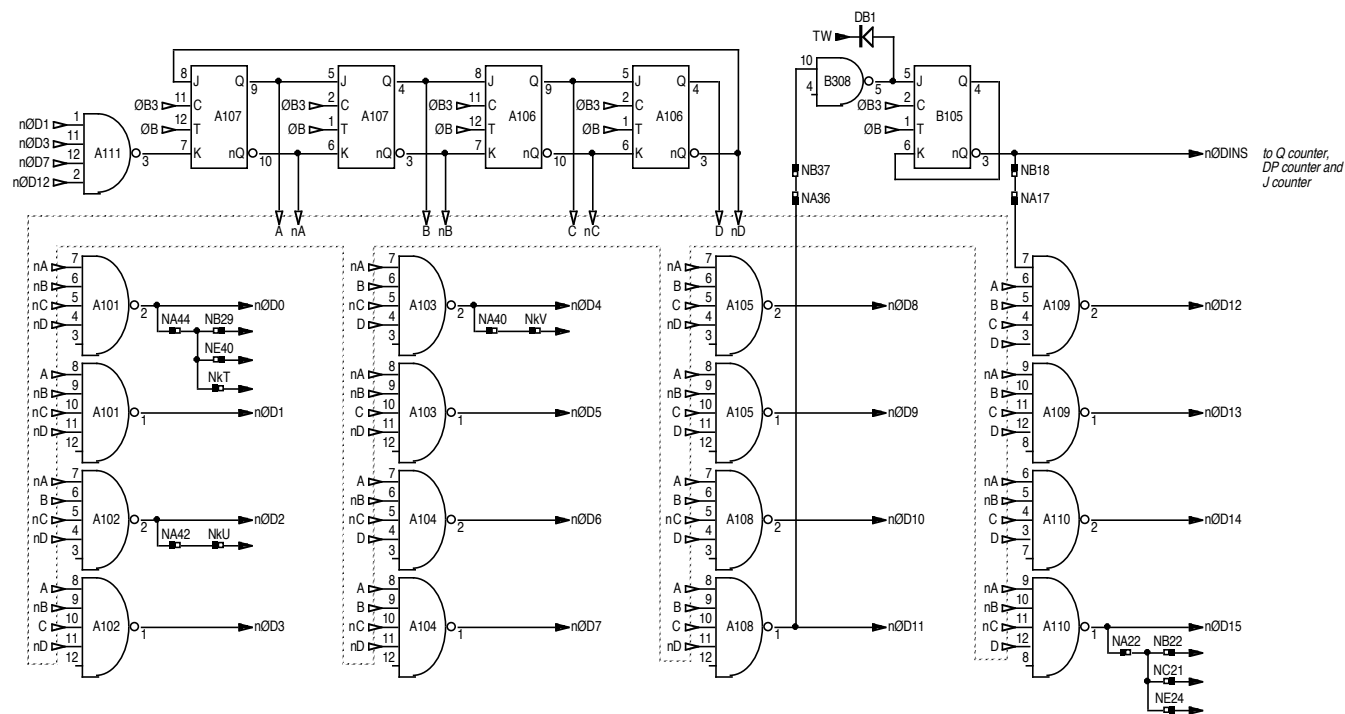
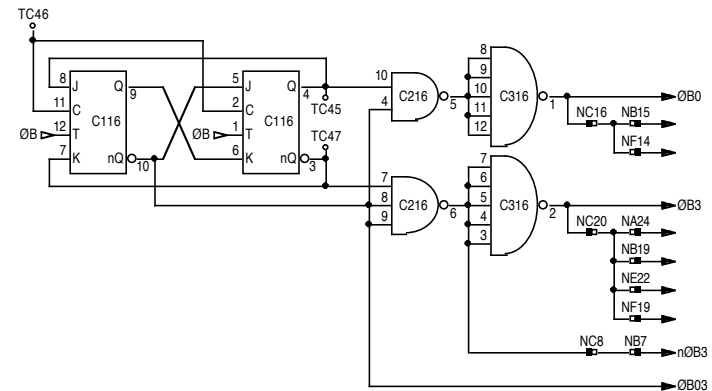
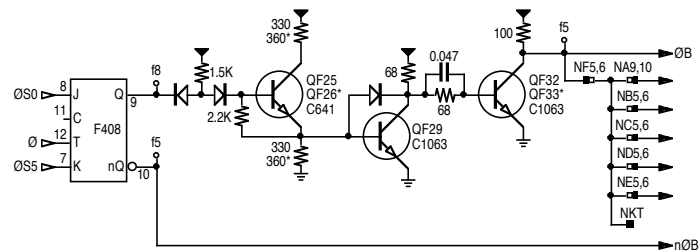
Section: Section & Signal Name Descriptions

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Section: Timing (Clock & Slice) & Initialisation
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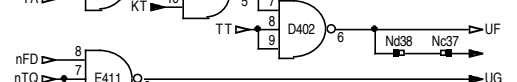
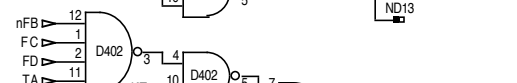
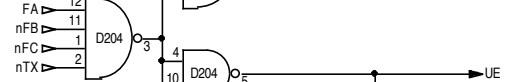
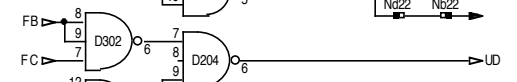
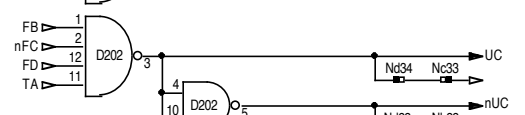
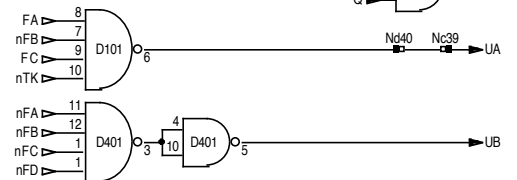
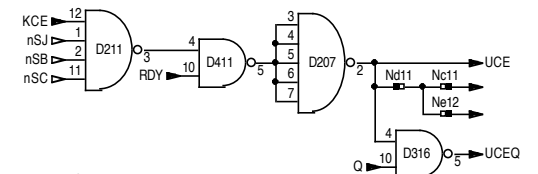
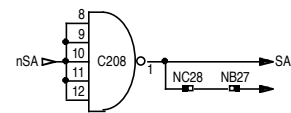
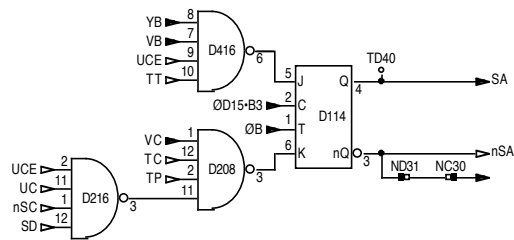
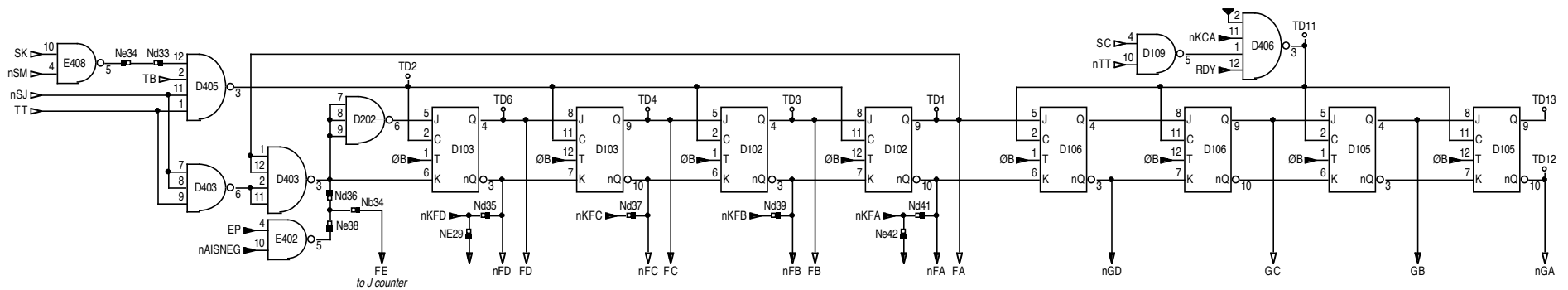


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Section: Timing (Bit & Digit)

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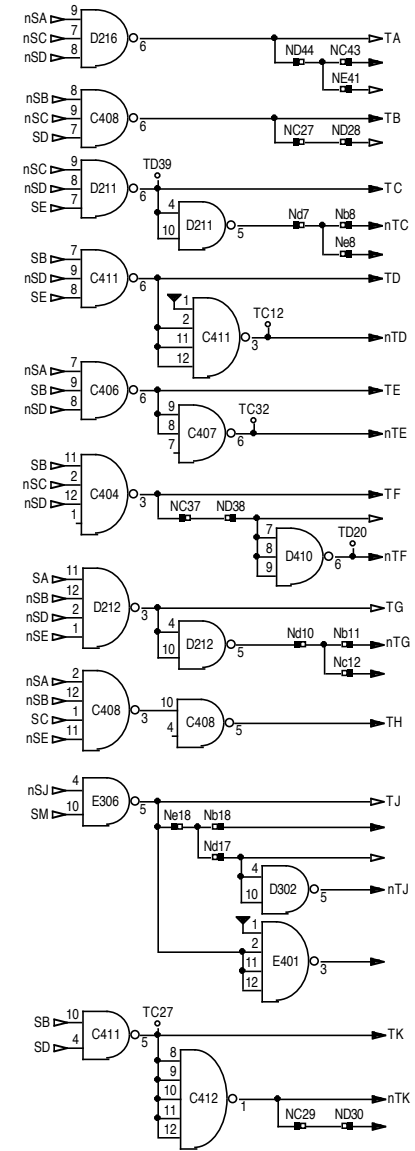
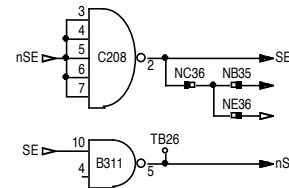
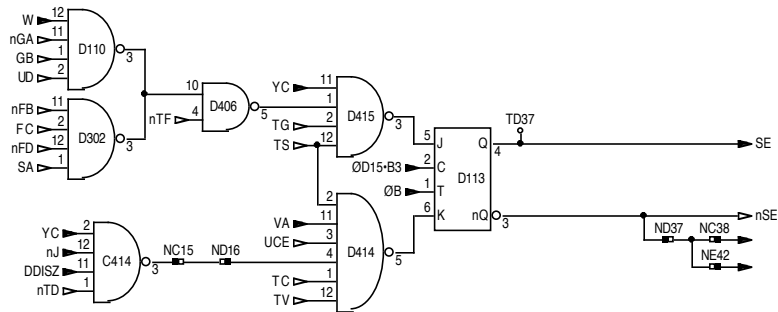
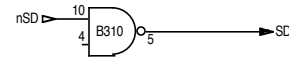
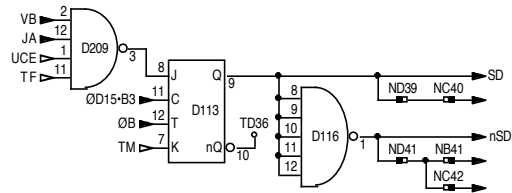
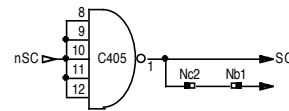
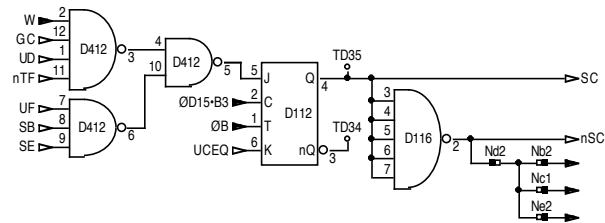


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Section: Control (part 1)

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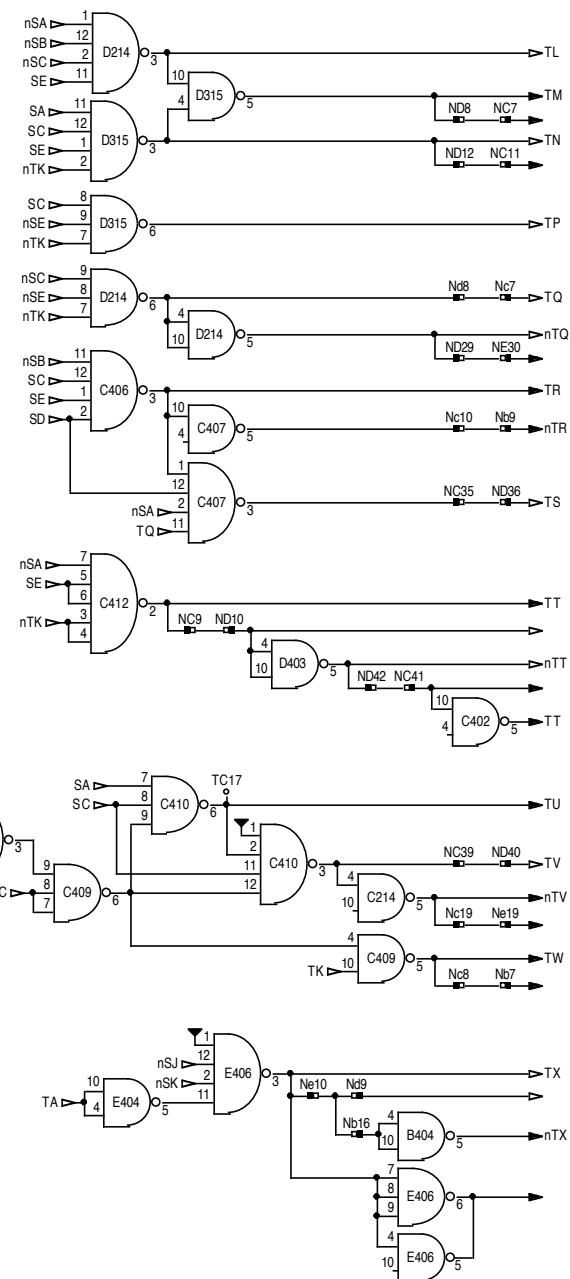
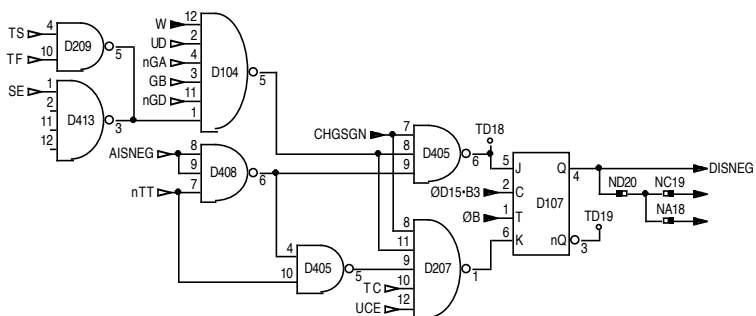


Sony SOBAX 2500 Calculator

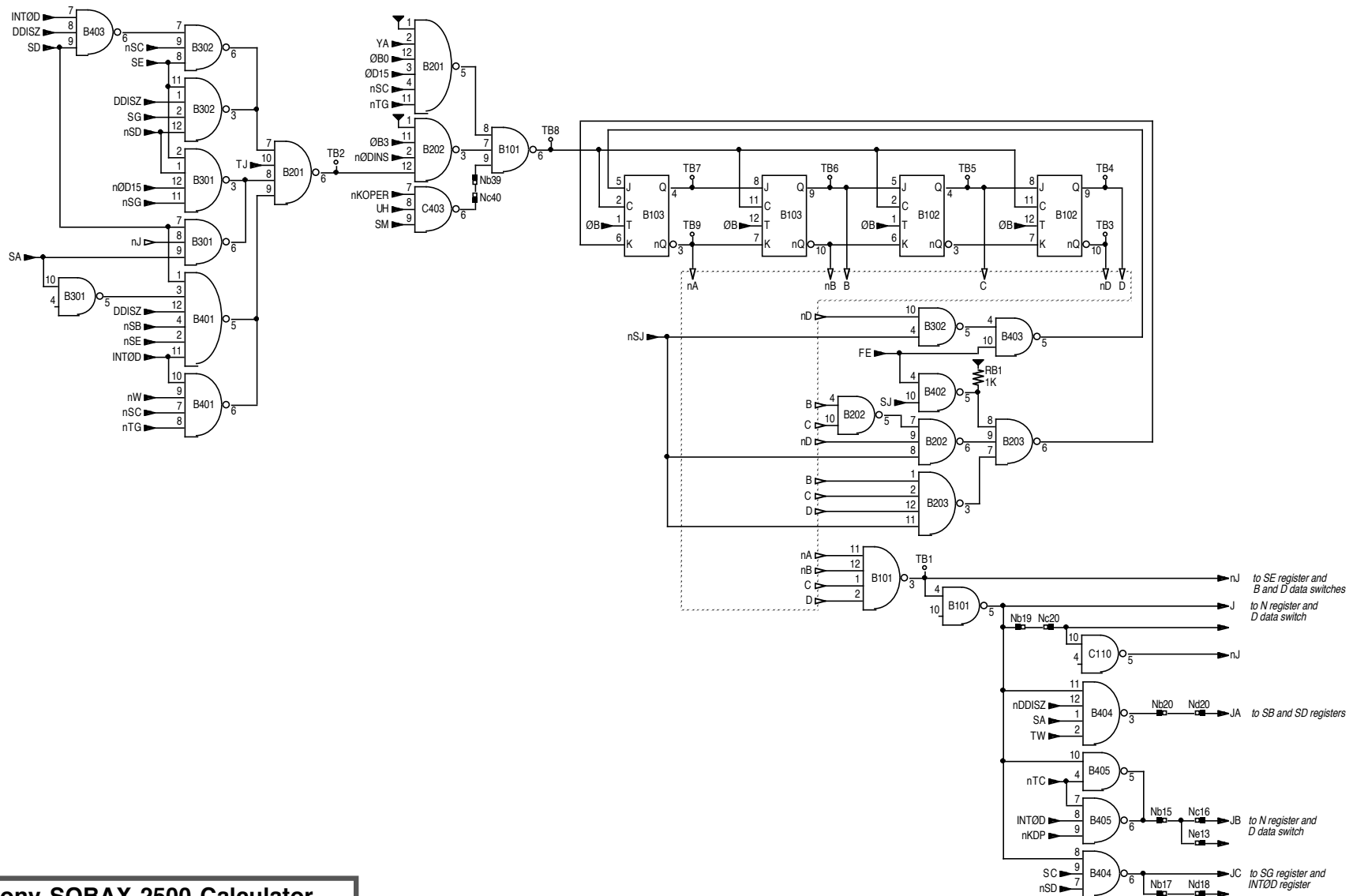
Section: Control (part 2)

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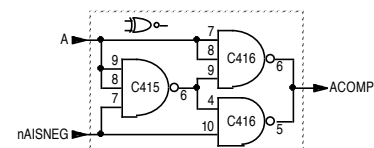
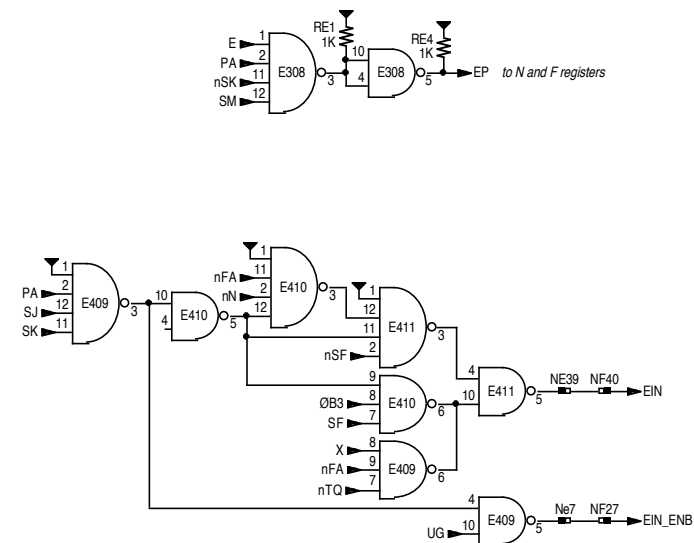
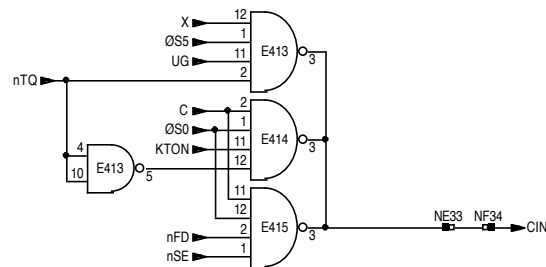
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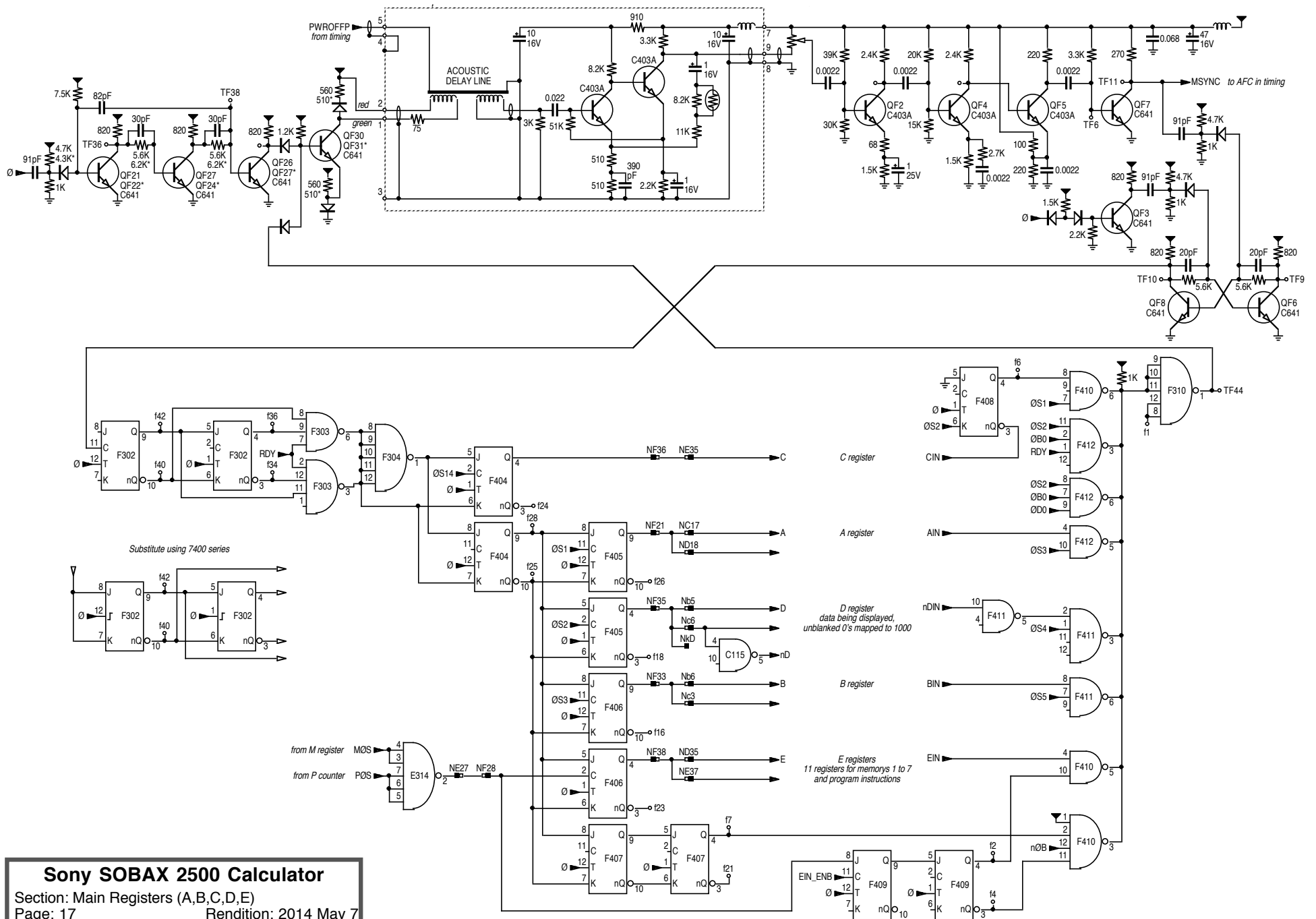
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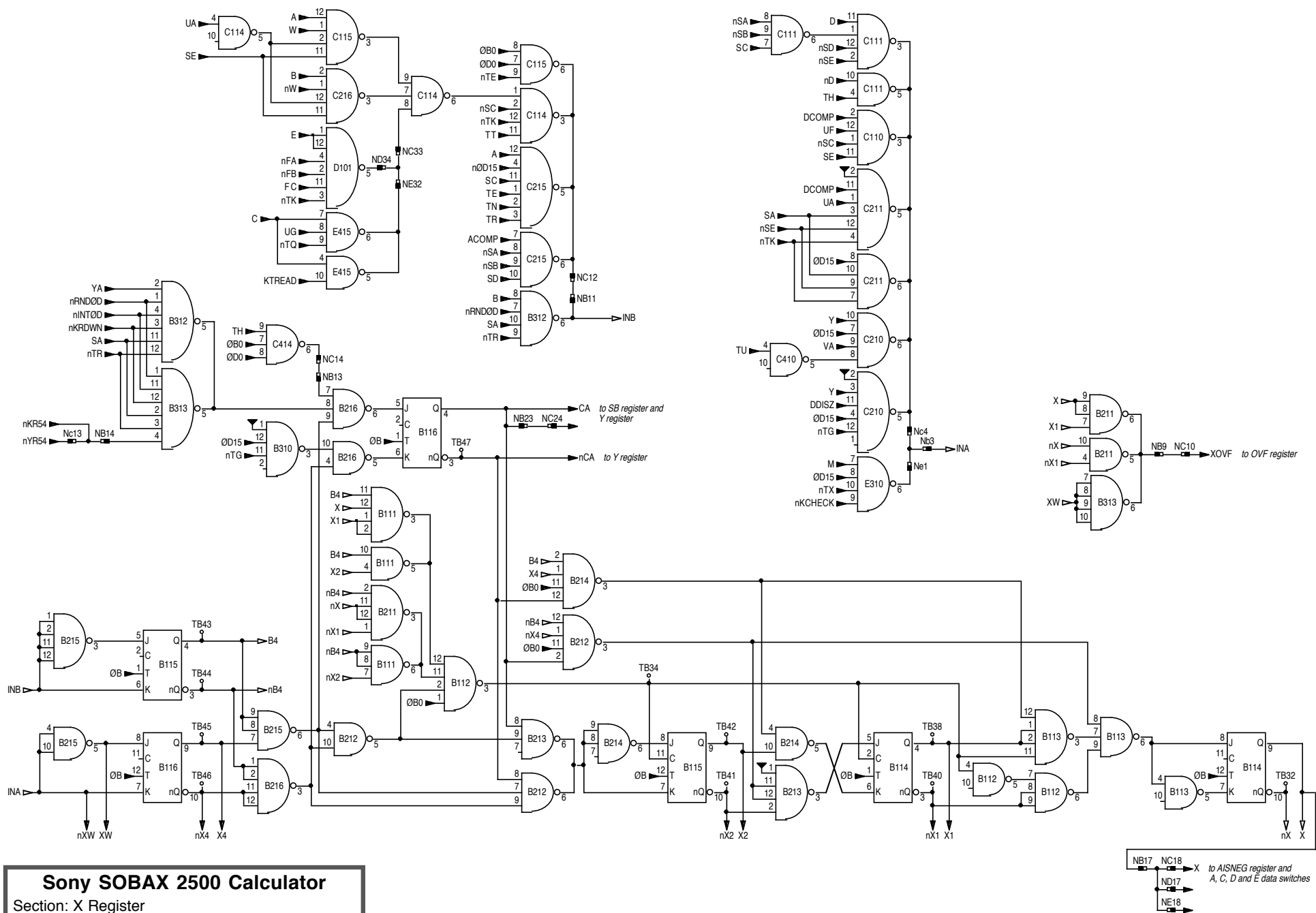


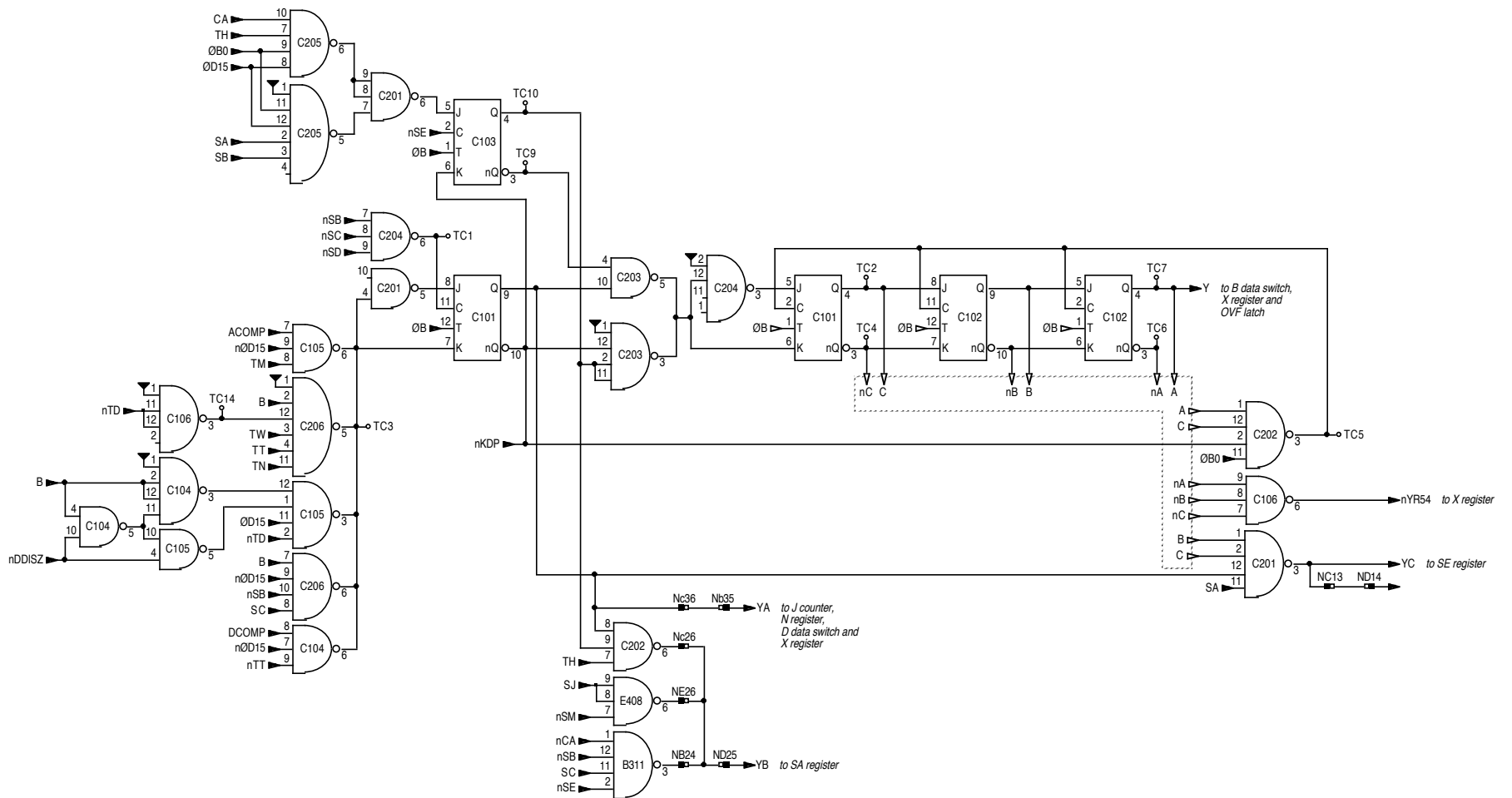
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Section: Main Register (A,B,C,D,E) Data Switches
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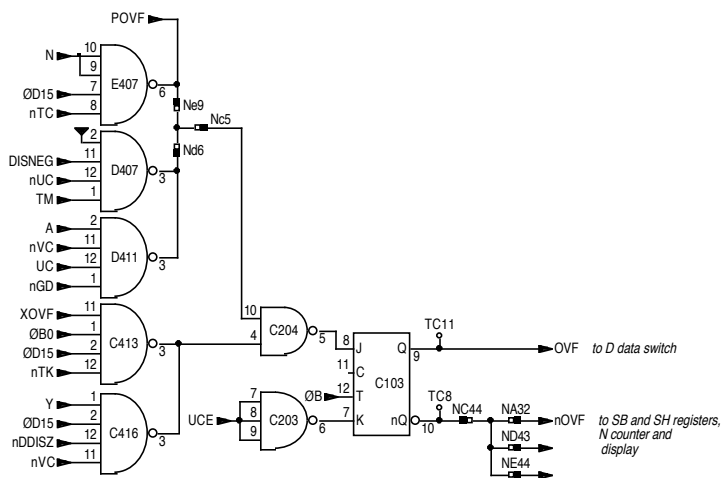
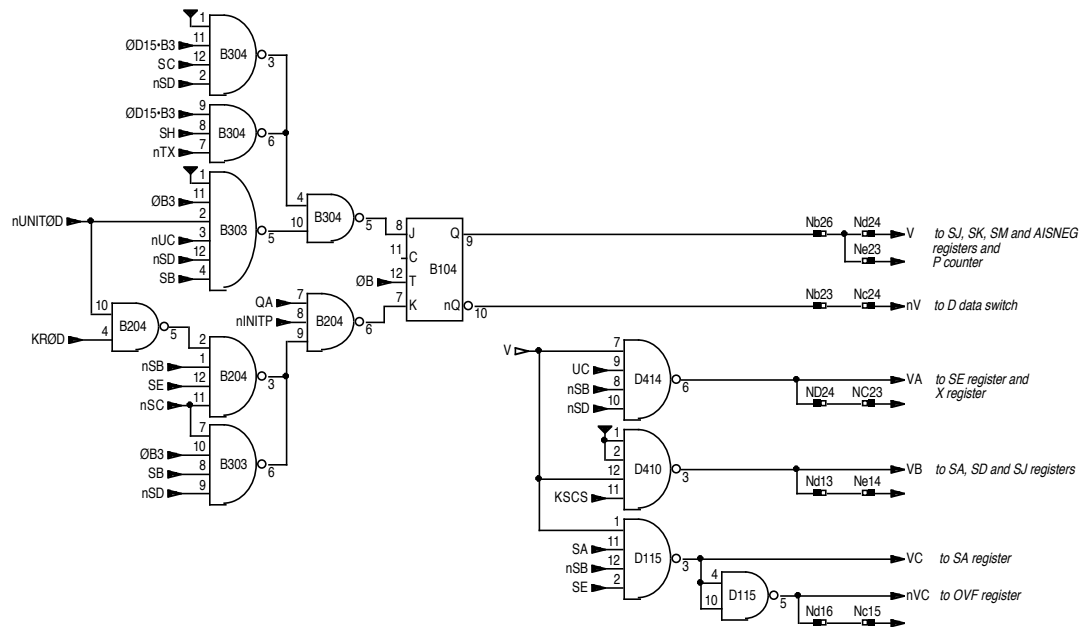
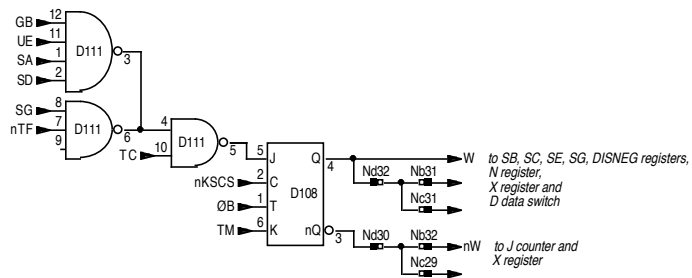
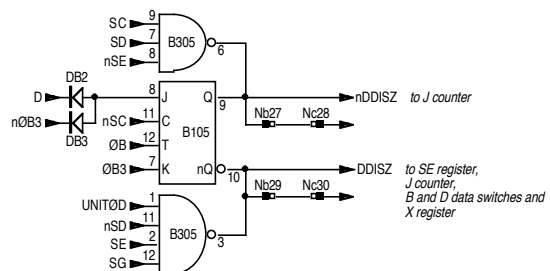
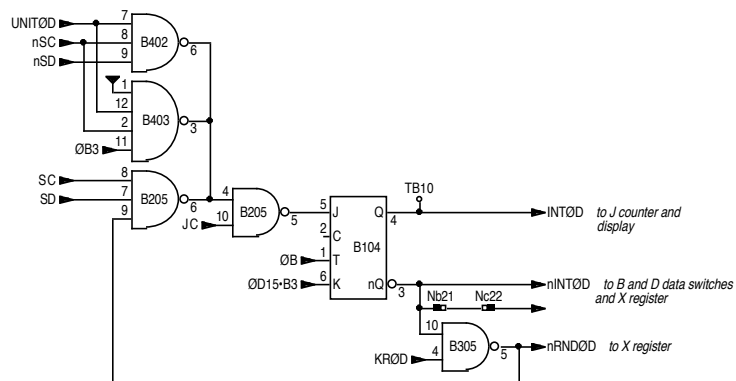


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Section: Y Register

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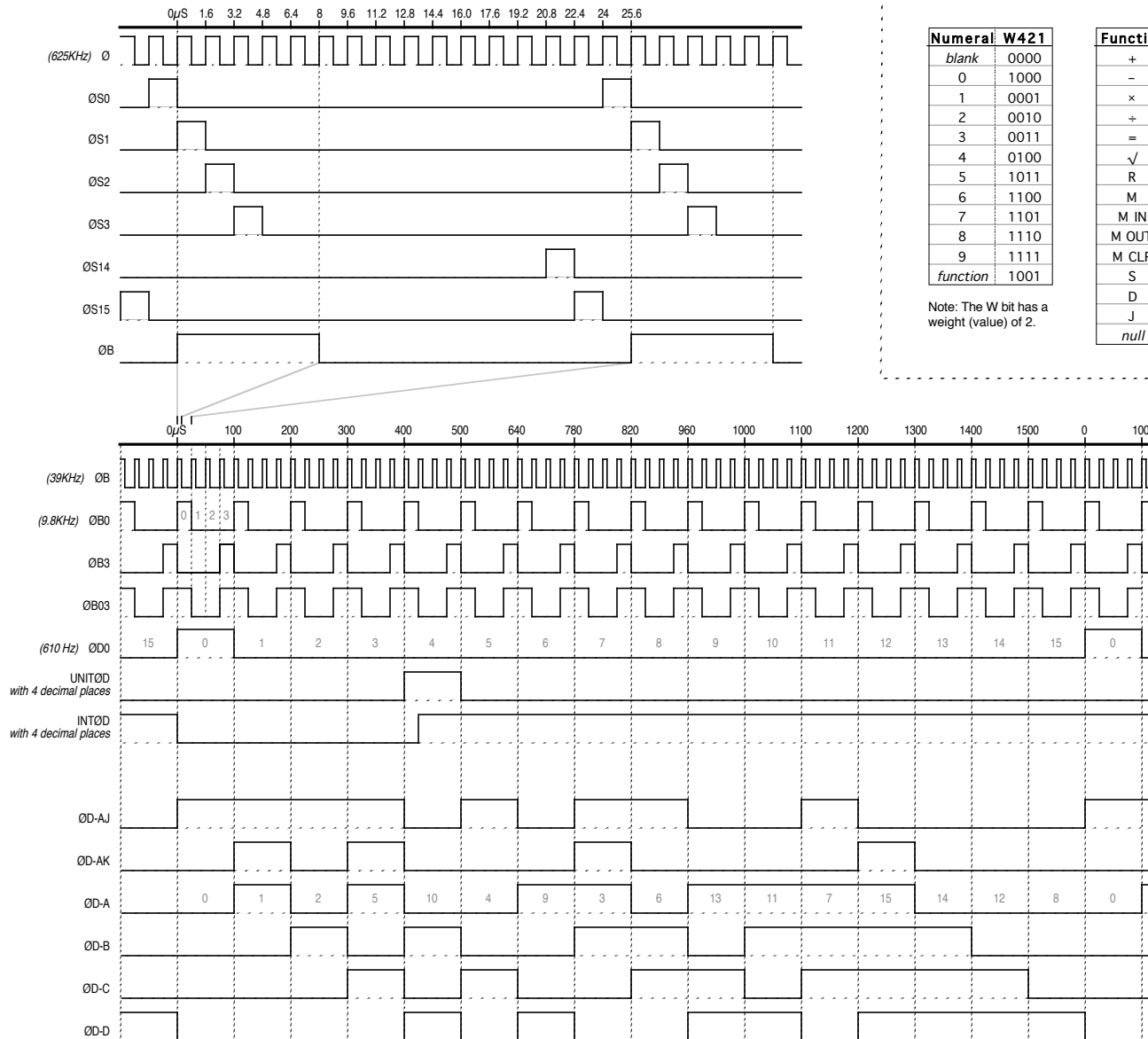
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Section: Misc. Registers

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Timing Signals



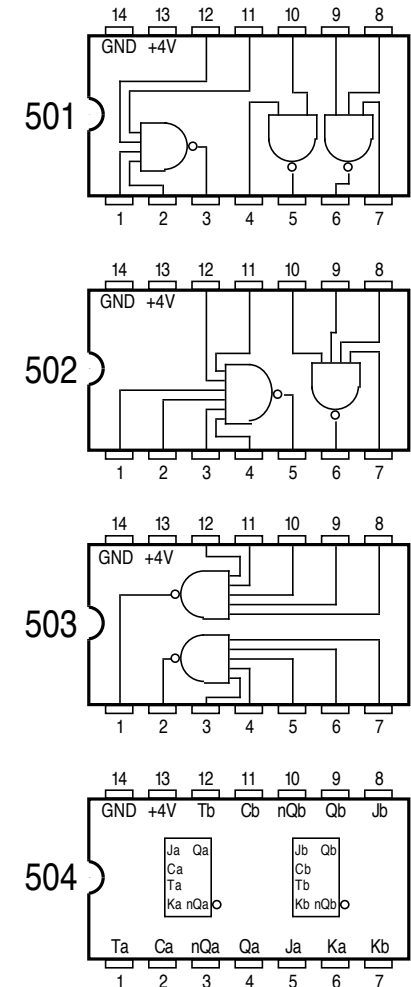
Bit Codes

Numerical	W421
blank	0000
0	1000
1	0001
2	0010
3	0011
4	0100
5	1011
6	1100
7	1101
8	1110
9	1111
function	1001

Note: The W bit has a weight (value) of 2.

Function	DCBA
+	1110
-	0110
×	0111
÷	1111
=	1001
√	1011
R	1101
M	1010
M IN	0100
M OUT	1100
M CLR	0101
S	1000
D	0010
J	0011
null	0000

IC Pinouts



IC technology inferred to be DTL inputs with open-collector outputs.

Inferred for 504 flip-flops:

C = Capture Input

T = Toggle (Clock) Input

The J/K state is captured when C is HIGH and T is LOW. Q and Q are set in accordance with the captured state when T goes HIGH.

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Section: Timing Diagram, Bit Codes & IC Pinouts
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Note: Frequencies shown are approximate, may vary with unit and temperature.

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Section: Connectors
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Notes:
• Italicised expressions are connections with no signal name in the schematic.

• Bold-faced expressions are signal sources.

A			nSC 2 1 SC			SC 2 1 nSC			nSC 2 1 F44			nSC 2 1 X INA			F						
nØD0	44	43	9	9	44	43	ØD0	nOVF	44	43	TA	nOVF	nOVF	44	43	F43	d1, e26	44	43	E43	
nØD2	42	41	–	n8	42	41	nSD	nSD	42	41	nTT	nSD	nSE	42	41	TA	e11	42	41	nKLEARN	
nØD4	40	39	7	7	40	39	CHGSGN	SD	40	39	TU	SD	nØD0	40	39	EIN	EIN	40	39	nDIN	
n8	38	37	6	6	38	37	nØD11	nSE	38	37	TF	nSE	KTON	38	37	E	E	38	37	nKCHECK	
nØD11	36	35	5	5	36	35	SE	SE	36	35	TS	E	SE	36	35	C	C	36	35	D	
–	34	33	4	4	34	33	nSB	nSB	34	33	E32	CHGSGN	nSB	34	33	CIN	CIN	34	33	B	
nOVF	32	31	3	3	32	31	SB	SB	32	31	BIN	nSA	C33, D34	32	31	ØD0	ØD0	32	31	BIN	
–	30	29	2	2	30	29	nØD0	nTK	30	29	nTK	nTQ	nTQ	30	29	nKFD	AIN	30	29	SJ	
–	28	27	1	1	28	27	SA	SA	28	27	TB	KTREAD	KTREAD	28	27	E ØS	E ØS	28	27	EIN_ENB	
–	26	25	0	0	26	25	D26	ØD0	26	25	AIN	e3, B25	YB	26	25	F26	E25	26	25	pwr off	
ØB3	24	23	–	YB	24	23	CA	CA	24	23	VA	VA	–	24	23	–	ØS5	24	23	pwr off	
nØD15	22	21	–	nØD15	22	21	ØD15	ØD15	22	21	nØD15	RDY	ØB3	22	21	ØS10	ØS10	22	21	A	
MEM1	20	19	–	Q	20	19	ØB3	ØB3	20	19	DISNEG	Q	ØD15	20	19	ØS14	ØS14	20	19	ØB3	
DISNEG	18	17	nØDINS	nØDINS	18	17	X	X	18	17	A	MAR	X	X	18	17	ØS0	ØS0	18	17	ØD15•B3
funct ind.	16	15	DP	funct ind.	16	15	ØB0	ØB0	16	15	D16	C15	–	MEM1	16	15	ØS4	RDY	16	15	ØS4
PEXP	14	13	RDY	nYR54	14	13	C14	B13	14	13	YC	YC	– (UE)	PEXP	14	13	P1ST	ØB0	14	13	GND
P1ST	12	11	nKCHECK	DP	12	11	X INB	X INB	12	11	TN	TN	E12	D11	12	11	nINITP	nINITP	12	11	GND
ØB	10	9	ØB	nINITP	10	9	XOVF	XOVF	10	9	TT	TT	SK	SK	10	9	Ø	Ø	10	9	V–10
V+4	8	7	V+4	ØD15•B3	8	7	nØB3	nØB3	8	7	TM	TM	ØD15•B3	ØD15•B3	8	7	Ø	Ø	8	7	V+4
GND	6	5	GND	ØB	6	5	ØB	ØB	6	5	ØB	ØB	ØB	ØB	6	5	ØB	ØB	6	5	ØB
V+8 unreg	4	3	V+8 unreg	V+4	4	3	V+4	V+4	4	3	V+4	V+4	V+4	V+4	4	3	V+4	V+4	4	3	V+4
V+200	2	1	V+130	GND	2	1	GND	GND	2	1	GND	GND	GND	GND	2	1	GND	GND	2	1	GND